

HITACHI IC MEMORY DATA BOOK

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HM10414-1	256-word × 1-bit RAM (ECL 10K)	572
HM10422	256-word × 4-bit RAM (ECL 10K)	576
HM10422-7	256-word × 4-bit RAM (ECL 10K)	581
HM2110	1024-word × 1-bit RAM (ECL 10K)	584
HM2110-1	1024-word × 1-bit RAM (ECL 10K)	584
HM2112	1024-word × 1-bit RAM (ECL 10K)	588
HM2112-1	1024-word × 1-bit RAM (ECL 10K)	588
HM10474	1024-word × 4-bit RAM (ECL 10K)	593
HM10474-8	1024-word × 4-bit RAM (ECL 10K)	598
HM10474-10	1024-word × 4-bit RAM (ECL 10K)	598
HM10470	4096-word × 1-bit RAM (ECL 10K)	601
HM10470-1	4096-word × 1-bit RAM (ECL 10K)	601
HM10470-20	4096-word × 1-bit RAM (ECL 10K)	606
HM2142	4096-word × 1-bit RAM (ECL 10K)	609
HM10480	16384-word × 1-bit RAM (ECL 10K)	612
HM10480F	16384-word × 1-bit RAM (ECL 10K)	612
HM10480-15	16384-word × 1-bit RAM (ECL 10K)	615
HM10480F-15	16384-word × 1-bit RAM (ECL 10K)	615
HM10480L	16384-word × 1-bit RAM (ECL 10K)	618
HM100422	256-word × 4-bit RAM (ECL 100K)	621
HM100422F	256-word × 4-bit RAM (ECL 100K)	621
HM100422CG	256-word × 4-bit RAM (ECL 100K)	621
HM100415	1024-word × 1-bit RAM (ECL 100K)	624
HM100415CG	1024-word × 1-bit RAM (ECL 100K)	624
HM100474	1024-word × 4-bit RAM (ECL 100K)	627
HM100474F	1024-word × 4-bit RAM (ECL 100K)	627
HM100474-8	1024-word × 4-bit RAM (ECL 100K)	632
HM100474F-8	1024-word × 4-bit RAM (ECL 100K)	632
HM100474-10	1024-word × 4-bit RAM (ECL 100K)	632
HM100474F-10	1024-word × 4-bit RAM (ECL 100K)	632
HM100470	4096-word × 1-bit RAM (ECL 100K)	635
HM100480-15	16384-word × 1-bit RAM (ECL 100K)	638
HM100480F-15	16384-word × 1-bit RAM (ECL 100K)	638

MEDICAL APPLICATIONS

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NOTICE

The example of an applied circuit or combination with other equipment shown herein indicates characteristics and performance of a semiconductor-applied products. The company shall assume no responsibility for any problem involving a patent caused when applying the descriptions in the example.

■ QUICK REFERENCE GUIDE TO HITACHI MEMORIES

■ MOS RAM

Mode	Total Bit	Type No.	Process	Organization (Word×bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package †								Page							
									Pin No.	G	P	FP	SP	ZP	CG	CP		M						
Static	4k-bit	HM6148H-45	CMOS	1024×4	45	45	+5	1.1m/0.175	18	●								52						
		HM6148H-55			55	55				●								52						
		HM6148HL-45			45	45		●										58						
		HM6148HL-55			55	55		●										58						
		HM6147H-35			35	35		●										63						
		HM6147H-45			45	45		●										63						
		HM6147H-55			55	55		●										63						
		HM6147HL-35			35	35		●										69						
		HM6147HL-45			45	45		●										69						
		HM6147HL-55			55	55		●										69						
	16k-bit	4k-bit		HM6116-2	2048×8	4096×1		120	120	+5	0.1m/0.2	24	●	●							73			
				HM6116-3				150	150				●	●							73			
				HM6116-4				200	200		●		●								73			
				HM6116L-2				120	120		●		●								84			
				HM6116L-3				150	150		●		●								84			
				HM6116L-4				200	200		●		●								84			
				HM6116A-12				120	120		●			●							95			
				HM6116A-15				150	150		●			●							95			
				HM6116A-20				200	200		●			●							95			
				HM6116AL-12				120	120		●			●							102			
		HM6116AL-15		150		150		●			●							102						
		HM6116AL-20		200		200		●			●							102						
		16k-bit		16k-bit		HM6168H-45		4096×4	16384×1		45	45	+5	0.1m/0.2	20	●								106
						HM6168H-55					55	55				●								106
						HM6168H-70					70	70		●										106
						HM6168HL-45					45	45		●										112
						HM6168HL-55					55	55		●										112
						HM6168HL-70					70	70		●										112
						HM6268-25*					25	25		●										117
						HM6268-35*					35	35		●										117
						HM6268L-25*					25	25		●										121
						HM6268L-35*					35	35		●										121
	HM6167-6				85	85				●											126			
	HM6167-8				100	100				●											126			
	64k-bit	64k-bit		HM6167L-6	8192×8	16384×1		85	85	+5	0.1m/0.15	28	●								132			
				HM6167L-8				100	100				●								132			
				HM6167H-55				55	55		●										136			
				HM6167H-70				70	70		●										136			
				HM6167HL-55				55	55		●										143			
				HM6176HL-70				70	70		●										143			
				HM6267-35				35	35		●								●		147			
				HM6267-45				45	45		●								●		147			
				HM6267L-35				35	35		●										157			
				HM6267L-45				45	45		●										157			
	64k-bit	64k-bit		HM6264-10	8192×8	16384×1		100	100	+5	0.1m/0.2	28	●	●							162			
				HM6264-12				120	120				●	●							162			
				HM6264-15				150	150		●		●								162			
				HM6264L-10				100	100		●		●								172			
				HM6264L-12				120	120		●		●								172			

(to be continued)

QUICK REFERENCE GUIDE

Mode	Total Bit	Type No.	Process	Organization (word x bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package †								Page						
									Pin No.	G	P	FP	SP	ZP	CG	CP		M					
Static	64k-bit	HM6264L-15	CMOS	8192 x 8	150	150	+5	5μ/0.2	28		●	●						172					
		HM6264L-10L			100	100					●	●						184					
		HM6264L-12L			120	120					●	●						184					
		HM6264L-15L			150	150					●	●						184					
		HM6264A-12			120	120						●	●					194					
		HM6264A-15			150	150					●	●					194						
		HM6264AL-12			120	120					●	●					201						
		HM6264AL-15			150	150					●	●					201						
		HM6288-35*			35	35		16384 x 4		Bi-CMOS	+5	0.1m/15m		●									209
		HM6288-45*			45	45								●								209	
	HM6288-55*	55	55		●												209						
	HM6788-30*	30	30		●												213						
	HM6287-45	45	45			●								●			218						
	HM6287-55	55	55	65536 x 1	CMOS	+5	0.1m/0.3					●				●				218			
	HM6287-70	70	70									●				●				218			
	HM6287L-45	45	45									●								224			
	HM6287L-55	55	55									●								224			
	HM6287L-70	70	70									●								224			
	HM6787*	25	25				Bi-CMOS	+5	38m/0.15		●					●				229			
	HM6787-30*	30	30								●					●			229				
Static RAM Module	256k-bit	HM62256-8	CMOS				32768 x 8	85	85	+5	0.2m/40m	28		●	●						234		
		HM62256-10						100	100					●	●						234		
		HM62256-12						120	120					●	●						234		
		HM62256-15		150	150			●	●									234					
		HM62256L-8		85	85			●	●								239						
		HM62256L-10		100	100			●	●								239						
		HM62256L-12		120	120			●	●								239						
		HM62256L-15		150	150			●	●								239						
	Pseudo Static	256k-bit	HM66202-12	CMOS	32768 x 8	120	120	+5	0.4m/0.2		30									●	245		
			HM66202-15			150	150														●	245	
HM66202-20			200			200												●	245				
HM66202L-12			120			120											●	251					
HM66202L-15			150			150											●	251					
HM66202L-20			200			200											●	251					
1M-bit		HM66203-10**	100	100	131072 x 8				+5	0.8m/40m		32								●	257		
		HM66203-12**	120	120															●	257			
		HM66203L-10**	100	100									40μ/40m								●	257	
		HM66203L-12**	120	120															●	257			
HM66203L-15**	150	150											●	257									
Pseudo Static	256k-bit	HM65256A-12	CMOS	32768 x 8	120	190	+5	2m/0.175	28		●		●					260					
		HM65256A-15			150	235					●		●					260					
		HM65256A-20			200	310					●		●					260					
		HM65256B-12*			120	190					●	●	●					267					
		HM65256B-15*			150	235				●	●	●					267						
		HM65256B-20*			200	310				●	●	●					267						
		HM65256BL-12*			120	190				●	●	●					274						
		HM65256BL-15*			150	235				●	●	●					274						
		HM65256BL-20*			200	310				●	●	●					274						

(to be continued)

Mode	Total Bit	Type No.	Process	Organization (word×bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package †								Page			
									Pin No.	G	P	FP	SP	ZP	CG	CP		M		
Dynamic	256k-bit	HM50464-12	NMOS	65536×4	120	220	+5	20m/0.35	18		●					●	282			
		HM50464-15			150	260				●				●	282					
		HM50464-20			200	330				●				●	282					
		HM50465-12			120	220				●				●	290					
		HM50465-15			150	260				●				●	290					
		HM50465-20			200	330				●				●	290					
		HM50256-12		120	220	20m/0.35		16	●		●			●	298					
		HM50256-15		150	260				●		●		●	298						
		HM50256-20		200	330				●		●		●	298						
		HM50256A-10**		100	190				●					306						
		HM50256A-12**		120	220				●					306						
		HM50256A-15**		150	260				●					306						
		HM50257-12		120	220	20m/0.35		16	●			●		●	307					
		HM50257-15		150	260				●		●		●	307						
		HM50257-20		200	330				●		●		●	307						
		HM50257A-10**		100	190				●					315						
		HM50257A-12**		120	220				●					315						
		HM50257A-15**		150	260				●					315						
	HM51256-10*	100	180	CMOS	262144×1	100	180	+5	5m/0.2	16	●					●	316			
	HM51256-12*	120	210			●							●	316						
	HM51256-15*	150	250			●							●	316						
	HM51256L-10*	100	180			●							●	324						
	HM51256L-12*	120	210			●							●	324						
	HM51256L-15*	150	250			●							●	324						
	HM51258-8	85	155			5m/0.2	16				●				●	332				
	HM51258-10	100	180								●				●	332				
	HM51258-12	120	210								●				●	332				
	HM51258-15	150	250								●				●	332				
	HM511000-10*	100	190								1048576×1	5m/0.2	18	●	●					340
	HM511000-12*	120	220											●	●				340	
	HM511000-15*	150	260			●	●										340			
	HM511001-10*	100	190			●	●										348			
	HM511001-12*	120	220			●	●										348			
HM511001-15*	150	260	●	●				348												
HM511002-10*	100	190	●	●				357												
HM511002-12*	120	220	●	●				357												
HM511002-15*	150	260	●	●				357												
Multi-Port DRAM	256k-bit	HM53461-10*	65536×4	1048576×1	100	190	+5	10m/0.4	24		●						366			
		HM53461-12*			120	220				●				366						
		HM53461-15*			150	260				●				366						
		HM53462-10*			100	190				●				382						
		HM53462-12*			120	220				●				382						
		HM53462-15*			150	260				●				382						
DRAM Module	1M-bit	HB561004A-12	NMOS	262144×4	120	220	+5	60m/1.21	22							●	415			
		HB561004A-15			150	260				●				415						
		HB561004A-20			200	330				●				415						
		HB561005A-12		120	220	262144×5		75m/1.51	24						●	423				
		HB561005A-15		150	260					●				423						
		HB561005A-20		200	330					●				423						

(to be continued)

QUICK REFERENCE GUIDE

Mode	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns)max	Cycle Time (ns)min	Supply Voltage (V)	Power Dissipation (W)	Package †								Page
									Pin No.	G	P	FP	SP	ZIP	CG	CP	
DRAM Module	2M-bit	HB561008B-12	NMOS	216444 × 8	120	220	+ 5	0.12 2.42	30							●	431
		HB561008B-15			150	260		0.12 1.92							●	431	
		HB561008B-20			200	330		0.12 1.51							●	431	
		HB561003A-12			120	220		0.135 2.55							●	406	
		HB561003A-15		150	260	0.135 2.16								●	406		
		HB561003A-20		200	330	0.135 1.70								●	406		
		HB561003B-12		120	220	0.135 2.55								●	406		
		HB561003B-15		150	260	0.135 2.16								●	406		
		HB561003B-20		262144 × 9	200	330		0.135 1.70							●	406	

* Preliminary ** Under Development

† The package codes of G, P, FP, SP, ZIP, CG, CP, and M are applied to the Package materials as follows.

G : Cerdip, P : Plastic DIP, FP : Flat Plastic Package(SOP), SP : Skinny Type Plastic DIP,

ZIP : Plastic ZIP, CG : Ceramic Leadless Chip Carrier, CP : Plastic Leaded Chip Carrier

M : Module

■ MOS ROM

Mode	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package †				Page	
								Pin No.	G	P	FP		
Mask	64k-bit	HN61361	CMOS	8192 × 8	250	+ 5	5μ 50m	28		●	●		440
		HN61365								●			442
		HN61366								●			444
	128k-bit	HN613128		16384 × 8	250		5μ 50m	28		●	●		446
		HN61256		32768 × 8	3500		5μ 7.5m			●	●		448
	256k-bit	HN613256		32768 × 8	250		5μ 75m	28		●	●		450
		HN623256			150		5μ 100m			●	●		452
	1M-bit	HN62101		131072 × 8	5000		5μ 10m	28		●	●		454
		HN62301A			250		2.5m 75m			●	●		456
		HN62301B*			150		5μ 0.1			●	●		459
		HN62301D*								●	●		462
	2M-bit	HN62402*		131072 × 16	200		5μ 0.1	40		●			465
		HN62302*		262144 × 8	200		5μ 0.1			●			468
	U. V. Erasable & Electrically	64k-bit		HN482764	NMOS		8192 × 8	250	+ 5	50m 0.15	28		●
HN482764-2			200	●								472	
HN482764-3			300	●								472	
HN27C64-15			150	●								482	
HN27C64-20			200	●								482	
HN27C64-25		250	●			482							
128k-bit		HN27128A-17	NMOS	16384 × 8	170	+ 5	80m 0.3	28		●			494
		HN27128A-20			200				●			494	
		HN27128A-25			250				●			494	
		HN27128A-30			300				●			494	
256k-bit		HN27256-25	CMOS	32768 × 8	250	+ 5	50m 0.2	28		●			507
		HN27256-30			300				●			507	
		HN27C256-17			170				●			516	
		HN27C256-20			200				●			516	
		HN27C256-25			250				●			516	
HN27C256-30		300	●			516							
512k-bit		HN27512-25	NMOS	65536 × 8	250	+ 5	50m 0.2	28		●			527
		HN27512-30			300				●			527	
1M-bit		HN27C1024-15**	CMOS	65536 × 16	150	+ 5	5μ 50m	40		●			540
		HN27C1024-20**			200				●			540	
	HN27C101-20*	200			●						541		
	HN27C101-25*	250			●						541		

(to be continued)

Mode	Total Bit	Type No.	Process	Organization (word × bit)	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package †			Page			
								Pin No.	G	P		FP		
U. V. Erasable & Electrically	1M-bit	HN27C301-20*	CMOS	131072 × 8	200		5μ 50m				548			
		HN27C301-25*			250						548			
One Time Electrically	64k-bit	HN482764	NMOS	8192 × 8	250		50m 0.15				477			
		HN482764-3			300						477			
		HN27C64-20	CMOS		200						5μ 20m			489
		HN27C64-25			250							489		
	128k-bit	HN27128A-20	NMOS	16384 × 8	200		80m 0.3				501			
		HN27128A-25			250						501			
	256k-bit	HN27256-25*	NMOS	32768 × 8	250		50m 0.2				512			
		HN27256-30*			300						512			
		HN27C256-20	CMOS		200						5μ 20m			522
		HN27C256-25			250							522		
	512k-bit	HN27C256-30		300	522									
		HN27512-25*	NMOS	65536 × 8	250		50m 0.2				534			
HN27512-30*	300	534												
Electrically Erasable & Programmable	64k-bit	HN58064-25	NMOS	8192 × 8	250		0.1 0.2				556			
		HN58064-30			300						556			
		HN58C65-20*	CMOS		200						5μ 20m			562
		HN58C65-25*			250							562		
		HN58C65-30*			300							562		

* Preliminary ** Under Development

† The Package codes of G,P and FP are applied to the package materials as follows.

G : Cerdip,P : Plastic DIP,FP : Plastic Flat Package

■ BIPOLAR RAM

Level	Total Bit	Type No.	Organization (word × bit)	Output	Access Time (ns)max	Supply Voltage (V)	Power Dissipation (W)	Package †			Replacement	Page			
								Pin No.	F	G			CG		
ECL 10K	256-bit	HM10414	256 × 1	Open Emitter	10	-5.2	0.7	16				F10414	572		
		HM10414-1			8									572	
	1k-bit	HM10422	256 × 4		10		0.8	24					F10422	576	
		HM10422-7			7										581
		HM2110	1024 × 1		35		0.5	16					F10415	584	
		HM2110-1			25										584
	HM2112	10			0.8								588		
	HM2112-1	8												588	
	4k-bit	HM10474	1024 × 4		25		0.8	24					F10474	593	
		HM10478-8			8										598
		HM10474-10			10										598
		HM10470	4096 × 1		25		0.8	18					F10470	601	
		HM10470-1			15										601
		HM10470-20			20										606
	HM2142	10			609										
	16k-bit	HM10480	16384 × 1		25		0.8	20					F10480	612	
HM10480-15*		15		615											
HM10480L		25		618											
ECL 100K	1k-bit	HM100422	256 × 4	10	0.8	24					F100422	621			
		HM100415	1024 × 1	10									0.6	16	
	4k-bit	HM100474	1024 × 4	25	0.8	24					F100474	627			
		HM100474-8*		8									632		
		HM100474-10*		10									632		
		HM100470		4096 × 1									25	0.8	18
	16k-bit	HM100480-15*	16384 × 1	15	0.8	20			F100480	638					

† Preliminary

* The package codes of F, Gand CG are applied to the package materials as follows.

F : Flat Package,G : Cerdip,CG : Ceramic Leadless Chip Carrier

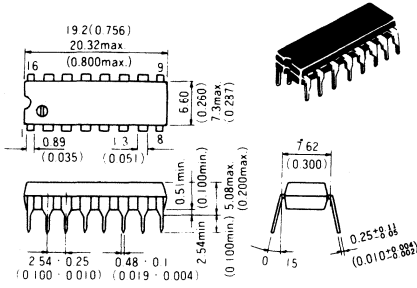


PACKAGE INFORMATION

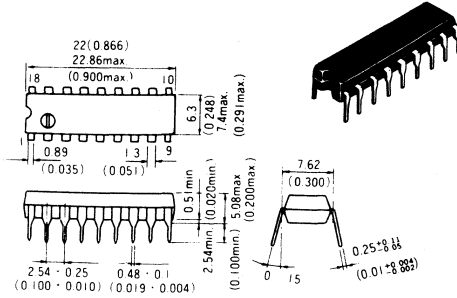
● Dual-in-line Plastic

Unit: mm (inch) Scale 1/1

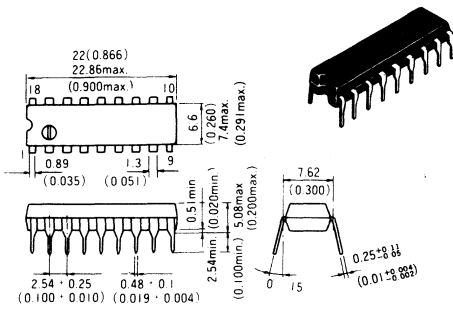
● DP-16B



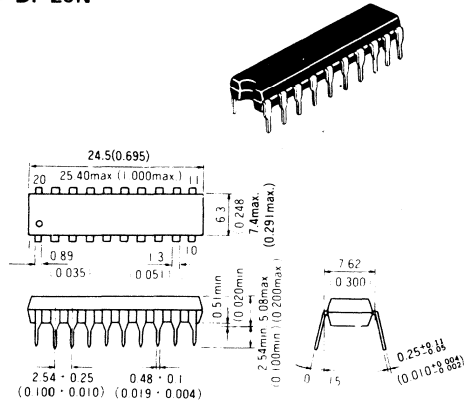
● DP-18



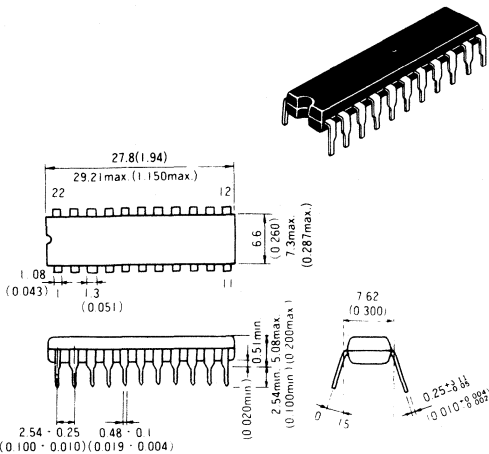
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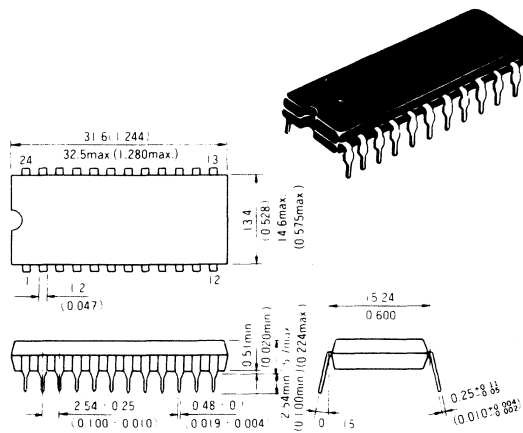
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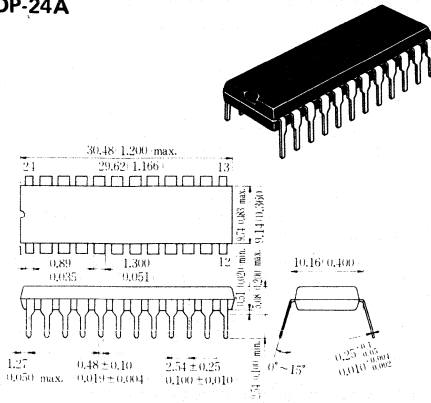
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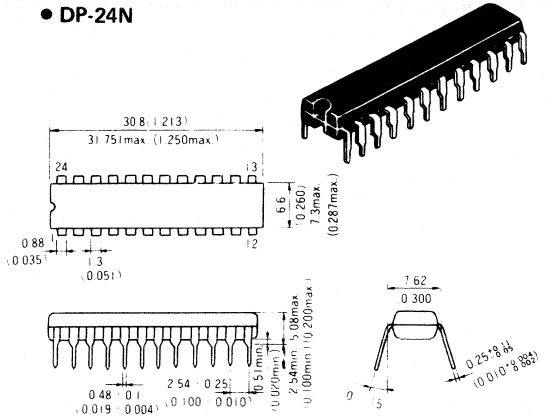
● DP-24



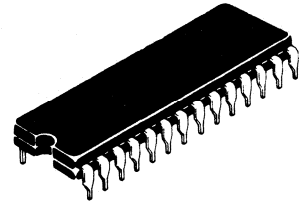
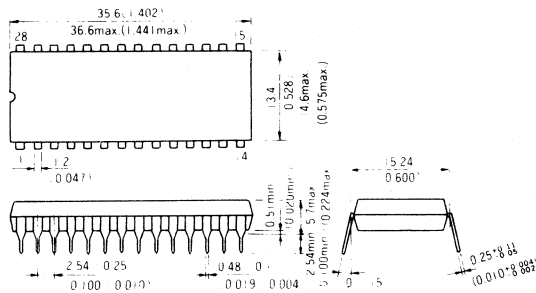
● DP-24A



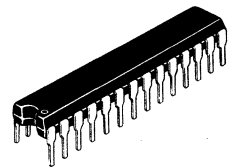
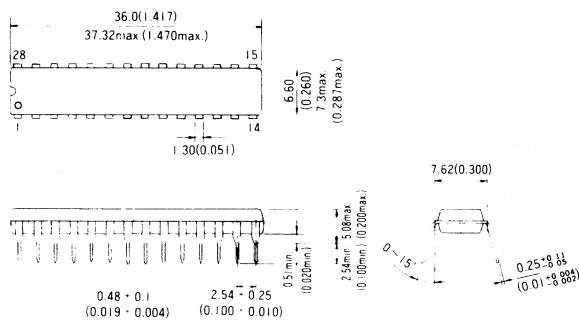
● DP-24N



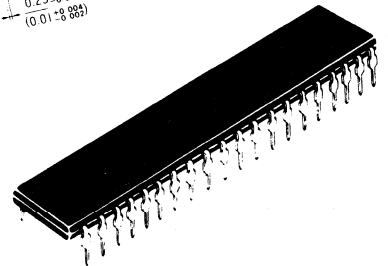
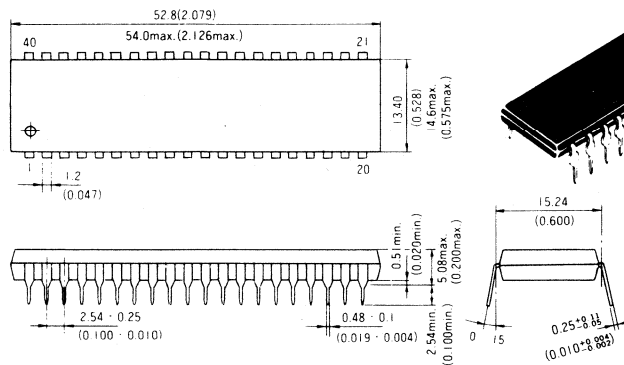
● DP-28



● DP-28N



● DP-40



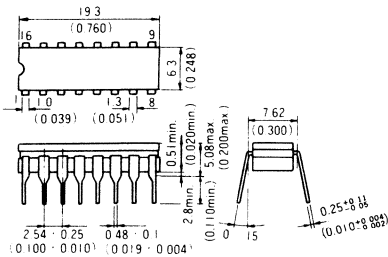
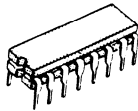
PACKAGE INFORMATION

● **Applicable ICs**

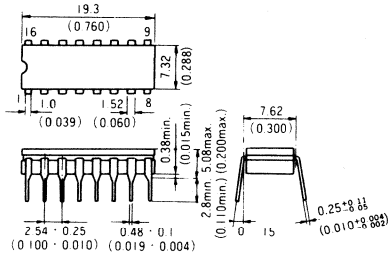
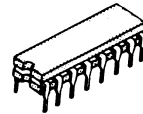
DP-16B	HM50256P Series, HM50256AP Series, HM50257P Series, HM50257AP Series, HM51256P Series, HM51256LP Series, HM51258P Series
DP-18	HM6148HP Series, HM6147HP Series, HM6147HLP Series, HM511000P Series, HM511001P Series, HM511002P Series
DP-18B	HM50464P Series, HM50465P Series
DP-20N	HM6168HP Series, HM6168HLP Series, HM6268P Series, HM6167P Series, HM6167LP, HM6167HP Series, HM6167HLP Series, HM6267P Series, HM6267LP Series,
DP-22N	HM6287P Series, HM6287LP Series, HM6288P Series,
DP-24	HM6116P Series, HM6116LP Series, HM6116AP Series, HM6116ALP Series, HN61365P, HN61366P
DP-24A	HM53461P Series, HM53462P Series
DP-24N	HM6116ASP Series, HM6116ALSP Series,
DP-28	HM6264P Series, HM6264LP Series, HM6264LP-L Series, HM62256P Series, HM62256LP Series, HM65256AP Series, HM65256BP Series, HM65256BLP Series, HN61364P, HN613128P, HN61256P, HN613256P, HN623256P, HN62101P, HN62301AP, HN62301BP, HN62301DP, HN482764P Series, HN27128AP Series, HN27256P Series, HN27512P Series, HN58064P Series, HN58C53P Series
DP-28N	HN6264ASP Series, HM6264ALSP Series, HM65256ASP Series, HM65256BSP Series, HM65256BLSP Series
DP-40	HN62302P, HN642402P

● **CERDIP**

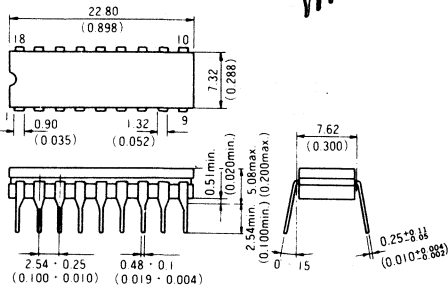
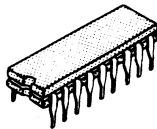
● **DG-16**



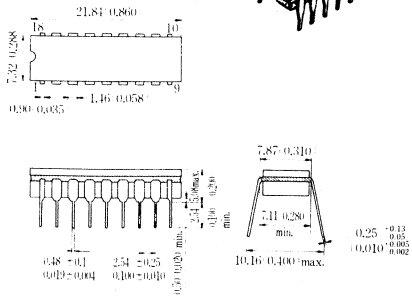
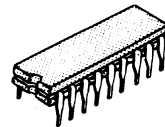
● **DG-16A**



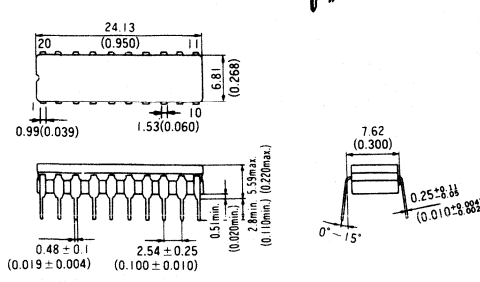
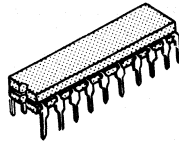
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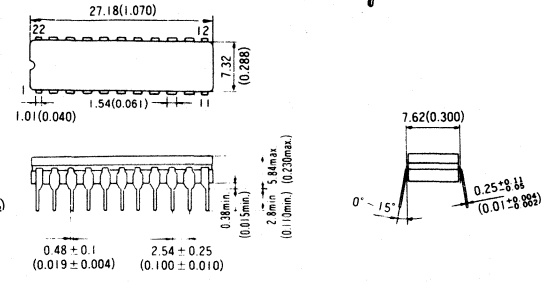
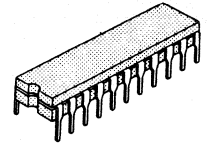
● **DG-18A**



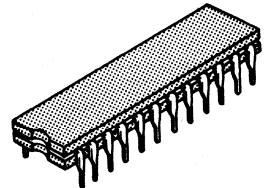
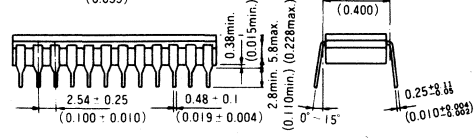
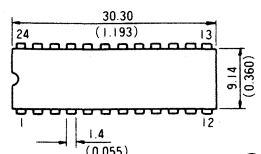
● DG-20NA



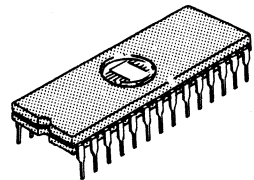
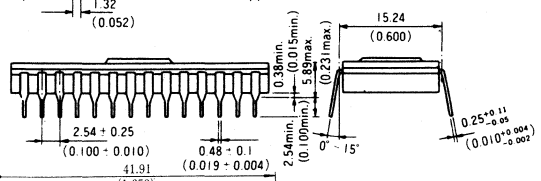
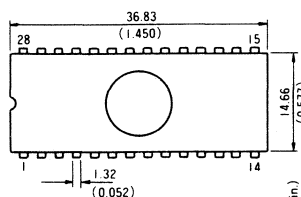
● DG-22N



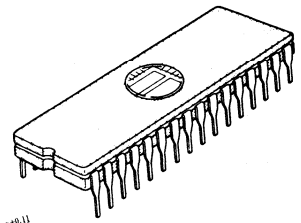
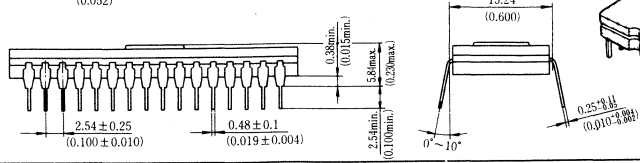
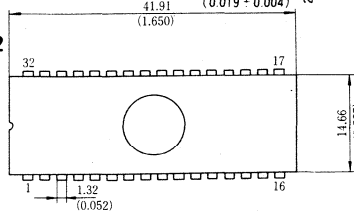
● DG-24N



● DG-28



● DG-32



PACKAGE INFORMATION

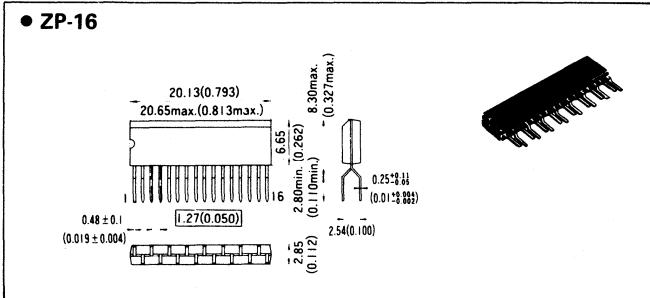
● **Applicable ICs**

DG-16	HM10414, HM1014-1
DG-16A	HM2110, HM2110-1, HM2112, HM2112-1, HM100415
DG-18	HM10470, HM10470-1, HM10470-20, HM100470
DG-18A	HM511000 Series, HM511001 Series, HM511002 Series
DG-20NA	HM2142, HM10480, HM10480-15, HM10480L, HM100480-15
DG-22N	HM6787, HM6787-30, HM6788
DG-24N	HM10422, HM10422-7, HM10474-8, HM10474-10, HM100422, HM100474, HM100474-8, HM100474-10
DG-28	HN482764G Series, HN27C64G Series, HN27128A Series, HN27256G Series, HN27C256G Series, HN27512G Series
DG-32	HN27C101G Series, HN27C301G Series

● **Zigzag-in-line Plastic**

Unit: mm (inch) Scale 1/1

● **ZP-16**



● **Applicable ICs**

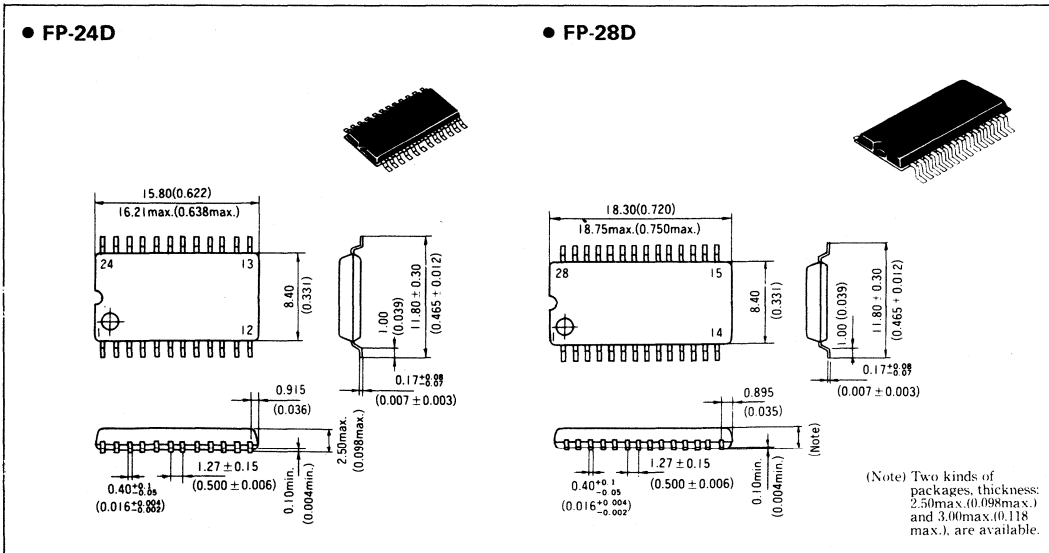
ZP-16	HM50256ZP Series, HM50257ZP Series
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● **Flat Package**

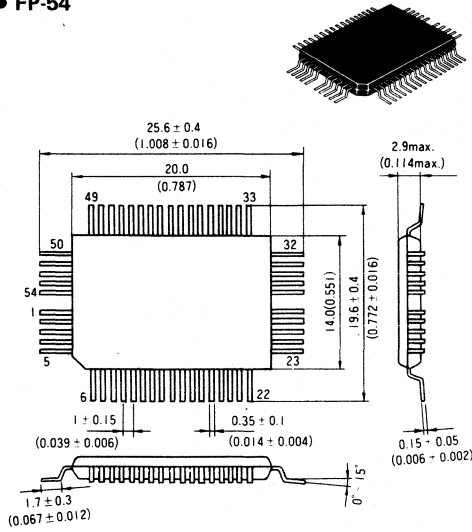
Unit: mm (inch) Scale 1-1/2

● **FP-24D**

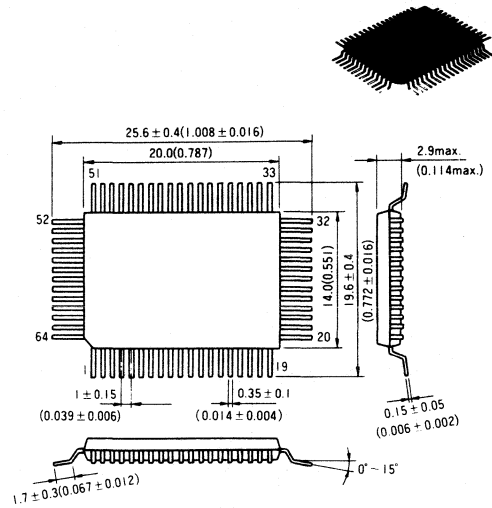
● **FP-28D**



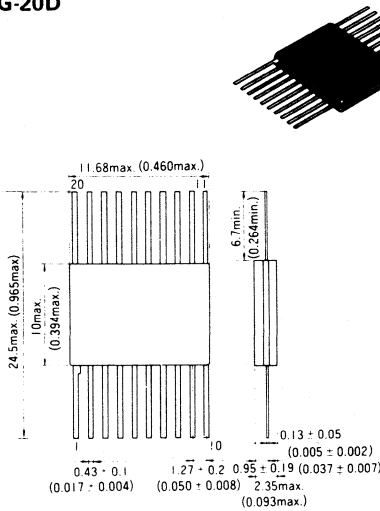
● FP-54



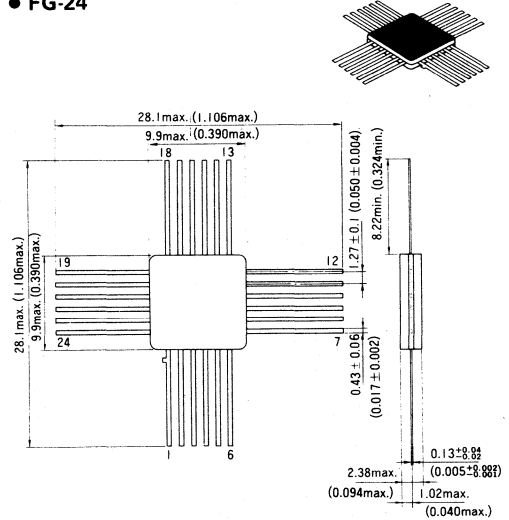
● FP-64



● FG-20D



● FG-24



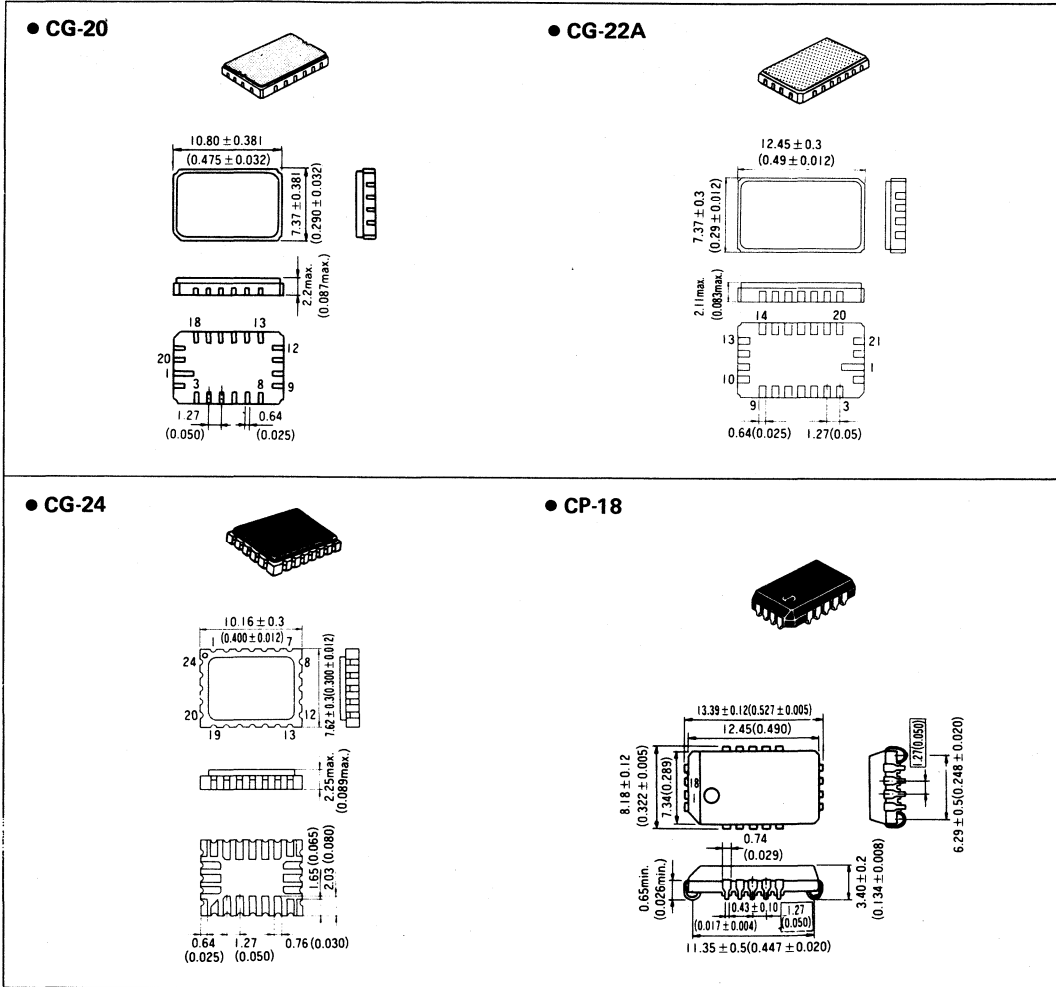
● Applicable ICs

FP-24D	HM6116FP Series, HM6116LFP Series
FP-28D	HM6264FP Series, HM6264LFP Series, HM6264LLFP Series, HM6264AFP Series, HM6264ALFP Series, HM62256FP Series, HM62256LFP Series, HM65256BFP Series, HM65256BLFP Series, HN27C64FP Series, HN27C256FP Series
FP-54	HN61364FP, HN613128FP, HN61256FP, HN613256FP, HN623256FP, HN62101FP
FP-64	HN62301AFP, HN62301BFP, HN62301DFP
FG-20D	HM10480F, HM10480F-15, HM100480F-15
FG-24	HM100422F, HM100474F, HM100474F-8, HM100474F-10

PACKAGE INFORMATION

● CHIP CARRIER

Unit: mm (inch) Scale 1-1/2



● Chip Carrier

CG-20	HM6267CG Series
CG-22A	HM6287CG Series, HM6787CG Series
CG-24	HM100422CG, HM100415CG
CP-18	HM50464CP Series, HM50465CP Series, HM50256CP Series, HM50257CP Series, HM51256CP Series, HM51256LCP Series, HM51258CP Series

RELIABILITY OF HITACHI IC MEMORIES

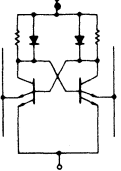
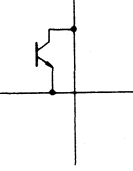
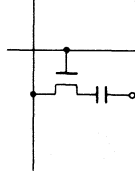
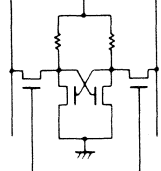
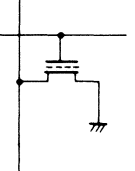
1. STRUCTURE

IC memories are basically classified into bipolar type and MOS type and utilized effectively by their characteristics. The characteristic of bipolar memories is high speed but small capacity, instead, MOS memories have large capacity. There are also differences in circuit design, layout pattern, degree of integration, and manufacturing process. These memories have been produced with the standardized concept of design and inspection all through the

processes of designing, manufacturing and inspection.

IC memories are constituted by the unit patterns called cells, which are integrated in high density. The knowhows based on our experience have been applied in every production stage. In addition, reliability has been ensured using TEG (Test Element Group) evaluation. Examples of cell circuits of bipolar and MOS memories are shown in Table 1.

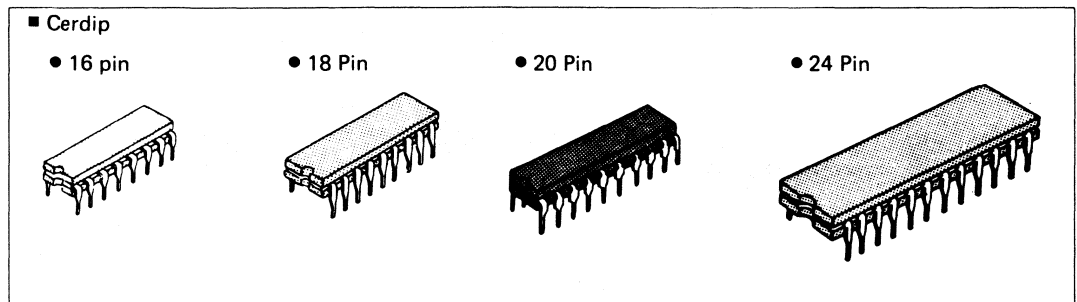
● Table 1 Basic Cell Circuit of IC Memories

Classification	Bipolar memory (RAM)	Bipolar memory (PROM)	NMOS memory (Dynamic RAM)	NMOS, CMOS memories (Static RAM)	NMOS memory (PROM)
Application	Buffer memory, control memory of high-speed computer	Microcomputer control use	Main memory of computer, microcomputer memory		For microcomputer control
Example of basic cell circuit					

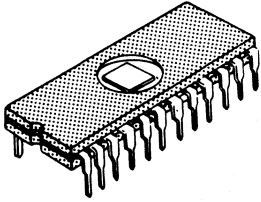
Dies of IC memories are produced in various packages. In this process of packaging, Hitachi has also innovated new techniques and ensured to high level. As packages for IC memories, cerdip (glass-sealed) packages and plastic packages are currently used. Also such packages as LCC (Leadless Chip Carrier) or SOP (Small Outline Package) have been developed for high density packaging. Cerdip packages sealed hermetically are suitable for equipment requiring high reliability. Plastic packages are widely applied to many kinds of equipment. Hitachi plastic packages have been improved the reliability

level as highly as that of the hermetically sealed packages. Table 2 shows the outlines of the Hitachi packages.

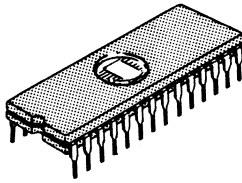
● Table 2 IC Memory Package Outline



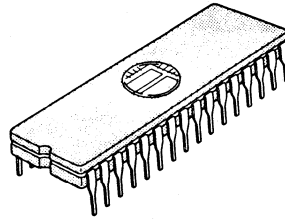
● 24 Pin with Lid



● 28 Pin with Lid



● 32 Pin with Lid

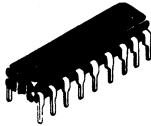


■ Plastic DIP

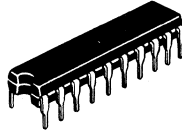
● 16 Pin



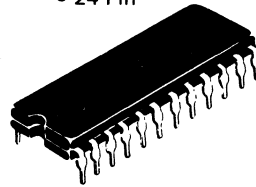
● 18 Pin



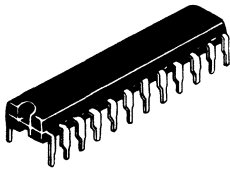
● 20 Pin



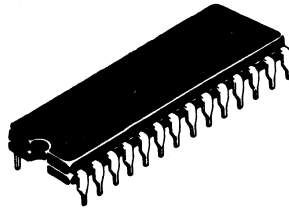
● 24 Pin



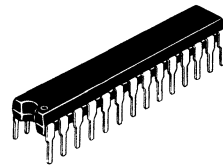
● 24 Pin



● 28 Pin



● 28 Pin



■ Leadless Chip Carrier

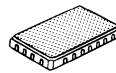
● 18 Pin



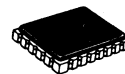
● 20 Pin



● 22 Pin

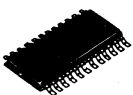


● 24 Pin

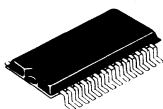


■ SOP

● 24 Pin

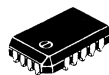


● 28 Pin



■ PLCC

● 18 Pin



■ SOJ

● 26/20 Pin



2. RELIABILITY Results of reliability tests are listed below.

2.1 Reliability Test Data on Bipolar Memories

The reliability test data on the bipolar memories are shown in Table 3 and 4. Since they are manufactured under the standardized design rules and quali-

ty control, there is no difference in reliability among the various types. And the larger the capacity is, the higher the reliability per bit becomes.

● **Table 3 Results on Bipolar Memory Reliability Test (1)**

Test item	Test condition	HM10480 (Cerdip)				HM10470 (Cerdip)				HM100422 (Flat Package)					
		samples	Total component hours	Failures	Failure rate* (1/hr)	Test condition	samples	Total component hours	Failures	Failure rate* (1/hr)	Test condition	samples	Total component hours	Failures	Failure rate* (1/hr)
High-temperature (Operating)	$T_a=125^\circ\text{C}$ $V_{EE}=4.5\text{V}$	40	C.H. 4.0×10^4	0	2.3×10^{-5}	$T_a=125^\circ\text{C}$ $V_{EE}=-5.2\text{V}$	125	C.H. 4.0×10^5	0	2.3×10^{-5}	$T_a=150^\circ\text{C}$ $V_{EE}=-5.0\text{V}$	80	C.H. 8.0×10^4	0	1.2×10^{-5}
	$T_a=150^\circ\text{C}$ $V_{EE}=-4.5\text{V}$	40	4.0×10^4	0	2.3×10^{-5}	$T_a=150^\circ\text{C}$ $V_{EE}=-5.2\text{V}$	80	2.7×10^5	0	3.4×10^{-2}		80	8.0×10^5	0	1.2×10^{-5}
High-temp. storage	$T_a=150^\circ\text{C}$	80	8.0×10^5	0	1.2×10^{-5}	$T_a=150^\circ\text{C}$	120	1.2×10^5	0	7.7×10^{-5}	$T_a=150^\circ\text{C}$	80	8.0×10^5	0	1.2×10^{-5}

● **Table 4 Results on Bipolar Memory Reliability Test (2)**

Test item	Test condition	HM10480 (Cerdip)		HM10470 (Cerdip)		HM100422 (Flat Package)	
		Samples	Failure	Samples	Failures	Sample	Failures
Temperature cycling	$-60^\circ\text{C} \sim +150^\circ\text{C}$, 10 cycles	40	0	120	0	40	0
Soldering heat	260°C , 10 seconds	22	0	22	0	—	—
Thermal shock	$0^\circ\text{C} \sim +100^\circ\text{C}$, 10 cycles	30	0	36	0	20	0
Mechanical shock	1500G, 0.5ms, Three times each for X, Y and Z	30	0	30	0	60	0
Variable frequency	100~2000Hz, 200G, Three times each for X, Y and Z	40	0	40	0	60	0
Constant-acceleration	20000G, 1 minute, each for X, Y and Z	40	0	40	0	60	0

2.2 Reliability test data on MOS memories

2.2.1 Reliability test data on MOS DRAM and SRAM

The reliability test data on the MOS memories are shown in Tables 5, 6 and 7. In these tables, data are shown on representative types of 256K DRAM (HM50256), 64K SRAM (HM6264P), 16K SRAM (HM6116P).

The life test at high temperature and high voltage is performed to estimate the reliability of the products using fewer samples. The cause of failure are all in manufacturing process, so we feedback the data into manufacturing process to improve the quality and reliability.

● **Table 5 Reliability Data on 256K and 64K DRAM**

Test item	Test condition	HM50256 (Cerdip)				HM4864AP (Plastic)				Remarks
		Sam- ples	Total component hours	Fail- ures	Failure rate* (1/hr)	Sam- ples	Total component hours	Fail- ures	Failure rate* (1/hr)	
High-temperature pulse operation	$150^\circ\text{C}/8\text{V}$	525	1.02×10^5	10^{*1}	1.13×10^{-3}	500	1.00×10^4	1^{*4}	2.02×10^{-4}	*1-3 Oxide Failure x 17, Foreign material x 1 *4 Oxide Failure x 1
	$150^\circ\text{C}/7\text{V}$	448	0.81×10^4	4^{*2}	6.47×10^{-4}	69	0.35×10^4	0	2.63×10^{-4}	
	$125^\circ\text{C}/8\text{V}$	336	0.67×10^4	4^{*3}	7.82×10^{-4}	300	0.60×10^4	0	1.53×10^{-4}	
	$125^\circ\text{C}/7\text{V}$	2834	0.95×10^4	0	9.68×10^{-1}	429	1.04×10^4	0	8.85×10^{-4}	
High-temperature Pressure cooker	85°C 85% RH 5.5V $121^\circ\text{C}/100\%$ RH	160	0.36×10^5	0	2.56×10^{-4}	650	1.23×10^4	0	7.48×10^{-7}	
		—	—	—	—	100	5.00×10^4	0	1.84×10^{-5}	

* Confidence level 60%.

● Table 6. Reliability Data on 64K and 128K EPROM

Test item	Test condition	HM6264P (Plastic)				HM616P (Plastic)				Remarks
		Sam- ples	Total component hours	Fail- ures	Failure rate* (1/hr)	Sam- ples	Total component hours	Fail- ures	Failure rate* (1/hr)	
High- temperature pulse operation	150°C/7V	100	0.10×10 ⁵	1*1	2.02×10 ⁻⁵	—	—	—	—	*1-3 Foreign material *2 PSG failure x 1 *4 Other x 1 *5 failure x 2
	125°C/8V	162	0.20×10 ⁴	2*2	1.55×10 ⁻⁵	—	—	—	—	
	125°C/7V	1014	1.16×10 ⁴	2*3	2.67×10 ⁻⁴	—	—	—	—	
	125°C/5.5V	—	—	—	—	9940	2.28×10 ⁴	2*4	1.36×10 ⁻⁴	
High- temperature Pressure cooker	85°C/85% RH 7V	304	0.30×10 ⁴	0	3.07×10 ⁻⁴	1430	2.35×10 ⁴	4*5	2.23×10 ⁻⁴	*5 AK x 2 Passiva- tion x 2
	121°C/ 100% RH	55	2.20×10 ⁴	0	4.18×10 ⁻⁵	250	4.40×10 ⁴	0	2.09×10 ⁻⁵	

* Confidence level 60%.

2.2.2 Reliability Test Data on ERROM

EPROM has two types; the conventional EPROM with transparent window and the one time programmable ROM (OTPROM). The latter is packaged in

plastic package. The reliability test data on the representative EPROM types of 64K EPROM (HN482764, HN482764P), 128K EPROM (HN4727128) are shown in Table 7.

● Table 7 Reliability Data on 64K and 128K EPROM

Test item	Test condition	HN482764 (Cerdip/Plastic)				HN4827128 (Cerdic)				Remarks
		Sam- ples	Total component hours	Fail- ures	Failure rate* (1/hr)	Sam- ples	Total component hours	Fail- ures	Failure rate* (1/hr)	
High-temp. pulse operation	125°C/5.5V	131	0.43×10 ⁴	0	2.14×10 ⁻⁴	100	0.10×10 ⁻⁶	0	9.20×10 ⁻⁶	*1 Data dissipa- tion x 38
	125°C/7V	760	0.61×10 ⁵	0	1.51×10 ⁻⁴	—	—	—	—	
High- temperature Storage	200°C	117	1.17×10 ⁵	1*1	1.73×10 ⁻⁵	80	0.40×10 ⁵	0	2.30×10 ⁻⁵	Data of 64K OTP
	250°C	106	1.06×10 ⁵	5*1	5.94×10 ⁻⁴	65	0.33×10 ⁵	1*1	6.12×10 ⁻⁵	
	300°C	67	0.67×10 ⁵	25*1	3.73×10 ⁻⁴	50	0.25×10 ⁵	6*1	2.93×10 ⁻⁴	
High- temperature Pressure cooker	85°C/85% RH 5V	200	0.20×10 ⁴	0	4.60×10 ⁻⁴	—	—	—	—	Data of 64K OTP
	121°C/ 100% RH	78	0.16×10 ²	0	5.75×10 ⁻⁵	—	—	—	—	

* Confidence level 60%.

The failure in table 7 is due to the data dissipation in memory cells. Getting thermal energy, electrons in memory cells are activated and go through the floating gate. In actual usage, however, it has no problem because this phenomenon depends on temperature (about 1.0eV of activated energy) greatly. The moisture resistance of OTPROM is also satisfactory.

The example of PROM derating are shown in Table 8. When users apply the derating, the parameter is generally only the temperature because IC memories are specified the operating condition. Especially to lower the junction temperature during mounting is important to stabilize operation on access time, refresh time and other characteristics.

● Table 8 Example of EPROM Derating

Factor	Temperature	
Failure criteria	Electrical Characteristics, Function Test	
Failure mechanism	Increase of leak current and others	
Summary The result from high temperature baking of PROM is shown in the right figure.		
Note:	Decreasing junction temperature shown in the figure will promise the higher reliability the junction temperature can be calculated by a formula: $T_j = T_a + \theta_{ja} \cdot P_d$. θ_{ja} is about 100°C/W with no air flow and about 60 to 70°C/W with 2.5 m/s air flow.	

2.2.3 Reliability Data on MASK ROM

The reliability test data on 256K and 1M bit MASK ROM are shown in Table 9. MASK ROM is pat-

terned according to ROM information in manufacturing process, so has no problem of data dissipation in high temperature like EPROM and EEPROM.

● Table 9 Reliability Data on 256K and 1M MASK ROM

Test item	Test condition	HN613256P (Plastic)				HN62301P (Plastic)				Remarks
		Samples	Total component hours	Failures	Failure rate* (1/hr)	Samples	Total component hours	Failures	Failure rate* (1/hr)	
High-temp. pulse operation	125°C/5.5V	90	0.9×10 ⁵	0	1.02×10 ⁻⁵	—	—	—	—	
	125°C/7V	50	0.5×10 ⁵	0	1.84×10 ⁻⁵	246	2.46×10 ⁵	0	3.74×10 ⁻⁴	
High-temperature	85°C/85% RH 5V	120	1.2×10 ⁵	0	7.67×10 ⁻⁵	120	1.20×10 ⁵	0	7.67×10 ⁻⁴	
Pressure cooker	121°C/100% RH	80	0.8×10 ⁴	0	1.15×10 ⁻⁴	78	1.56×10 ⁴	0	5.90×10 ⁻⁴	

* Confidence level 60%.

2.2.4 Reliability Data on MOS Memory (The result of environment test)

Examples of each environment test data are shown in Table 10. They show good results without any failure even in severe environment.

V_{TH} of MOS transistor is one of the basic process

parameters in MOS memory, which has almost no change using surface stabilization technology and clean process. Table 2 shows the examples of time changes for 256K DRAM; V_{cc} min. (V_{min}) and access time (t_{RAC}) in high temperature pulse test.

● Table 10 Reliability Data on MOS Memories

Test item	Test condition	HM5026 (Cerdip)		EPROM (Cerdip)		HM4864AP (Plastic)		HM6264P (Plastic)		LCC		Remarks
		Samples	Failure	Samples	Failures	Samples	Failures	Samples	Failures	Samples	Failures	
Temperature cycling	-55°C~150°C 10 cycle	1486	0	775	0	887	0	3315	0	860	0	
Temperature cycling	-55°C~150°C 1000 cycle	316	0	250	0	277	0	150	0	445	0	
Thermal shock	-65°C~150°C 15 cycle	145	0	146	0	38	0	76	0	498	0	
Soldering heat	260°C, 10	50	0	90	0	38	0	76	0	82	0	
	1,500G, 0.5ms	38	0	90	0	—	—	—	—	82	0	
Variable frequency	20~2,000Hz 20G	38	0	90	0	—	—	—	—	82	0	
Constant-acceleration	20,000G	38	0	90	0*	—	—	—	—	82	0	*6,000G

2.3 Change of Electrical Characteristics on IC Memory

The degradation of I_{CBO} and h_{FE} are the main factors of degradation in inner cell transistor of bipolar memory. In actual element designing, how-

ever, it is designed to operate in the range at which no degradation happen. Therefore no change of characteristics including access time are observed. Time dependence in access time for HM10470 are shown in Fig. 1.

Fig. 1 Time Dependence in Access Time for HM10470

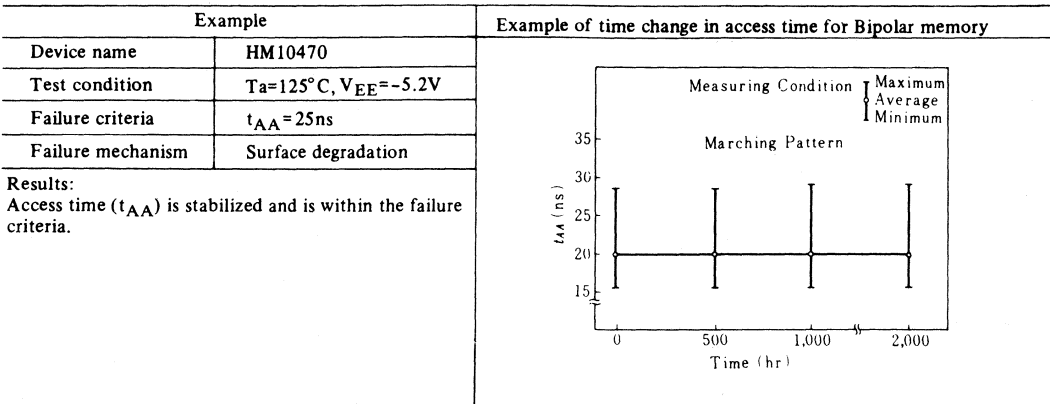
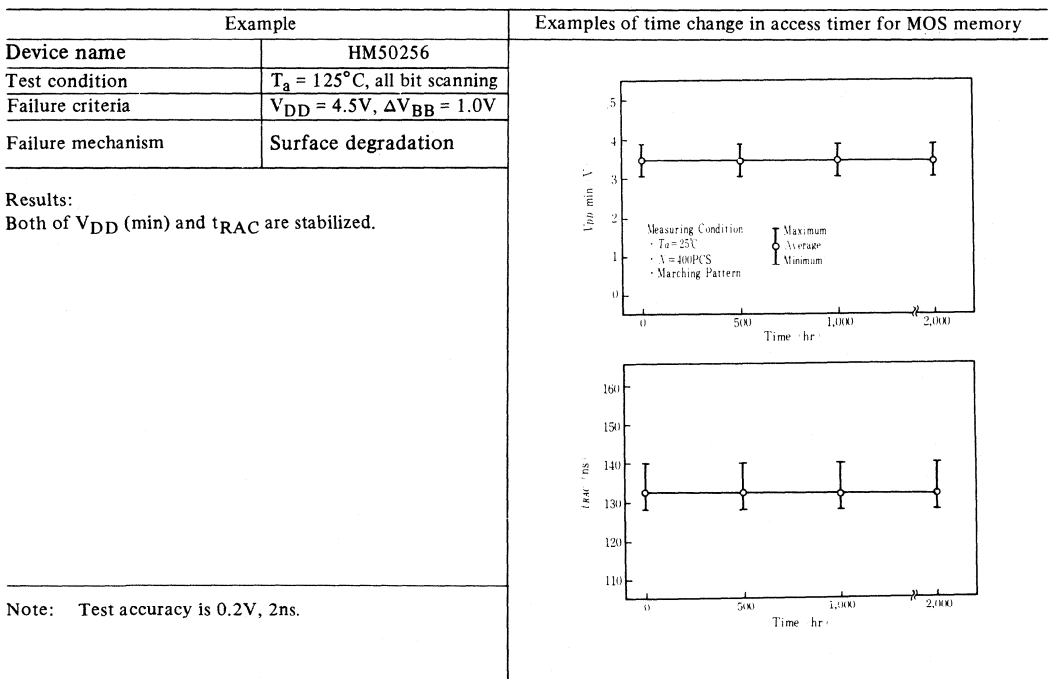


Fig. 2 Time Dependence in $V_{DD\ min}$ and t_{RAC} for HM50256



2.4 Failure Mode Rate

Examples of failure mode happened in users' application are shown in Figure 3 and 4. Since IC memories require the finest pattern process of semiconductor technology, the percentage of fail-

ures, such as pinholes, defects on photoresist and foreign materials, tends to increase. To eliminate the defects in the manufacturing process, Hitachi has improved the process and performed 100%

burn-in screening under high temperature. Hitachi has been collecting and checking customers' process-data and marketing data for higher reliability of our

products. To analyze them is very helpful for the improvement of designing and manufacturing.

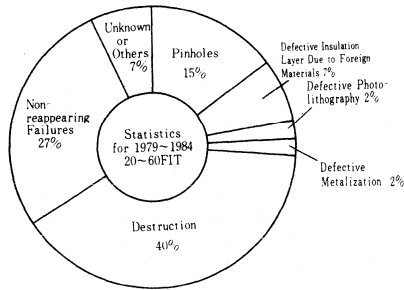


Fig. 3 Failure Mode Rate of Bipolar Memory

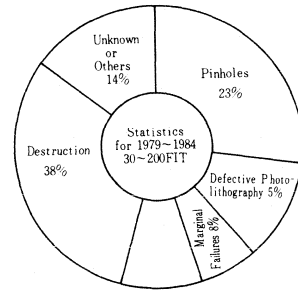


Fig. 4 Failure Mode Rate of MOS Memory

3. SOFT ERROR

3.1 Soft Error Mechanism

As mentioned before, IC memories have been highly integrated. By integration, the chip size is reduced and also signal level on the chip and storage charge of dynamic memories is reduced. An obstacle of integration is soft error. Soft error is a transitory failure which can be recovered by reprogramming. It is caused by α -particles emitted from U and TH contained in the package materials. As memory chips are irradiated by α -particles, a great deal of electron-hole pairs are induced in Si substrate. These induced electrons reverse the data in memory cell.

Fig. 5 shows the mechanism of soft error by α -particle. In case of NMOS dynamic memory, positive holes are drawn to substrate because negative voltage is applied to the Si substrate, so, the data is reversed only by electrons (from data "1" to "0")

Fig. 5 shows the soft error in memory cell mode. This soft error is defined as "Memory cell mode" distinguished from "Bit line mode".

Soft error in "Bit line mode" is shown in Fig. 6. As the data is read out on bit line, bit line potential changes according to the data in memory cell. As this changed level is very small (about 100 mV), it is amplified by sense amplifier compared with the

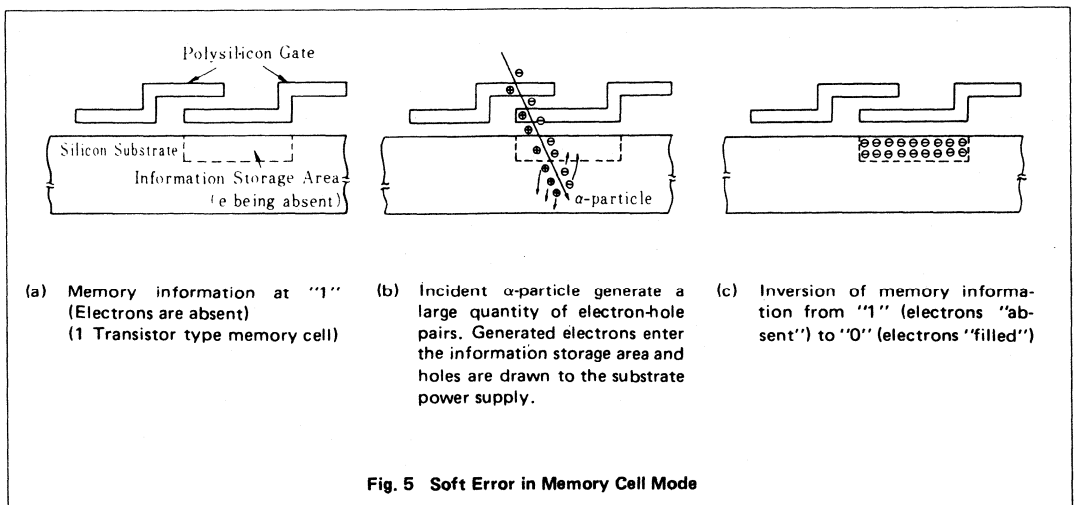
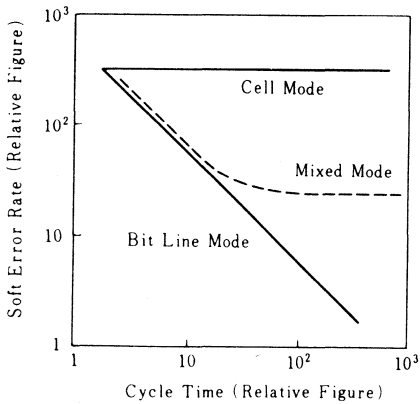
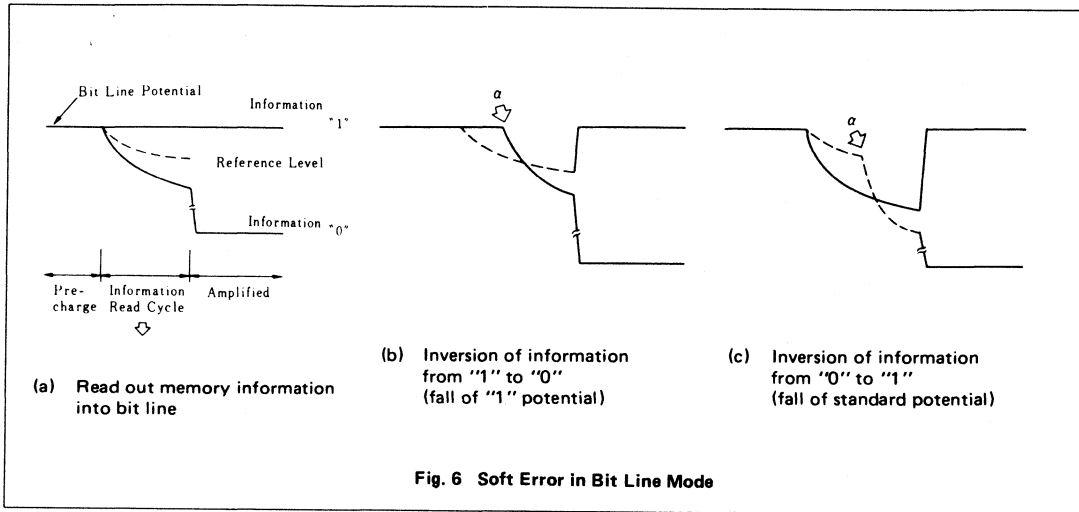


Fig. 5 Soft Error in Memory Cell Mode



3.2 Prevention against Soft Error in Products

The soft error rate of initial 64K DRAM was beyond the expected rate. Therefore Hitachi has prevented against soft error as follows.

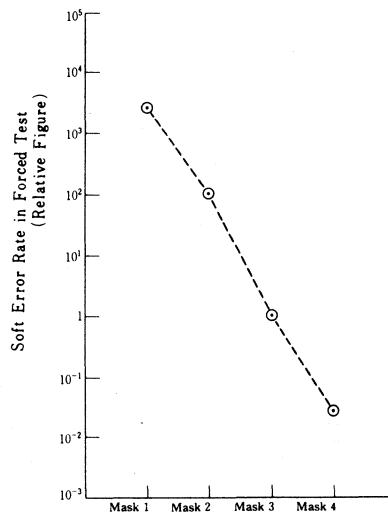
- 1) Use of package materials which emit less number of α -particles
- 2) Application of chip coating technology to prevent the α -particle
- 3) Improvement of circuitry and layout technology with α -particle immunity

As the result of these preventions, the soft error rate

reference potential (potential read out from dummy cell). If bit line is irradiated by α -particle in this short cycle of read out to amplification, bit line potential decreases. In case that bit line potential becomes less than reference potential, soft error (data "1" to "0") will be occurred. On the other hand, with decrease of reference potential, soft error (data "0" to "1") will be occurred. Both are defined as the soft error in "Bit line mode" because the errors are occurred by the α -particle irradiation to bit line.

Fig. 7 shows the soft error rate depending on cycle time.

In actual products, the soft errors are occurred in three different modes; Memory cell mode, Bit line mode and a mixture of both modes.



of 64K DRAM has attained the acceptable level. Figure 8 shows a development of the soft error rate of 64K DRAM. Chip coating was applied for mask 1 and 2, however, according to the improved technology, it is not required for mask 3 and 4. The improved technology in 64K DRAM has also applied to 256K SRAM and attained the high level.

3.3 Request for Prevention against Soft Error in System Equipment

System reliability can be improved more by supplying some function, that is, ECC device for large-scale memory system and parity bit for small-scale one.

4. RELIABILITY CLASSIFICATION

In designing IC memories, Hitachi classifies memory reliability according to their application and controls the flows of design, production and test. Reliability can be roughly classified as follows;

- 1) For large scale computers and electronic exchanges
- 2) For Important parts of auto-motive application
- 3) For general communication industry

Our products would be used effectively to consider the above-mentioned classification by its application.

Especially, for your special application, please consult our sales engineering staff.

■ PRECAUTIONS FOR HANDLING IC MEMORIES

A variety of IC memories such as large capacity dynamic memory, high speed bipolar memory and low power dissipation static CMOS memory have been developed and commercially available, which can be selected according to application. Precaution for handling IC memories will be given below to prevent the device from malfunctioning.

1. BIPOLAR MEMORY

1.1 Prevention of Static Electricity

Bipolar memories have been more affected by the static electricity than conventional type because their diffused layers have become thinner. Preventions against electrostatic discharge are as follows.

- (1) Keep all terminals of a device at the same potential, use conductive mat and tubes in transporting or storing them.
Hitachi usually uses the plastic tube coated with or made of conductive material, and in some cases, uses the conductive mat called "MOSPAK" for our shipment. Reused tubes should not be used.
- (2) Ground operator in handling memories for inspection or connection as shown in Fig. 1. Insert a 1M ohm resistor to protect operator against an electric shock.
- (3) Control the ambient relative humidity at about 50%.
- (4) Wear cotton clothes instead of the ones made of synthetic fabrics.
- (5) Ground tips of soldering iron, which is preferable the one operates at low voltage.
- (6) Pack with conductive mats in shipping IC memories mounted on the circuit board.

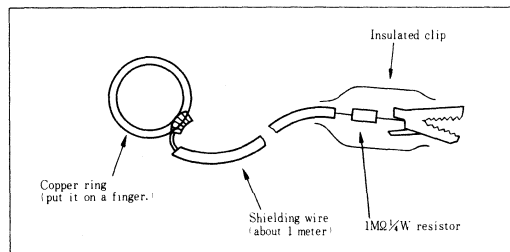


Fig. 1

1.2 Prevention of Reverse Insertion

Inserting ICs reversely may cause excess current to be flown and sometimes the devices to be damaged.

The device orientation is indicated on the package surface definitely.

1.3 Mounting and Removal of ICs with Power On

Usually rather high current flows in regulator of bipolar memory. Therefore, if ICs are mounted or removed from board with power on, the induced voltage may destroy the ICs. The device should be mounted on or removed from the board with power off. The same precaution is required in measuring ICs using tester.

1.4 Prevention of Oscillation

As ECL bipolar memory has a high transistor cut-off frequency, external circuit might cause oscillation which brings ICs into misoperation. So, the capacity of about 0.1 μF with high frequency characteristics is recommended to put between ICs and voltage supply line.

1.5 Precaution on Simple "H" Level of ECL Memory

In some cases, the input of ICs is directly connected to ground to set input as "H" level. However, it sometimes causes misoperation in conjunction with internal circuit conjunction with internal circuit composition. "H" and "L" level of input are specified as $V_{IL}(\text{min})$ and $V_{IH}(\text{max})$ respectively. Please utilize ICs properly according to its specification.

1.6 Cooling

Power dissipation of bipolar memory is 400 mW to 1000 mW per chip. In the case that many bipolar

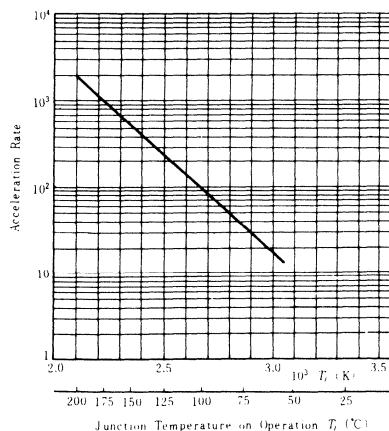


Fig. 2 Derating of ECL Memory

memories are mounted on a board, it is difficult to cool the device sufficiently in natural air flow. Therefore, the forced-air cooling at higher than 2.5 m/s is required. Then, reliability will be improved as shown in Fig. 2.

We recommend the junction temperature to be kept less than 85°C in high reliability use.

1.7 Other Precaution

(1) Deforming of Shipping Tube and Carrier

Since the plastic tube and carrier for shipment (for ECL flat package) are usually made of thermo-plastic, they are deformed at the temperature of higher than 40 to 50°C.

If the device is subjected to the burn-in by users, please use the aluminum tube or other metal fixtures.

- (2) Glass sealed package is easily damaged by the shock, however, it is not so seriously damaged by normal handling or the drop test (JIS C7021A-8) on individual one. In case of receiving strong shock during transportation or loading of devices packed in the tube, they are damaged. So please take care not to drop the tube packed the device in transporting and loading on/off. In addition after mounting on board, the device may be damaged if the board strength is not strong enough, or the board receives the strong deforming stress. Please be careful the board strength and handling of the board mounting ICs.

2. MOS MEMORY

2.1 Prevention against Static Electricity

MOS IC memory requires the same caution for handling as bipolar memory against static electricity as described in 1.1.

2.2 Prevention against Power Supply Noise

As for the dynamic memory, power supply current is different greatly between in operation (access time) and in non-operation (stand-by time). It is effective to reduce the power dissipation, however, it may cause the spike noise on the supply current. To supply the enough current during refresh, it is recommended to insert the large capacitor (ex. a 10 μ F capacitor for every 9 pieces of 64K-bit of HM4864) as well as an 0.1 μ F high-frequency capacitor for each device. In addition, it is very important to reduce the impedance in circuits on designing.

2.3 Evaluation of Memory System Design

The power margin curve (shmoo curve) is available for evaluating the memory system design (timing margin or adaptability to the peripheral circuits). Investigating the variable V_{DD} and access time, the device with the closer curve to its margin is judged to be better.

2.4 Parity Bit

Application of MOS IC static memory especially to microcomputers has been rapidly increasing due to the advantages that it operates by a single 5V supply and refreshing is not required.

In some cases, IC memory is designed as all bits are information bits and no parity bit. Is is, however, desirable to add parity bits to detect the memory errors.

2.5 Use under High Electric Field

In case MOS IC memories are placed near to high voltage source, the high electric field may cause failures in system operation.

To avoid the failure, shield the ICs from the high voltage source.

1. VIEWS ON QUALITY AND RELIABILITY

Hitachi basic views on quality are to meet individual users' purpose and their required quality level and also to maintain the satisfied level for general application. Hitachi has made efforts to assure the standardized reliability of our IC memories in actual usage. To meet users' requests and to cover expanding application, Hitachi performs the followings;

- (1) Establish the reliability in design at the stage of new product development.
- (2) Establish the quality at all steps in manufacturing process.
- (3) Intensify the inspection and the assurance of reliability of products.
- (4) Improve the product quality based on marketing data.

Furthermore, to get higher quality and reliability, we cooperate with our research laboratories.

With the views and methods mentioned above, Hitachi makes the best efforts to meet the users' requirements.

2. RELIABILITY DESIGN OF SEMICONDUCTOR DEVICES

2.1 Reliability Target

Establishment of reliability target is important in manufacturing and marketing as well as function and price. It is not practical to determine the reliability target based on the failure rate at a single common test condition. So, the reliability target is determined based on many factors such as each characteristics of equipment, reliability target of system, derating applied in design, operating condition and maintenance.

2.2 Reliability Design

Timely study and execution are essential to achieve the reliability based on reliability targets. The main items are the design standardization, device design including process and structural design, design review and reliability test.

- (1) Design Standardization

Design standardization needs establishing design rules and standardizing parts, material, and process. When design rules are established on circuit, cell, and layout design, critical items about quality and reliability should be examined. Therefore, in using standardized process or material, even newly developed products would have high reliability, with the excep-

tion of special requirement on function.

- (2) Device Design

It is important for device design to consider total balance of process design, structure design, circuit and layout design. Especially in case of applying new process or new material, we deeply study the technology prior to development of the device.

- (3) Reliability Test by Test Site

Test site is sometimes called Test Pattern. It is useful method for evaluating reliability of designing and processing ICs with complicated functions.

1. Purposes of Test Site are as follows;

- Making clear about fundamental failure mode;
- Analysis of relation between failure mode and manufacturing process condition.
- Analysis of failure mechanism.
- Establishment of QC point in manufacturing.

2. Effects of evaluation by Test Site are as follows;

- Common fundamental failure mode and failure mechanism in devices can be evaluated.
- Factors dominating failure mode can be picked up, and compared with the process having been experienced in field.
- Able to analyze relation between failure causes and manufacturing factors.
- Easy to run tests.

2.3 Design Review

Design review is a method to confirm systematically whether or not design satisfies the performance required including by users, follows the specified ways, and whether or not the technical items accumulated in test data and application data are effectively applied.

In addition, from the standpoint of competition with other products, the major purpose of design review is to insure quality and reliability of the product. In Hitachi, design review is performed in designing new products and also in changing products.

The followings are the items to consider at design review.

- (1) Describe the products based on specified design documents.
- (2) Considering the documents from the standpoint of each participant, plan and execute the sub-program such as calculation, experiments and investigation if unclear matter is found.
- (3) Determine the contents and methods of reliability test based on design document and drawing.

- (4) Check process ability of manufacturing line to achieve design goal.
- (5) Arrange the preparation for production.
- (6) Plan and execute the sub-programs of design changes proposed by individual specialists, for tests, experiments and calculation to confirm the design change.
- (7) Refer to the past failure experiences with similar devices, confirm the prevention against them, and plan and execute the test program for confirmation of them.

In Hitachi, these study and decision at design review are made using the individual check lists according to its objects.

3. QUALITY ASSURANCE SYSTEM OF SEMICONDUCTOR DEVICES

3.1 Activity of Quality Assurance

The following items are the general views of overall quality assurance in Hitachi;

- (1) Problems is solved in each process so that even the potential failure factors will be removed at final stage of production.
- (2) Feedback of information is made to insure satisfied level of process ability.

As the result, we assure the reliability.

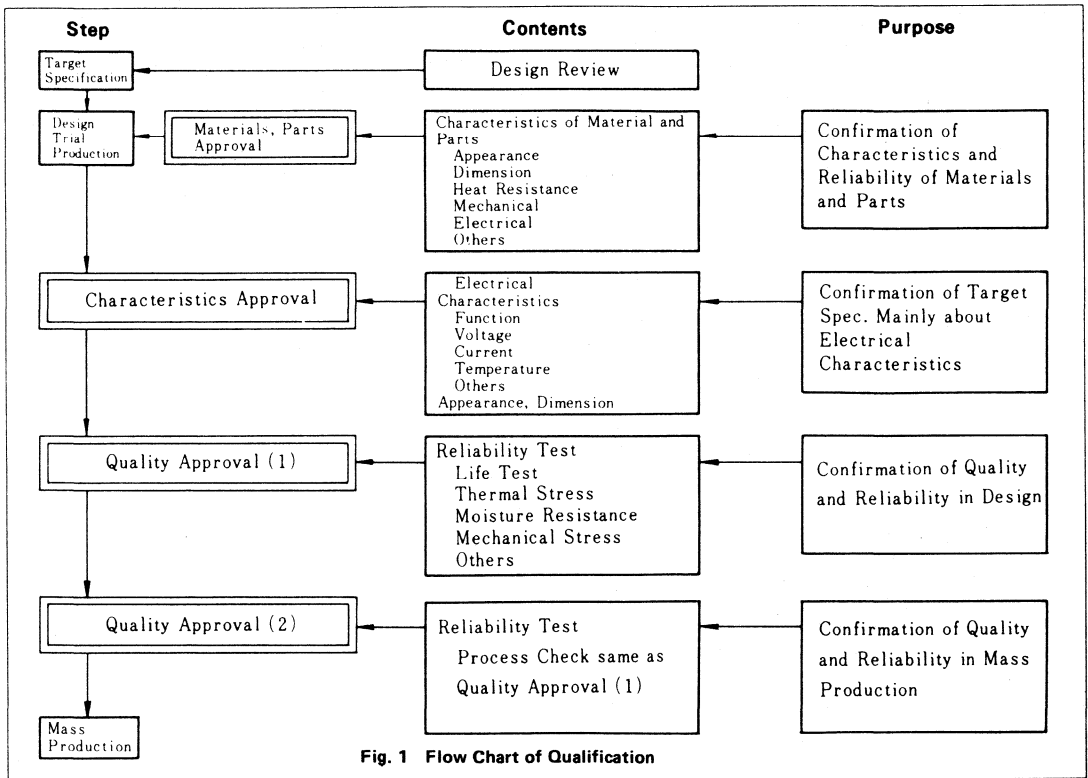


Fig. 1 Flow Chart of Qualification

3.2 Qualification

To assure the quality and reliability, the qualification tests are done at each stage of trial production and mass production based on the reliability design described at section 2.

The followings are the views on qualification in Hitachi:

- (1) From the standpoint of customers, quality the products objectively by a third party.
- (2) Consider the failure experiences and data from

customers.

- (3) Qualify every change in design and work.
- (4) Qualify intensively on parts and materials and process.
- (5) Considering the process ability and factor of manufacturing fluctuation, establish the control points in mass production.

Considering the views mentioned above, qualification shown in Fig. 1 is done.

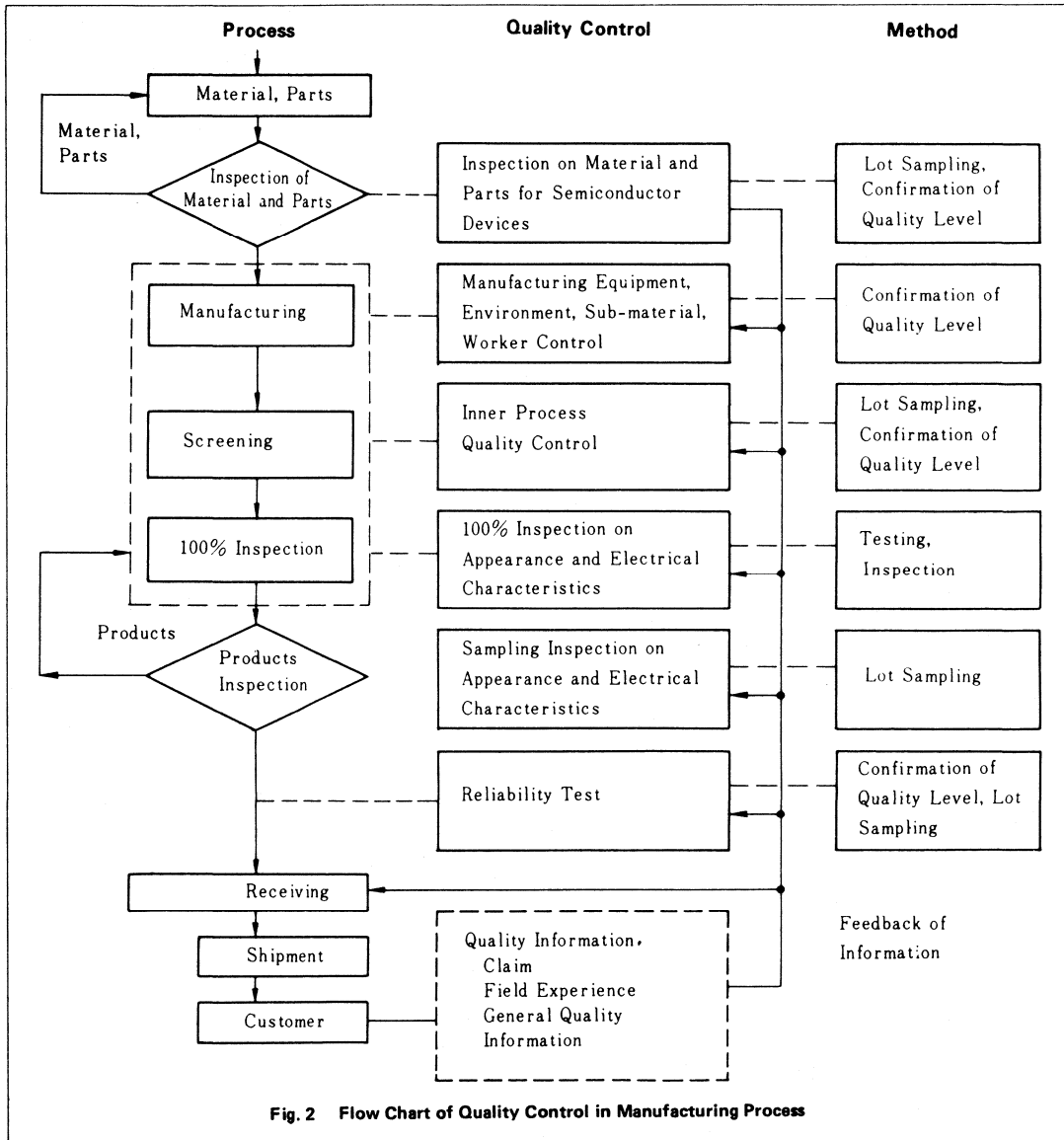


Fig. 2 Flow Chart of Quality Control in Manufacturing Process

3.3 Quality and Reliability Control in Mass Production

To assure quality in mass production, quality is controlled functionally by each department, mainly by manufacturing department and quality assurance department. The total function flow is shown in Fig. 2.

3.3.1 Quality Control on Parts and Materials

With the tendency toward higher performance and higher reliability of devices, quality control of parts and materials becomes more important. The items such as crystal, lead frame, fine wire for wire bonding, package and materials required in manufacturing process like mask pattern and chemicals, are all subject to inspection and control.

Besides qualification of parts and materials stated in 3.2, quality control of parts and materials is defined in incoming inspection. Incoming inspection is performed based on its purchase specification, drawing and mainly sampling test based on MIL-STD-105D. The other activities for quality assurance are as follows.

● **Table 1. Quality Control Check Points of Parts and Material (example)**

Material, Parts	Important Control Items	Point for Check
Wafer	Appearance	Damage and Contamination on Surface
	Dimension Sheet Resistance Defect Density Crystal Axis	Flatness Resistance Defect Numbers
Mask	Appearance	Defect Numbers, Scratch
	Dimension Resistoration Gradation	Dimension Level Uniformity of Gradation
Fine Wire for Wire Bonding	Appearance	Contamination, Scratch, Bend, Twist
	Dimension Purity Elongation Ratio	Purity Level Mechanical Strength
Frame	Appearance	Contamination, Scratch
	Dimension Processing Accuracy Plating Mounting Characteristics	Dimension Level Bondability, Solderability Heat Resistance
Ceramic Package	Appearance	Contamination, Scratch
	Dimension Leak Resistance Plating Mounting Characteristics Electrical Characteristics Mechanical Strength	Dimension Level Airtightness Bondability, Solderability Heat Resistance Mechanical Strength
Plastic	Composition	Characteristics of Plastic Material
	Electrical Characteristics Thermal Characteristics Molding Performance Mounting Characteristics	Molding Performance Mounting Characteristics

(1) Technology Meeting with Vendors

(2) Approval and Guidance of Vendors

(3) Analysis and tests of physical chemistry.

The typical check points of parts and materials are shown in Table 1.

3.3.2 Inner Process Quality Control

To control inner process quality is very significant for quality assurance of devices. The quality control of products in every stage of production is explained below. Fig. 3 shows inner process quality control.

(1) Quality Control of Products in Every Stage of Production

Potential failure factors of devices should be removed in manufacturing process. Therefore, check points are set up in each process so as not to move the products with failure factors to the next process. Especially, for high reliability devices, manufacturing lines are rigidly selected in order to control the quality in process. Additionally we perform rigid check per process or per lot, 100% inspection in proper processes so as to remove failure factors caused by manufacturing fluctuation, and screenings depending on high temperature aging or temperature cycling. Contents of controlling quality under processing are as follows:

- Control of conditions of equipment and workers and sampling test of uncompleted products.
- Proposal and execution of working improvement.
- Education of workers
- Maintenance and improvement of yield
- Picking up of quality problems and execution of countermeasures toward them.
- Communication of quality information.

(2) Quality Control of Manufacturing Facilities and Measuring Equipment

Manufacturing facilities have been developed as the need of higher devices in performance and the automated production. It is also important to determine quality and reliability.

In Hitachi, automated manufacturing is promoted to avoid manufacturing fluctuation, and the operation of high performance equipment is controlled to function properly.

As for maintenance inspection for quality control, daily and periodically inspections are performed based on specification on every check point.

As for adjustment and maintenance of measuring equipment, the past data and specifications are clearly checked to keep and improve quality.

(3) Quality Control of Manufacturing Circumstances and Sub-material.

Quality and reliability of devices are affected especially by manufacturing process. Therefore, we thoroughly control the manufacturing circumstances such as temperature, humidity, dust, and the sub-materials like gas or pure water used in manufacturing process.

Dust control is essential to realize higher integration and higher reliability of devices. To maintain and improve the clearness of manufacturing site, we take care buildings, facilities, air-conditioning system, materials, clothes and works. Moreover, we periodically check on floating dust in the air, fallen dust or dirtiness on floor.

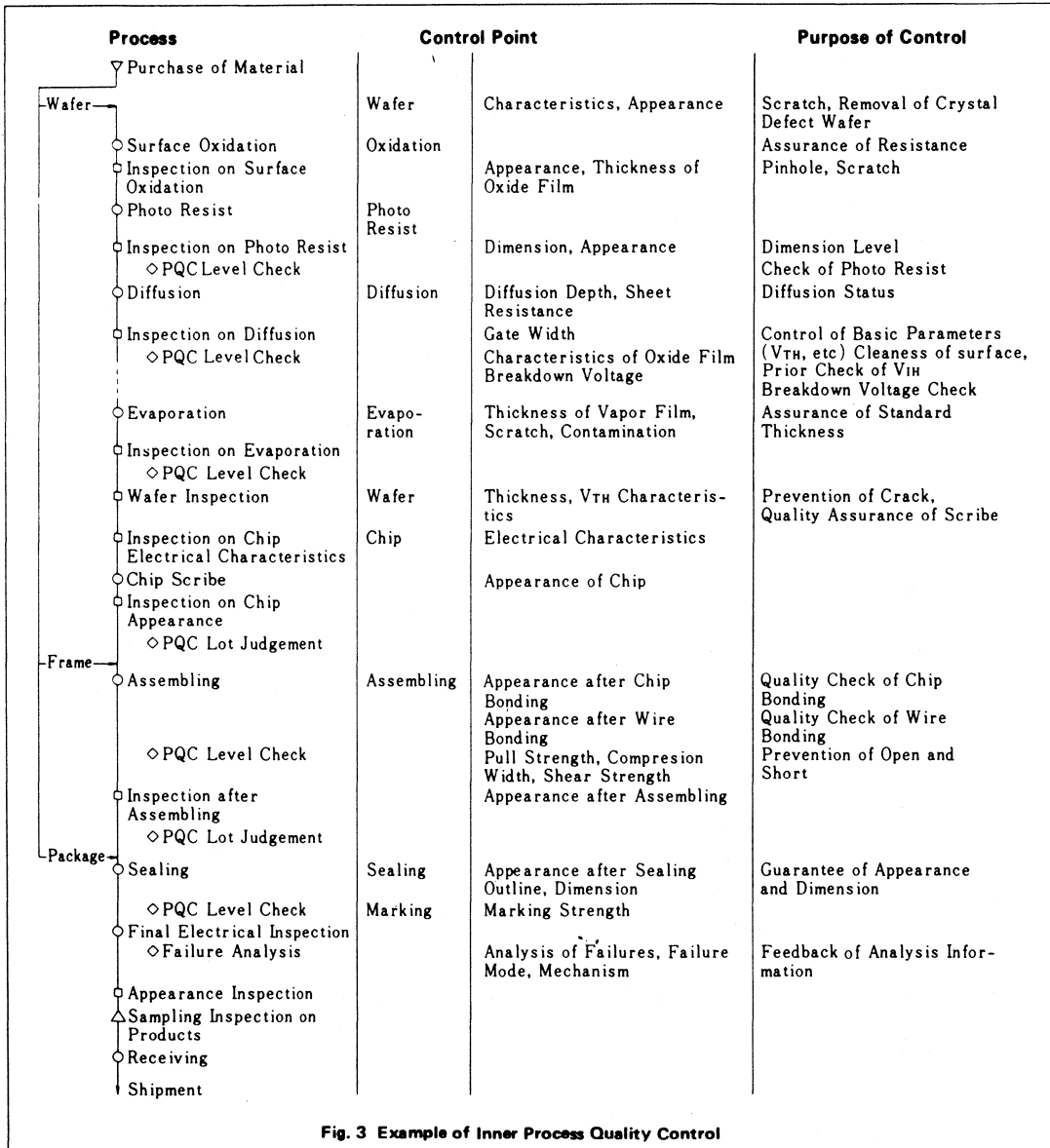


Fig. 3 Example of Inner Process Quality Control

3.3.3 Final Tests and Reliability Assurance

(1) Final Tests

Lot inspection is done by quality assurance department for the product passed in 100% test in final manufacturing process. Though 100% of passed products is expected, sampling inspection is subjected to prevent mixture of failed products by mistake.

The inspection is executed not only to confirm that the products meet users' requirement, but to consider potential factors. Our lot inspection is based on MIL-STD-105D.

(2) Reliability Assurance Tests

To assure reliability, the reliability tests are performed periodically, and performed on each manufacturing lot if user requires.

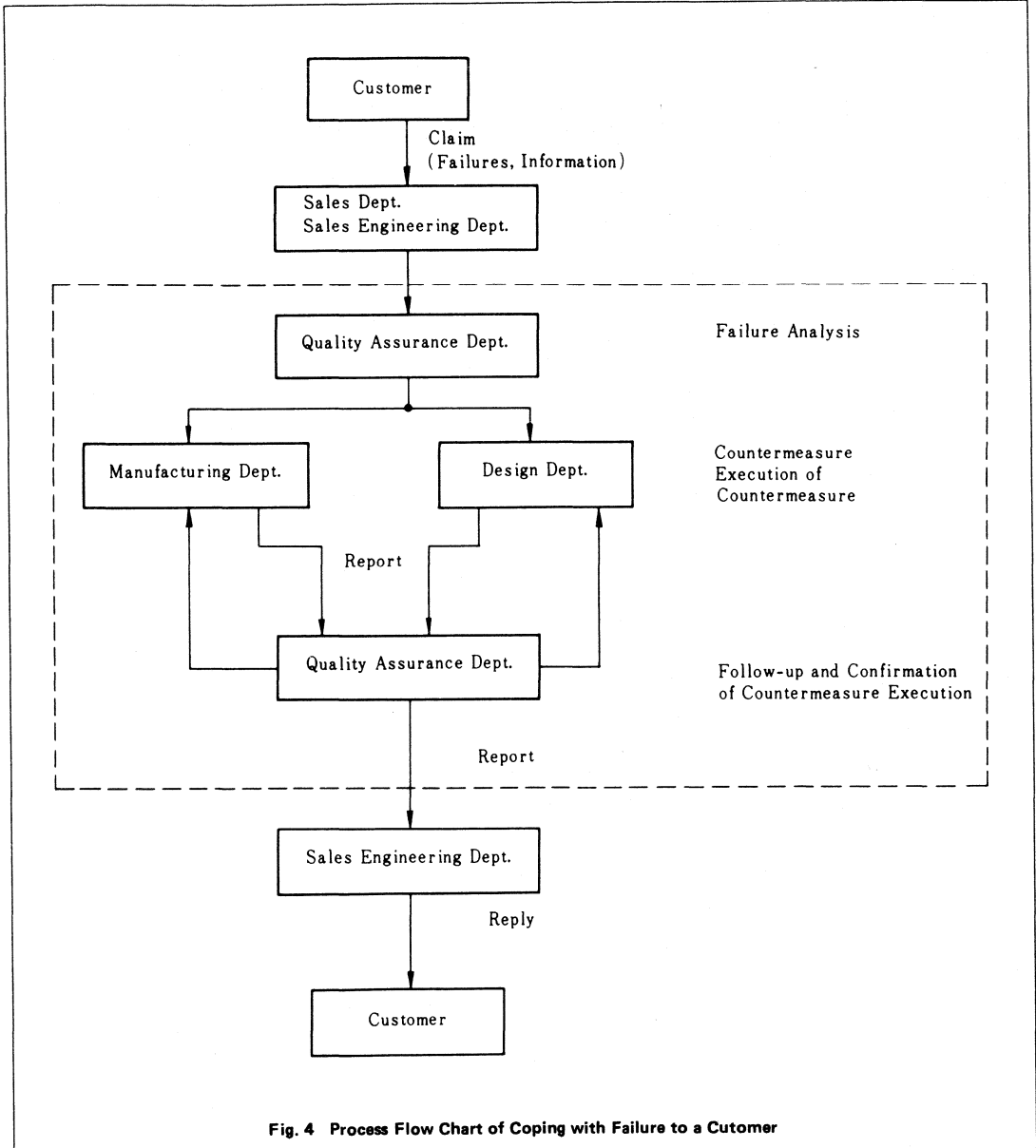


Fig. 4 Process Flow Chart of Coping with Failure to a Customer

1. INSPECTION METHOD

Compared to conventional core memories, IC memories contain all peripheral circuits, such as the decoder circuit, write circuit and read circuit. As a result, assembly and electrical inspection of ICs are all performed by IC manufactures. Consequently, as the electrical inspection of IC memories are becoming more systematic, conventional IC inspection facilities are becoming useless. This has led to the development and introduction of a memory tester with pattern generator to generate the inspection pattern of the memory IC at high speed. A function test for such as TTL gates can be performed even by a simple DC parameter facility. However, when the address input becomes multiplexed as in 16K, 64K and 256K memory, even the generation of the function test pattern becomes a serious problem.

In the memory IC inspection, its quality cannot be judged by DC test at external pins only, because the number of the element such as transistor which can be judged in the DC test is only 1/1000 of all elements. The followings are the address patterns proposed to inspect whether the internal circuits are functioning correctly.

- (1) All "Low", All "High"
- (2) Checker Flag
- (3) Stripe Pattern
- (4) Marching Pattern
- (5) Galloping
- (6) Waling
- (7) Ping-Pong

Those are not all, but only representative ones. There are the pattern to check the mutual interference of bits and the pattern for the maximum power dissipation. Among the above mentioned patterns, those of (1) to (4) are called N pattern, which can check one sequence of N bit IC memory with the several times of N patterns at most. Those of (5) to (7) are called N² pattern, which need several times of N² patterns to check one sequence of N bit IC memory. Serious problem arises in using N² pattern in a large-capacity memory. For example, inspection of 16K memory with galloping pattern takes a lot of time — about 30 minutes. (1), (2) and (3) are rather simple and good methods, however, they are not perfect to find any failure in decoder circuits. Marching is the most simple and necessary pattern to check the function of IC memories.

2. MARCHING PATTERN

The marching pattern, as its name indicates, is a pattern in which "1"s march into all bits of "0"s. For example, a simple addressing of 16 bit memory is described below.

- (1) Clear all bits See Fig. 1 (a)
- (2) Read "0" from 0th address and check that the read data is "0". Hereafter, "Read" means "checking and judging data"
- (3) Write "1" on 0th address. See Fig. 1(b)
- (4) Read "0" from 1st address.
- (5) Write "1" on 1st address.
- (6) Read "0" from nth address.
- (7) Write "1" on nth address See Fig. 1(c)
- (8) Repeat (6) to (7) to the last address. Finally, all data will be "1".
- (9) After all data become "1", repeat from (2) to (8) replacing "0" and "1".

In this method, 5N address patterns are necessary for the N-bit memory.

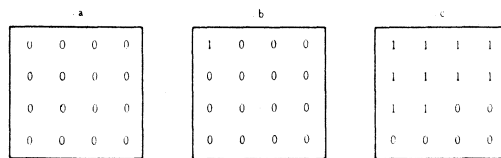


Fig. 1 Addressing method of for 16 bit memory in the Marching pattern

3. GENERATION OF MARCHING PATTERN

The simple method of generating the marching pattern and displaying failure bits of the memory on the braun tube will be introduced. Fig. 2 shows the block diagram. The address pattern is generated using four synchronous 4 bit counters. Fig. 4 shows the entire pulse relations. This example is for 16K bit memory and shows that A14, which has a half frequency of A13, is the same as the data inputs. A15 signal, together with the carrier signal of HD74161, is used to determine the termination of the sequence.

As shown in Fig. 2, in the read and write cycles after clearing all bits, addressing is twice the period of clearing. This switching is performed at the binary gate, following the reference pulse generating circuit. Output of HD74161 is input to D/A converter and input to the oscilloscope as an analogue signal of X-Y matrix. The output of the comparator circuit is input to the Z axis and performed lumi-

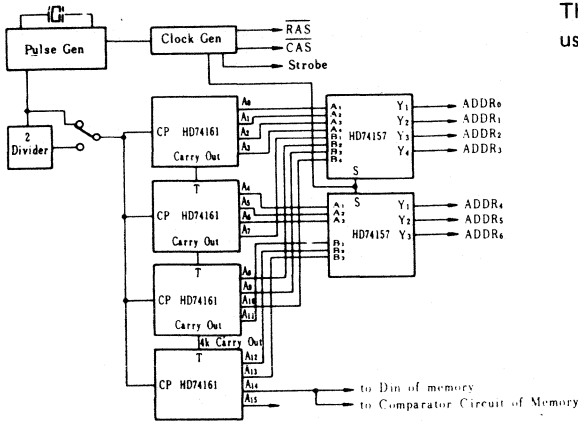


Fig. 2 Marching Pattern Generating Circuit

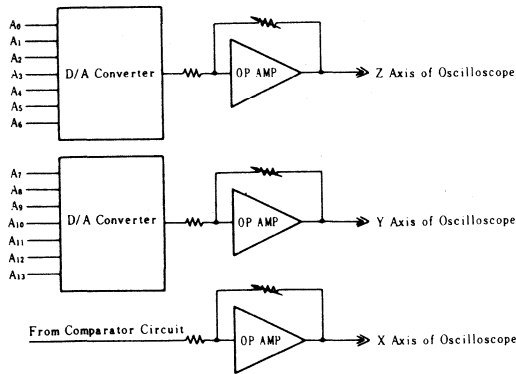


Fig. 3 Fail Bit Map Display Circuit

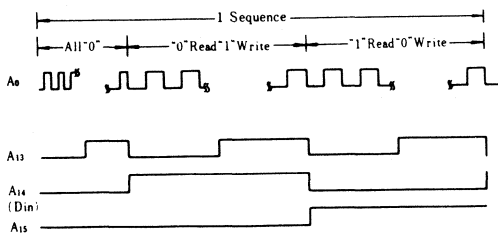
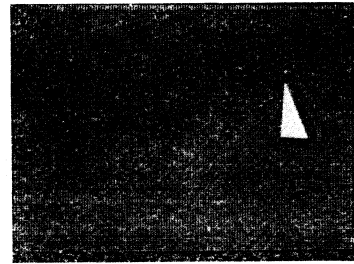
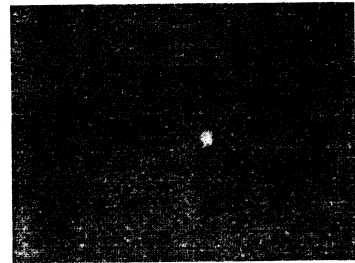


Fig. 4 Entire Pulse Relation

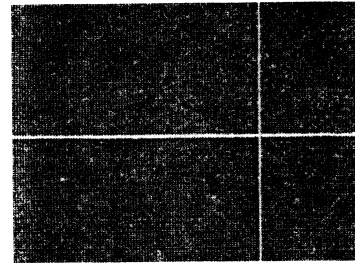
Therefore, the fail bit map as shown in Fig. 5 is very useful for observing the operation of IC memories.



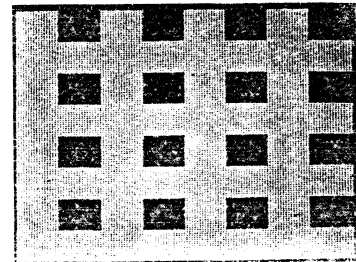
(A)



(B)



(C)



(D)

Fig. 5 Example of 1 bit Solid Failure

nous intensity modulation. In this way, the fail bit map is displayed on the CRT. Compared with others like TTL, the operation of IC memories is too complicated to understand only by pulse waveform observed with an ordinary oscilloscope.

4. FAILURE MODE

Generally, 70% – 90% of failures at users are called solid failures. This failure mode has no relation with access time, voltage margin or timing. In this mode, a certain specified bit is stuck in "0" or "1". The simple methods previously mentioned is useful to detect such failures. Therefore, high-precision measurements such as those performed in memory IC manufactures are not necessary except any special cases.

Hitachi performs 100% inspection on the worst conditions for devices so as to guarantee sufficient operations under all power voltage conditions and timing conditions specified.

An extremely accurate memory tester is necessary to perform high-precision inspection considering 1ns accuracy. Hitachi has been developing testers to supply excellent memory ICs in characteristics and quality to users, and establishing the system capable of developing further high-efficiency memory ICs.

APPLICATION OF DYNAMIC RAMS

1. Power On

After turning on power to set the memory circuitry, hold for more than 500 μ s and apply eight or more dummy loads before actuating the memory. The dynamic cycle may be either an ordinary memory cycle or a refresh cycle.

2. Operation Modes (See Fig. 1)

(1) Read Cycle:

First, decide the X address of the memory cell chosen and start with trailing of RAS. When the X address has been held by the internal circuitry, change it to Y address. Then, trail $\overline{\text{CAS}}$ to take in the Y address. If the $\overline{\text{WE}}$ pin is at high level, output will appear on the Dout pin after a certain time.

(2) Write Cycle:

The input at Din is written in the memory cell when $\overline{\text{WE}}$ turns to low before $\overline{\text{CAS}}$.

(3) Read/Modify/Write Cycle:

During this cycle, $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ are trailed down to low, so that data is read out from and written in the same address in the same memory cycle.

(4) Page Mode Cycle:

In this cycle; $\overline{\text{CAS}}$ is cyclically moved, after taking in the X address through RAS, to scan only the Y address. This permits reading out and writing in only one column data at high speed.

2. Data Output

Dout is a TTL-compatible three-state output with two TTL-load fan outs. The output is controlled by the $\overline{\text{CAS}}$ signals; it is held while $\overline{\text{CAS}}$ is low, while Dout returns to a floating state when $\overline{\text{CAS}}$ is high. In the early write cycle, the output reaches high-impedance to permit the use as a common I/O terminal.

3. Refresh

Refresh is a process of periodical rewriting to make up for the leakage of the charge accumulated in the memory cell. This operation is implemented in the $\overline{\text{RAS}}$ only refresh cycle, ordinary read cycle, and so on. In 16k and 64k bit memories, all bits can be refreshed by a 128-cycle scanning to only the X addresses from A0 to A6. In 256k bit memories, refresh is performed by 256-cycle scanning to X addresses from A0 to A7. Especially, the $\overline{\text{RAS}}$ only refresh cycle permits such a power-efficient refresh as calls for only approximately 75 percent of the current consumed by the read cycle. With $\overline{\text{CAS}}$ fixed at high level, the output is in high-impedance. There are two methods of refresh: concentrated and deconcentrated refresh. The former gives a concentrated 128-cycle or 250-cycle refresh after operating the memory for a period of 2ms or 4ms maximum. In contrast, the latter repeats a refresh cycle every 16 μ s following the initial 16 μ s (=2ms/128 or =4ms/256) memory operation. A choice between the two modes calls for a careful consideration about the system's efficiency.

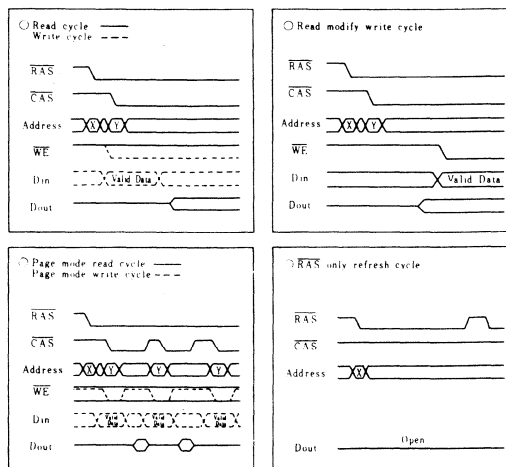


Fig. 1 Operating modes of Dynamic RAMs

4. Operating Current of Dynamic RAMs

Fig. 2 shows the waveforms of the current applied in various operating modes. The mean operating current in each mode equals the value obtained by dividing the integrated result of each waveform by the cycle time. The first peak current in each operating mode appears as a result of the circuit operation during the memory access time. On the other hand, the peak current during standby appear as a result of the precharging operation in each circuit. Having two circuitry operation modes -X and Y. Dynamic RAMs show different peak currents depending upon the operating timing of $\overline{\text{RAS}}$ and $\overline{\text{CAS}}$. That is, the greatest peak current appears when both X and Y circuits operate simultaneously. The current consumed while the memory stands by on the board is expressed in terms of the cycle time dependency shown in Fig. 3.

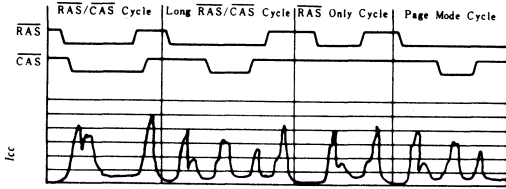


Fig. 2 Power supply voltage Wave form

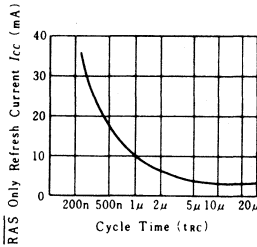


Fig. 3 Cycle time dependence of RAS only refresh current

5. Noise

Broadly, noise can be classified into power source noise and input signal noise. The power source noise can be further classed into low-frequency noise and high-frequency noise as shown in Fig. 4. To assure a stable memory operation, the peak-to-peak power supply voltage in the presence of low- or high-frequency noise should be held below 10 percent of its standard level. To prevent the power source noise, it is recommended to provide a condenser of 0.1 μ F or so to each one or two devices. Input signal noise can be classified overshoot or undershoot. The undershoot should be held below the highest input level specified. To prevent input-undershoot-induced parasitic transistor effects, a -5V V_{BB} is provided to the three-way power source or a built-in V_{BB} bias circuit is included on chip. Normally, design should be such that the input undershoot does not exceed the minimum value specified for V_{IL} , at worst. Overshoot and undershoot can be reduced by inserting a damping resistance of several tens of ohms in Dynamic RAM series.

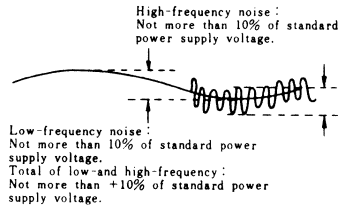


Fig. 4 Power source noise

PROGRAMMING & ERASING OF EPROMS

1. PROGRAMMING & ERASING OF EPROM

1.1 Programming

Data is programmed into the memory cell of an EPROM by applying a high voltage to its drain and gate (Fig. 1 and 2). The high voltage at the drain increases the energy of the electrons in the channel area. When the energy becomes high enough, the electrons become what are known as "hot electrons" that are capable of jumping across the oxide film. Pulled by the high voltage at the gate, the hot electrons are admitted into the floating gate. The electric charge entering the floating gate changes the threshold voltage in the memory element, whereby it is stored as new information. When reading out, voltage is applied as shown in Fig. 3, and "1" and "0" are identified by checking whether or not current flows. Since the drain voltage for read-out is set at about 3V, no erroneous writing takes place. When shipped, all bits of the EPROM are held at logic "1" with all electric charge released (with no data in). In changing the logic 1 to logic 0 through the application of the specified waveform and voltage, the necessary information is programmed in. The higher the V_{pp} voltage and the longer the program pulse width t_{pw} , the more the quantity of electrons can be programmed in, as shown in Fig. 4. If the V_{pp} exceeds the rated value, such as by overshoot, the p-n junction of the memory may yield to permanent breakdown. To avoid this, check V_{pp} overshoot by the PROM programmer. Also, check negative-voltage-induced noise at other terminals, which can create a parasitic transistor effect and apparently reduce the yield voltage. Hitachi's EPROMs are usually capable of being written and erased more than 100 times.

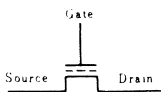


Fig. 1 Memory transistor circuit symbols

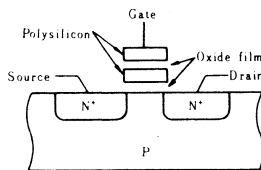


Fig. 2 Cross section of memory transistor

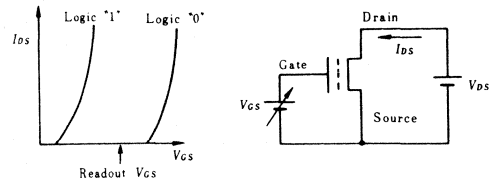


Fig. 3 Reading out stored information

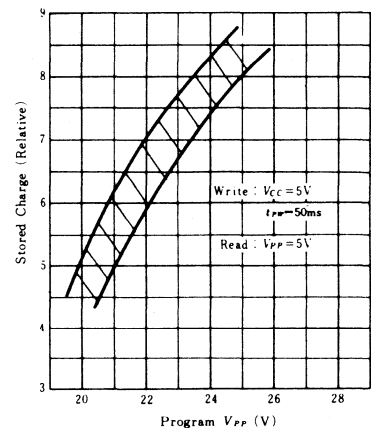
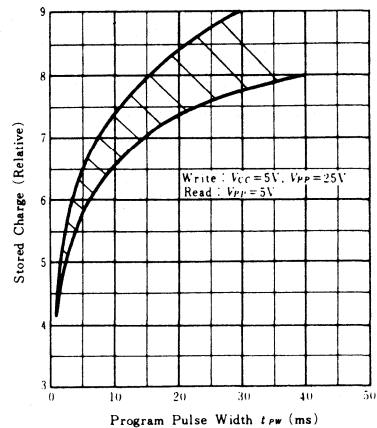


Fig. 4 Typical Programming Characteristics of EPROMs.

1.2 Erasing

Data stored in the EPROM is erased by releasing the electric charge from the floating gate through the exposure of the memory chip to ultraviolet light. Light has an energy that is inversely proportional to its wavelength. Receiving the energy of the ultraviolet light, the electrons in the floating gate are again turned into hot electrons, which jump across the oxide film into the control gate or substrate. As a result of this process, the stored information is erased. Accordingly, the stored information can not be erased by such lights whose wavelengths are too long to give adequate energy to jump over the barrier of the oxide film. For successful erasing, the wavelength and minimum exposure rate of ultraviolet light are specified as 2,537Å and 15W sec/cm² respectively. This condition is attained by exposing a device to an ultraviolet lamp of 12,000μW/cm² 1.2 ~ 3cm away for approximately 20 minutes. The ultraviolet light transmission rate of the transparent lid is about 70 percent. Any contamination or foreign material at the surface of the capsule lowers the transmission rate, prolonging the erasing time. So such contamination should be recovered by use of alcohol or other solvent that does not damage the package. Fig. 5 shows typical erasure characteristics for EPROM.

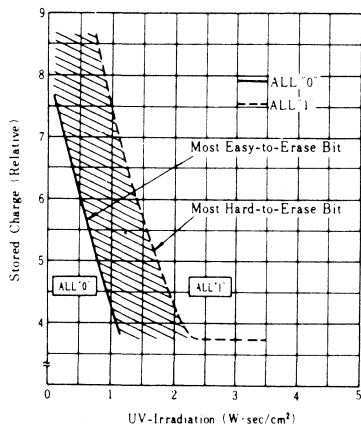


Fig. 5 Typical Erasing Characteristics

1.3 Data retention characteristic of EPROM

As a result of writing in, approximately 0.5 to 2.0 x 10⁻¹³ coulomb of electrons are accumulated at the floating gate. With the elapse of time, however, these electrons decrease, as a result of which the inversion of stored information can happen. The mechanism of electron dissipation is generally explained as follow:

(1) Data dissipation by heat

The accumulation of electrons at the floating gate is an unbalanced state, so the dissipation of thermally excited electron is unavoidable. Therefore, the data retention time has a close relationship with temperature. Fig. 6 shows typical data retention characteristics. The data retention time is proportional to the reciprocal of absolute temperature.

(2) Data dissipation by ultraviolet light

Ultraviolet rays at a wavelength of not greater than 3,000 ~ 4,000Å is capable of releasing the electric charge stored in the memory of the EPROM with varying efficiencies. Fluorescent light and sunlight contain some ultraviolet rays, so prolonged exposure to these lights can cause data corruption as a result of electric charge dissipation. Fig. 7 shows examples of the data retention time under an ultraviolet eraser, sunlight and fluorescent lighting. But it should be noted that the data for fluorescent light and sunlight are not definite because of their varying ultraviolet ray contents. The ultraviolet ray content in sunlight, for example, varies greatly with seasons, weather and the composition of the atmosphere.

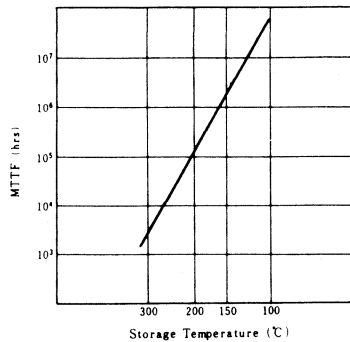


Fig. 6 Typical Data Retention Characteristics

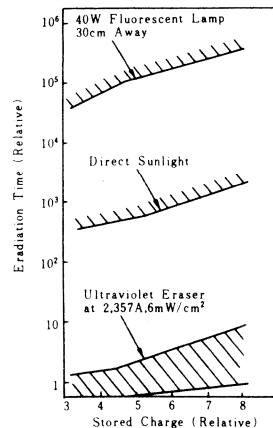


Fig. 7 EPROM's data retention time

(3) Data dissipation by voltage

This type of data dissipation occurs while information is being written in. At other memory cells lying on the same word line or data line as the memory cell being programmed, high voltage can cause the dissipation of stored electric charge. Of course, such defects are removed at the factory by pre-shipment inspection. The programming voltage and pulse width should be always kept within the specified range for the same reason.

1.4 Application of OTPROM

One time electrically programmable ROM (OTPROM) has two kinds of packages: standard Dual In-line Package (DIP) and Small Outline Package (SOP). And it features only one time programming because it has no window through which ultraviolet light exposes; testings of programming and erasure cannot be performed after assembled. So, in Hitachi, we perform screening test for programming, access time, and data retention on wafers at proving test.

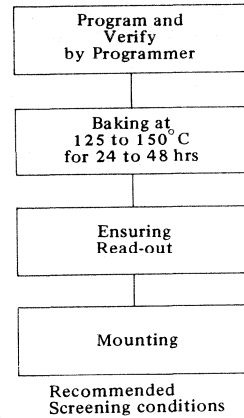
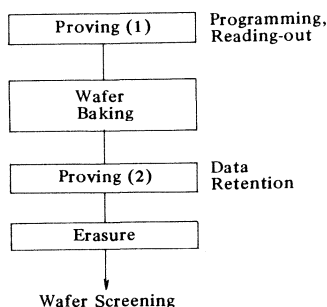
However, defects rarely occurred in assembly process cannot be completely removed in final test screening which can perform only reading test.

Therefore, we would recommend users to perform high temperature baking after programming devices in order to ensure high reliability so as not to be inferior to EPROMs.

Detailed conditions and procedures for the screening are shown in the right. First, please program and verify devices by programmer, then, leave them without bias at 125 to 150°C for 24 to 48 hours.

After that, please ensure the function of reading-out and remove the data retention failures.

From the results of devices in which the recommended screening test is properly performed, we would confirm that the data retention characteristics of OTPROMs are equal to general EPROMs.



1.5 EPROM Programmer

The 16K EPROM Programmer stores the program in its internal RAM and writes the program in the EPROM. For this programming, the minimum of 3 functions are necessary: blank check function prior to programming, programming function and the verify function after programming. As shown in the right chart, there are another programmers provided with a reverse insertion checking function or pin contact checking function prior to the blank check. The outline of each block is as follows.

(a) Pin contact check

In the connection test of the ROM pin and the socket, normally checking is performed by detecting the forward current of each EPROM pin. Care is necessary as this forward biased resistance differs according to products of each company.

(b) Reverse insertion check

This check detects the reverse insertion of the device, places the equipment in reset mode and protects the device and equipment.

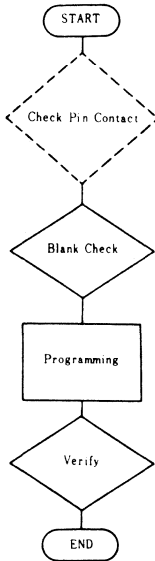
(c) Blank check

This check is performed before programming and checks whether or not it is an erased EPROM, or for preventing EPROM reprogramming. Since the output data in the erased condition are "1" (high level), check whether or not data in EPROM are all "1". It will fail-stop even when 1 bit is "0" (low level). Normally, it is designed to provide warning with a lamp or buzzer.

(d) Programming

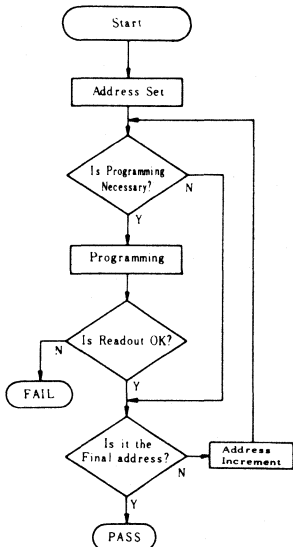
The function of programming the data in the internal RAM of the programmer into EPROM and will fail-stop when programming cannot be made. The normal flow is as shown below. The EPROM data will be read out prior to pro-

gramming and compared with programming data. If they coincide, programming will be skipped and if they differ, programming will be performed. Then, read out will be made again and compared with the programming data, and if they coincide, it will progress to the next address.



(e) Verify

This function is for checking after programming completion whether or not the programming is correct when comparing with the data in the internal RAM of the programmer and it performs fail-stop when it does not coincide. Normally, when it fails, together with lighting of the fail lamp, the address and data are displayed.



(f) How to input the program

There are the following methods for inputting the program data to the internal RAM of the programmer. Normally, paper tape input and teletypewriter input are options.

Method	Content
Copy input	Input by copying the master ROM.
Manual input	Input by the keyswitch of the front panel. Used for correction or revision of program
Paper tape input	Read the paper tape furnished from the host system with the tape reader
Teletypewriter input	Input with the teletypewriter. Preparation, correction and list preparation of the program can be made.

1.6 Maker Identifier Code

Programming condition of EPROM is various according to EPROM manufacturers and device types. It may cause miss operation. To countermeasure it, some EPROMs provide maker identifier code. Users can write EPROM by reading out write condition coded before shipped. Some commercial programmers set write condition by recognizing this code. This function enables effective program.

Following programming condition is; ① program voltage, ② program timing, ③ high speed programming algorithm, ④ pin configuration. EPROM has maker identifier code area besides memory access area, as shown in Fig. 2.32.

Table 2.7 describes how to utilize maker identifier code. Setting A9 at 12V and A1 – A8, A10 – A13 at V_{IL} access to maker identifier code area and O₀ – O₇ output programming condition code with V_{IL} or V_{IH} of A₀.

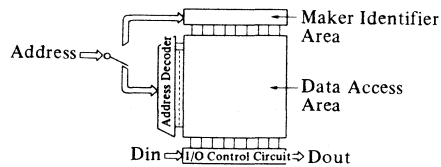


Fig. 2.32

Table 2.7

Maker code	Hitachi	A ₉	O ₀	O ₁	O ₂	O ₃	O ₄	O ₅	O ₆	O ₇	Hex Data
R	HN27128A	V _{IL}	0	0	0	0	0	1	1	0	1 0 D
O	HN27256		0	0	0	1	0	0	0	0	1 0
M	HN27C256	V _{IH}	1	0	1	1	0	0	0	0	3 0
	HN27512		1	0	0	1	0	1	0	0	9 4
	HN27C101		0	0	1	1	1	0	0	0	3 8
	HN27C301		1	0	1	1	1	0	0	1	B 9

A₉ - 12V
A₁ - A₈, A₁₀ - A₁₃, V_I
A₁₄, A₁₅ - Don't care

1.7 Handling EPROM

Contact with a charged human body or rubbed with plastics or dry cloth, the glass window of an EPROM generates static electricity which causes device malfunctions. Typical malfunctions are faulty blanking and write margin setting that give a wrong impression that information has been correctly written in. As already reported at the international conferences concerning the reliability of LSI chips, this is due to the prolonged retention of electric charge (resulting from the static electricity) on the glass window. Such malfunctions can be eliminated by neutralizing the charges through the irradiation of ultraviolet rays for a short time. It is recommended to execute reprogramming after this irradiation since it reduces the electric charges in the floating gate, too. The basic countermeasure is to prevent the charging of the window, which can be achieved by the following methods as in the prevention of common static breakdown of ICs.

- (1) Ground operator to handle EPROM. Avoid the use of things such as gloves that may generate static electricity.
- (2) Refrain from rubbing the glass window with plastics or other materials that may generate static electricity.
- (3) Avoid the use of coolant sprays which contain some ions.
- (4) Use shielding labels (especially those containing conductive substances) that can evenly distribute the established charge.

1.8 Shielding label

When using an EPROM in an environment where ultraviolet exposure can occur, it is advisable to put a shielding label on its glass window to absorb ultraviolet light. Specially prepared shielding labels are marketed. Metal-loaded labels are particularly effective. In choosing a shielding label, the following points should be carefully checked.

(1) Adhesiveness (mechanical strength)

Avoid repeated attaching and dusting that may reduce the adhesive strength. Ultraviolet erasing and reprogramming are recommended after stripping off an attached label. (When the need arises to change a label, it is advisable to put a new one on the old one since peeling may develop a static charge.)

(2) Temperature range

Use the shielding label in an environment whose temperature falls within the specified allowable temperature range. Beyond the specified temperature range, the paste on the label may harden or stick too fast. When it hardens, the label may be peeled off easily. When it sticks too fast, the paste may remain on the window glass even after the label has been removed.

(3) Damp-proofness

Use the shielding label in an environment whose humidity falls within the specified allowable humidity range. Today there are few shielding labels that can meet all environmental requirements established for the EPROM. So a suitable one must be chosen for each specific application.

■ MASK ROM PROGRAMMING INSTRUCTION

The writing of the custom program code into mask ROMs is performed by the CAD system, using a large-sized computer. ROM code data should conform to specifications given below, using either paper tape, EPROM, or magnetic tape. Additional instructions, such as chip select and customers' part number, should be given in the "ROM Specification Identification Sheet".

1. Specification of EPROM

- (1) Submit the three sets of the EPROM stored Data. Specify the address of the EPROM in the case of two or four EPROMs.
- (2) The ROM Code data is input from the start address to Final Address in the EPROM.
- (3) Type of EPROM
 HN482764 (8K-word x 8-bit, 2764 Compatible)
 HN4827128 (16-K word x 8-bit, 27128 Compatible)
 HN27256 (32K-word x 8-bit, 27256 Compatible)
 HN27C256 (32K-word x 8-bit, 27C256 Compatible)

2. Specification of Magnetic Tape

2.1 Use the following type of magnetic type which can be entered in a magnetic tape device compatible with the IBM magnetic tape device.

- (1) Length 2,400 feet, 1,200 feet or 600 feet
- (2) Width 1/2 inch
- (3) Channel 9 channels
- (4) Bit density 800 BPI or 1,600 BPI (Clearly state which it is in the "ROM Specification Identification Sheet".)

2.2 Use the EBCDIC code as the use code.

2.3 Follow the format of the magnetic tape as described below

- (1) No leading tape mark
- (2) No label
- (3) Record size 80 byte/1 record
- (4) Block size 10 records/1 block
- (5) The end of the file should be indicated by 2 successive tape marks (TM).

2.4 Data Mode

2.4.1 HMCS6800 Load Module Mode

This mode is the object mode output from the assembler of HMCS6800.

- (1) Divide the 8 bit code into the upper and lower 4 bit codes, and convert each into hexadecimal notation.

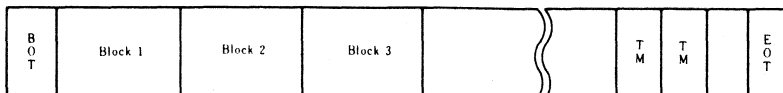
(Example) The code of 1100 0110 is as follows under binary notation.

(Upper 4 bits)	(Lower 4 bits)	Bit weight
D ₇ D ₆ D ₅ D ₄	D ₃ D ₂ D ₁ D ₀	(ROM output
1 1 0 0	0 1 1 0	equivalence)

- (2) The actual load module mode is shown as follows:

	Header record	
Record Start	5 3	S
Record Type	3 0	0
Byte Count	3 0	0 6
	3 6	
Address Size	3 0	0000
	3 0	
	3 0	
	3 0	
Data	3 4	48-H
	3 8	
Data	3 4	44-D
	3 4	
Data	3 5	52-R
	3 2	
Check Sum	3 1	1B (Check Sum)
	4 2	

Data record		End of file record	
5 3	S	5 3	S
3 1	1	3 9	9
3 1	1 6	3 0	0 3
3 6			
3 1	1100	3 0	0000
3 1			
3 0			
3 0			
3 9	9 8	4 6	FC (Check Sum)
3 8		4 3	
3 0	0 2		
3 2			
4 1	A8 (Check Sum)		
3 8			



S0 indicates the head of the file and S9 indicates the end of the file. The actual data enters following S1. It means that the data starts from the address (hexadecimal) indicated in the address size. The address of the address size of the data recorder is

compared with the next data recorder address by counting in increments of 1 byte of the data and checking whether it is sequential or not. The printed example of the HMCS6800 load module mode is as shown below.

Example

```

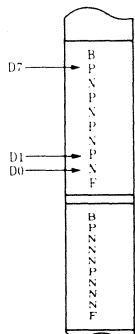
Header Record → S00B000058204558414D504CB5
Data Record   → S113F0007EF5587EF7897EFAA77EF9C07EF9C47E24
Data Record   → S112F010FA657EFA8B7EFAA07EF9DC7EFA247E06
End of
File Record   → S9030000FC
    
```

- (3) In case the address is skipped, perform entry into the "ROM Specification Identification Sheet" that the skipped address, and the data (00 or FF) entered into the skipped address by hexadecimal notation.

2.4.2 BNPF Mode

- (1) One word is symbolized by the word start mark B, the bit content represented by 8 characters of P and N, and the BNPF slice composed of successive 10 characters of the work end mark F.
- (2) The contents from F of one BNPF slice up to B of the next BNPF slice are ignored.
(Example) The code of AA by hexadecimal notation is symbolized as shown below.
- (3) It is necessary to designate the bit pattern (BNPF slice) on all ROM addresses. Therefore, the term of the ROM head address of "ROM Specification Identification Sheet" always becomes 0.
 B Indicates start of 1 word.
 N Indicates "0" of 1 bit data.
 P Indicates "1" of 1 bit data.
 F Indicates end or 1 word.

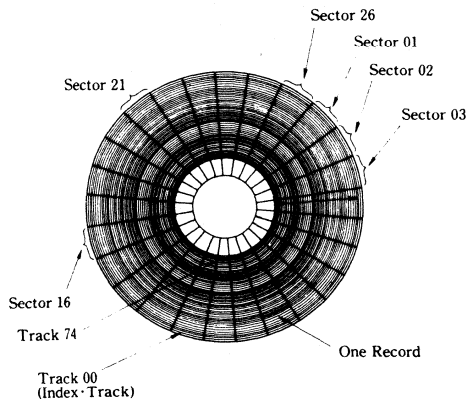
Example



3. Specification of Floppy Disk

3.1 Use the following type of Floppy Disk

- (1) Type . 8 Inch Single Sided and Single Density.
- (2) Number of Sector 26
- (3) Number of Track 77



3.2 Use the EBCDIC code as the use code.

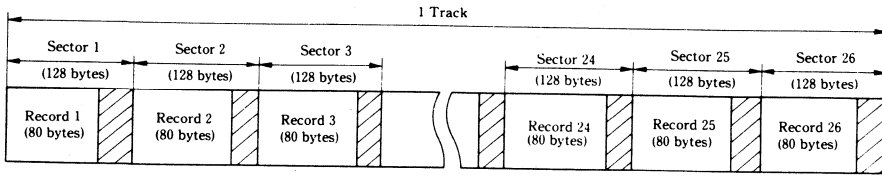
3.3 Make the format of the floppy disk as described below.

(1) Composition

No.	Item	Location	
		Track	Sector
1	Standard Volume Label	00	07
2	Standard Head Label	00	08 ~ 26
3	Data Area	01 ~ 73	01 ~ 26
4	Alternat Track	75, 76	01 ~ 26
5	Spare Track	00	01 ~ 06
		74	01 ~ 26

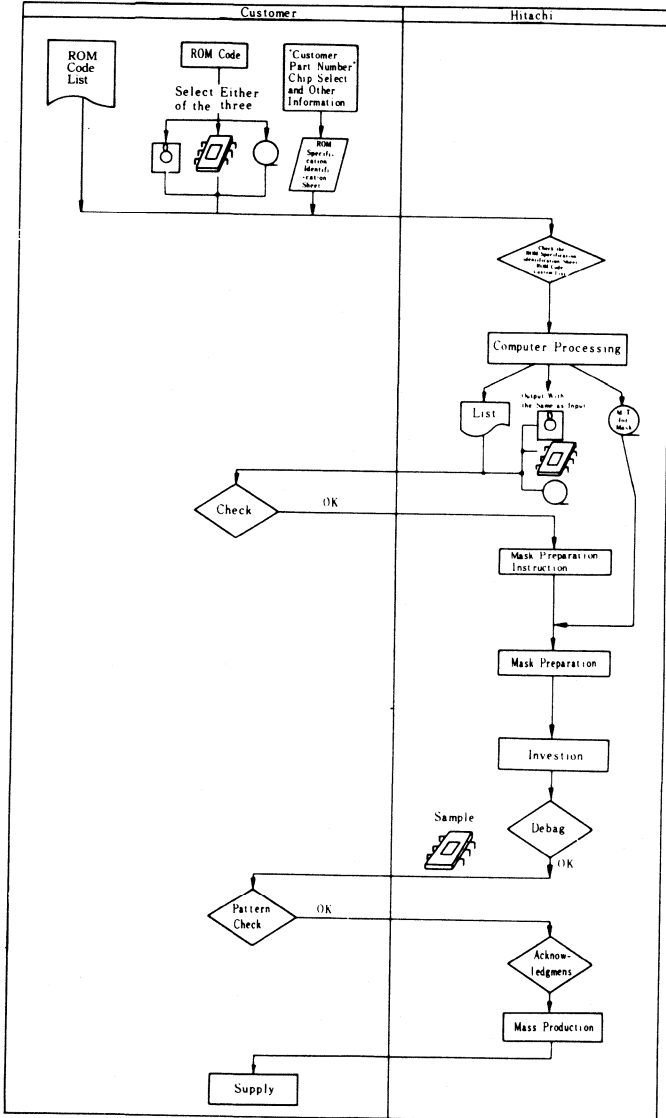
Mask ROM Programming Instruction

- (2) Record size 80 byte/1 record **3.4 Data Mode**
- (3) Use the sector as below. Use one sector for one record, that is 80 bytes out of 128 bytes used for one record. **See 2.4**



Mask ROM Development Flowchart

: unused



DATA SHEETS

MOS STATIC RAM

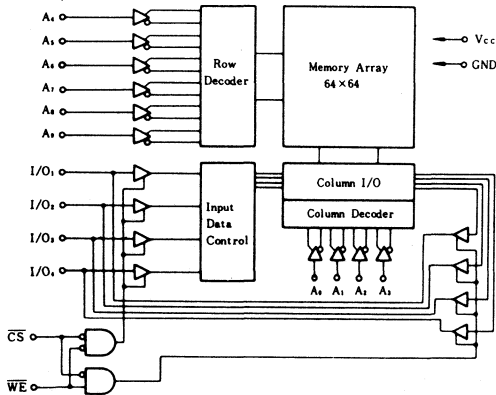
HM6148HP Series

1024-word x 4-bit High Speed Static CMOS RAM

■ FEATURES

- Fast Access Time 45/55ns (max)
- Low Power Standby and Low Power Operation;
Standby: 100 μ W (typ.), Operation: 175mW (typ.)
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Times
- Directly TTL Compatible; All Inputs and Outputs
- Common Data Input and Output; Three-State Outputs
- Pin-Out Compatible with Intel 2148H

■ BLOCK DIAGRAM



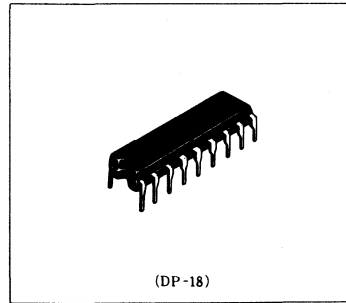
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C
Storage Temperature**	T_{stg}^{**}	-10 to +85	$^{\circ}$ C

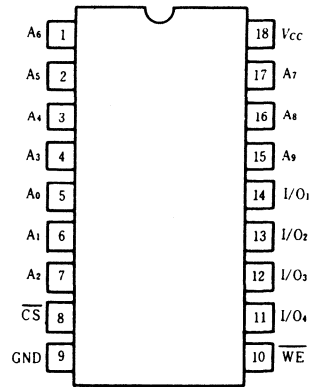
* with respect to GND. $V_{TLmax} = -3.5V$ (Pulse width=20ns)
** under bias

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2



■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5*	—	0.8	V

* -3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS[1] ($T_a=0\sim 70^\circ\text{C}$, $V_{CC}=5V\pm 10\%$, GND=0V)

Parameter	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{L1} $	$V_{CC}=\text{max}$, $V_{in}=\text{GND to } V_{CC}$	—	—	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$, $V_{I/O}=\text{GND to } V_{CC}$	—	—	2.0	μA
Operating Power Supply Current (1)	I_{CC}	$\overline{\text{CS}}=V_{IL}$, $I_{I/O}=0\text{mA}$	—	35	80	mA
Operating Power Supply Current (2)	I_{CC1}	min. cycle, $\overline{\text{CS}}=V_{IL}$, $I_{I/O}=0\text{mA}$	—	50	100	mA
Standby Power Supply Current (1)	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	5	20	mA
Standby Power Supply Current(2)	I_{SB1}	$\overline{\text{CS}}\geq V_{CC}-0.2\text{V}$, $V_{IN}\leq 0.2\text{V}$ or $V_{IN}\geq V_{CC}-0.2\text{V}$	—	20	800	μA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

* Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	—	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	—	7	pF

Note) This parameter is sampled and not 100% tested.

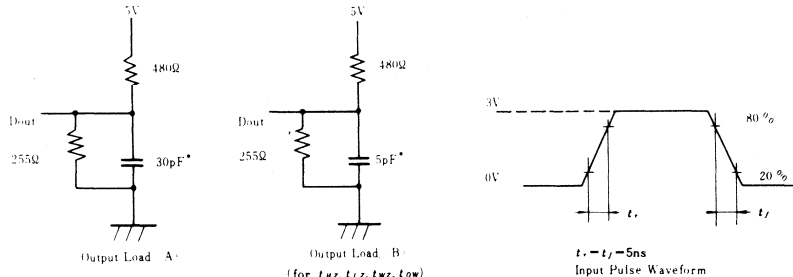
■ AC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

● RISE/FALL TIME

Item	Symbol	min	typ	max	Unit
Input Rise Time	t_r	—	5	100	ns
Input Fall Time	t_f	—	5	100	ns

● AC TEST CONDITIONS

- Input pulse levels : GND to 3.0V
- Input rise and fall times : 5ns
- Input and Output timing reference levels : 1.5V
- Output load : See Figure



* Including scope & jig.

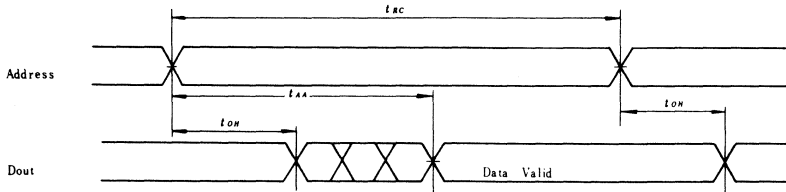
■ AC CHARACTERISTICS ($T_a=0$ to 70°C , $V_{CC}=5V\pm 10\%$, unless otherwise noted.)

● READ CYCLE

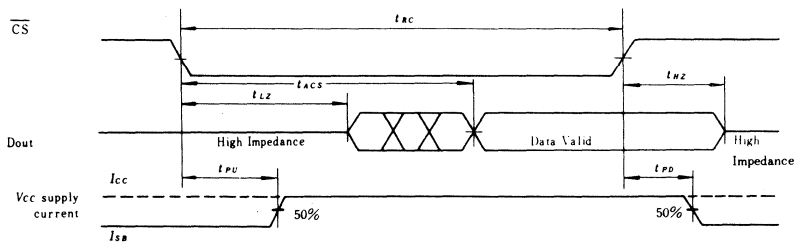
Item	Symbol	HM6148HP-45		HM6148HP-55		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	45	—	55	—	ns
Address Access Time	t_{AA}	—	45	—	55	ns
Chip Select Access Time	t_{ACS}	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}^*	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}^*	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

● TIMING WAVEFORM OF READ CYCLE NO.1 ⁽¹⁾⁽²⁾



● TIMING WAVEFORM OF READ CYCLE NO.2 ⁽¹⁾⁽³⁾



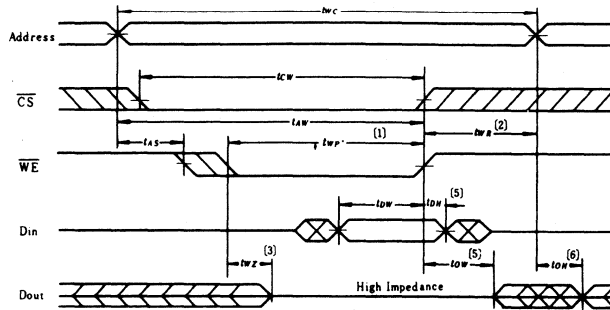
- Notes) 1. \overline{WE} is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with \overline{CS} transition Low.

● WRITE CYCLE

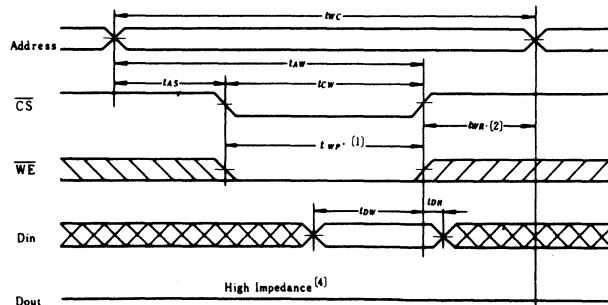
Item	Symbol	HM6148HP-45		HM6148HP-55		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	45	—	55	—	ns
Chip Selection to End of Write	t_{CW}	40	—	50	—	ns
Address Valid to End of Write	t_{AW}	40	—	50	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	ns

* Transition is measured ± 500 mV from steady state voltage with Load B.
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 (\overline{WE} Controlled)



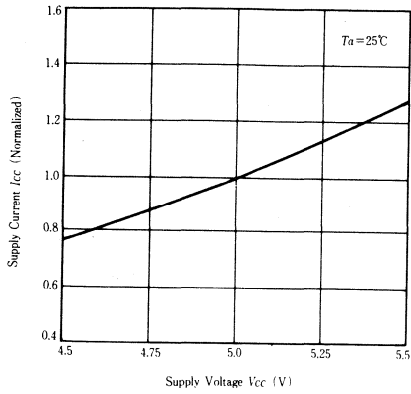
● TIMING WAVEFORM OF WRITE CYCLE NO.2 (\overline{CS} Controlled)



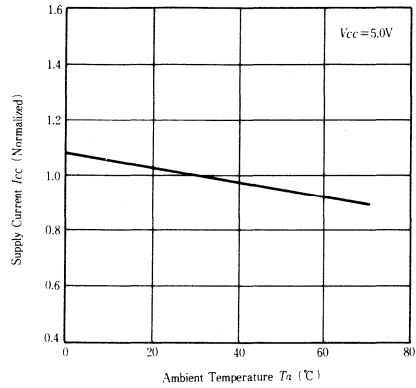
NOTES of Timing Waveform of Write

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . (t_{WP})
2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output buffers remain in a high impedance state.
5. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle.

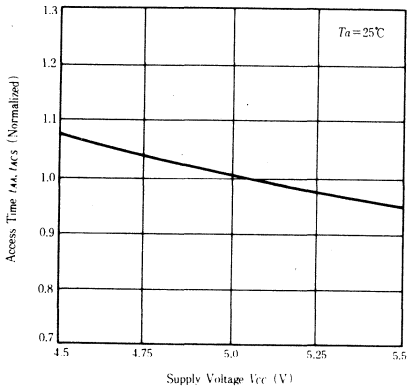
SUPPLY CURRENT VS. SUPPLY VOLTAGE



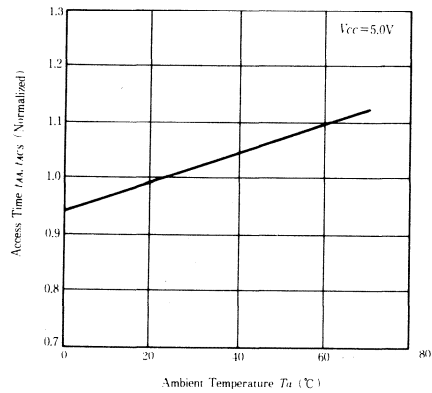
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



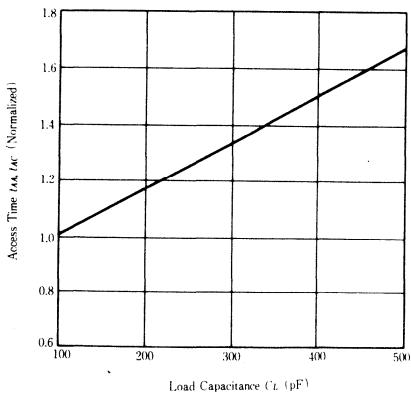
ACCESS TIME VS. SUPPLY VOLTAGE



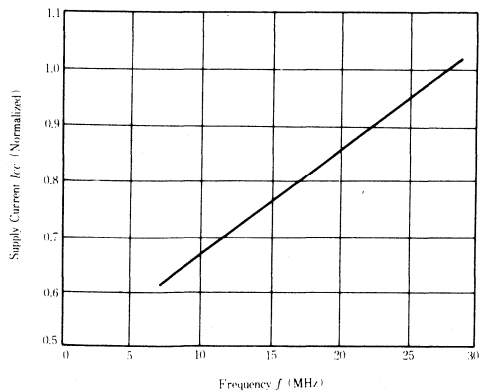
ACCESS TIME VS. AMBIENT TEMPERATURE



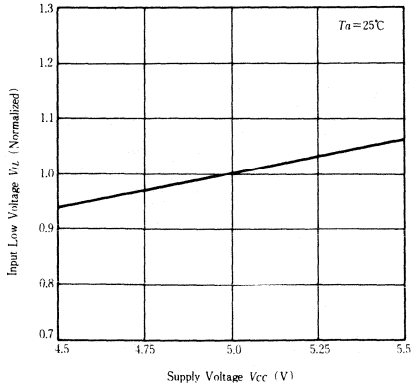
ACCESS TIME VS. LOAD CAPACITANCE



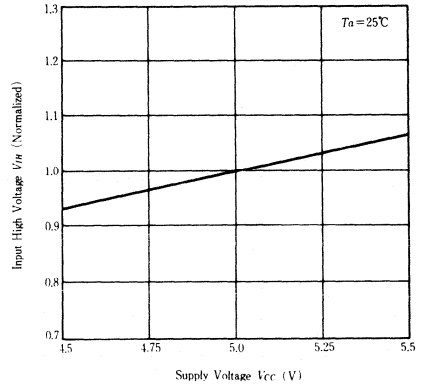
SUPPLY CURRENT VS. FREQUENCY



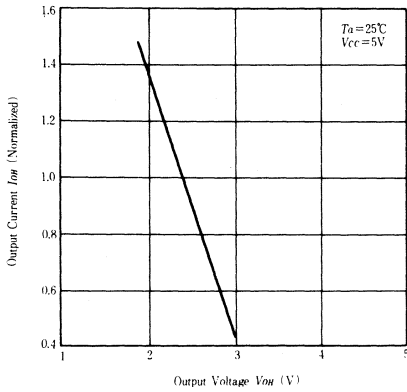
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



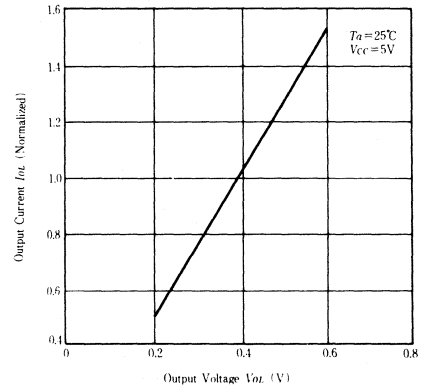
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



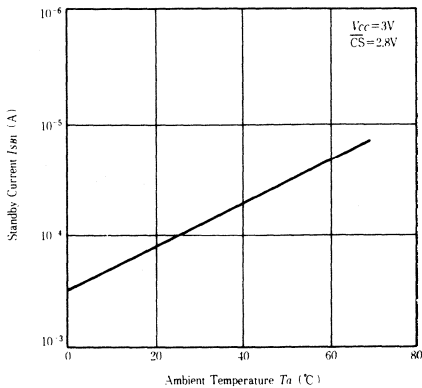
OUTPUT CURRENT VS. OUTPUT VOLTAGE



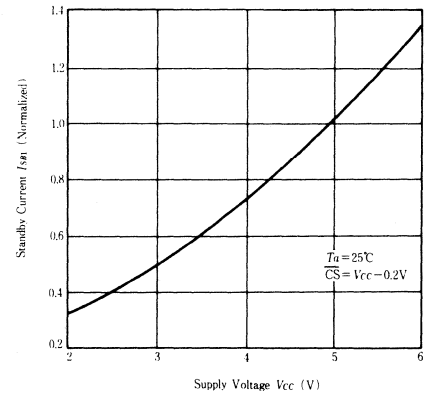
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



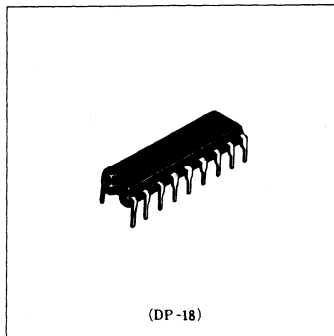
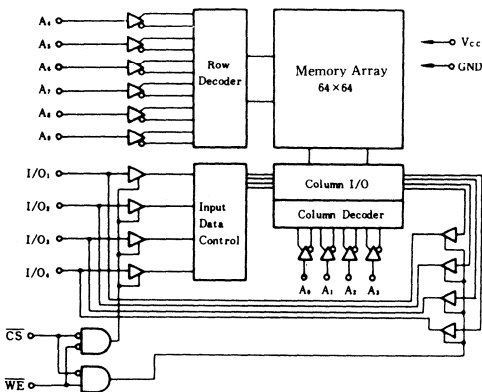
HM6148HLP Series

1024-word × 4-bit High Speed Static CMOS RAM

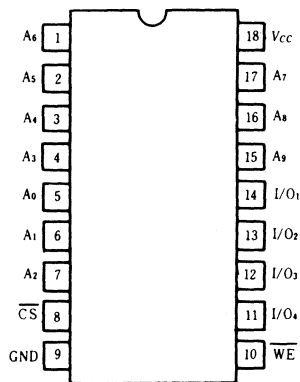
FEATURES

- Low Power Standby and Low Power Operation; Standby: 5μW (typ.), Operation: 175mW (typ.)
- Fast Access Time: 45/55ns (max)
- Capability of Battery Back Up Operation
- Single 5V Supply
- Completely Static RAM: No Clock or Timing Strobe Required
- No Peak Power-On Current
- No Change of t_{ACS} with Short Deselected Time
- Equal Access and Cycle Time
- Directly TTL Compatible: All Inputs and Outputs
- Three State Output
- Pin-Out Compatible with Intel 2148H

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Terminal Voltage*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature**	T_{bias}	-10 to +85	°C

* with respect to GND. $V_{IL(max)} = -3.5V$ (Pulse width = 20ns)

** under bias.

TRUTH TABLE

CS	WE	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.5*	—	0.8	V

* -3.0V (Pulse width 20ns)

■ DC AND OPERATING CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $\text{GND}=0\text{V}$)

Parameter	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{L1} $	$V_{CC}=\text{max}$, $V_{IN}=\text{GND}$ to V_{CC}	—	—	2.0	μA
Output Leakage Current	$ I_{L0} $	$\overline{\text{CS}}=V_{IH}$, $V_{ILO}=\text{GND}$ to V_{CC}	—	—	2.0	μA
Operating Power Supply Current (1)	I_{CC}	$\overline{\text{CS}}=V_{IL}$, $I_{ILO}=0\text{mA}$	—	35	80	mA
Operating Power Supply Current (2)	I_{CC1}	min. cycle, $\overline{\text{CS}}=V_{IL}$, $I_{ILO}=0\text{mA}$	—	50	100	mA
Standby Power Supply Current (1)	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	5	20	mA
Standby Power Supply Current(2)	I_{SB1}	$\overline{\text{CS}}\geq V_{CC}-0.2\text{V}$, $V_{IN}\leq 0.2\text{V}$ or $V_{IN}\geq V_{CC}-0.2\text{V}$	—	1	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

* Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{i1}	$V_{IN}=0\text{V}$	—	5	pF
Input/Output Capacitance	$C_{i/o}$	$V_{ILO}=0\text{V}$	—	7	pF

Note) This parameter is sampled and not 100% tested.

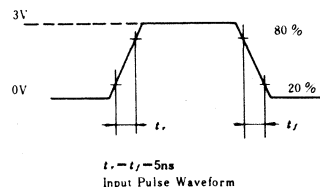
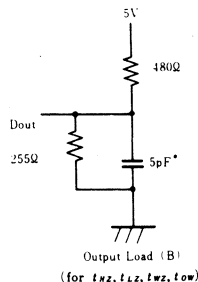
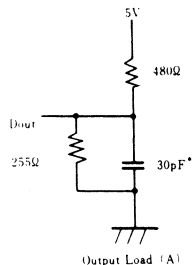
■ AC CHARACTERISTICS ($V_{CC}=5\text{V}\pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

● RISE/FALL TIME

Item	Symbol	min	typ	max	Unit
Input Rise Time	t_r	—	5	100	ns
Input Fall Time	t_f	—	5	100	ns

● AC TEST CONDITIONS

- Input pulse levels : GND to 3.0V
- Input rise and fall times : 5ns
- Input and Output timing reference levels : 1.5V
- Output load : See Figure



* Including scope & jig.

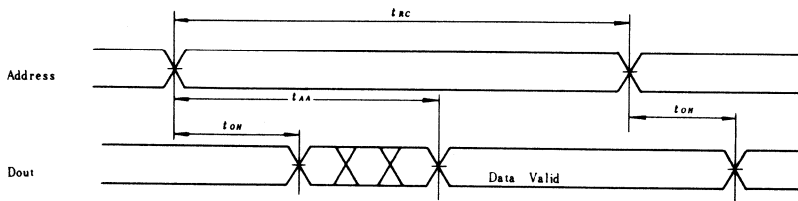
■ AC CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, unless otherwise noted.)

● READ CYCLE

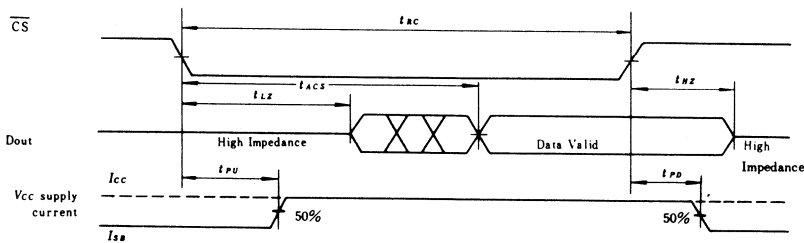
Item	Symbol	HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	45	—	55	—	ns
Address Access Time	t_{AA}	—	45	—	55	ns
Chip Select Access Time	t_{ACS}	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}^*	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}^*	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load(B). This parameter is sampled and not 100% tested.
At any temperature and voltage condition t_{HZ} max is less than t_{LZ} min.

● TIMING WAVEFORM OF READ CYCLE NO.1 (1)(2)



● TIMING WAVEFORM OF READ CYCLE NO.2 (1)(3)



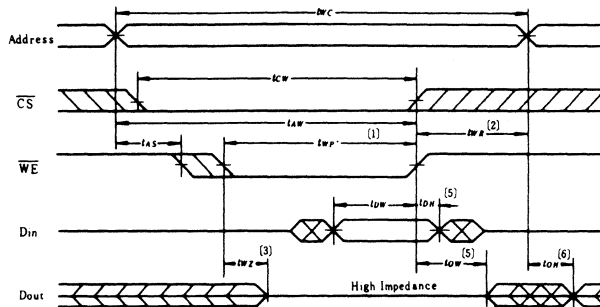
- Notes) 1. \overline{WE} is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with \overline{CS} transition Low.

● WRITE CYCLE

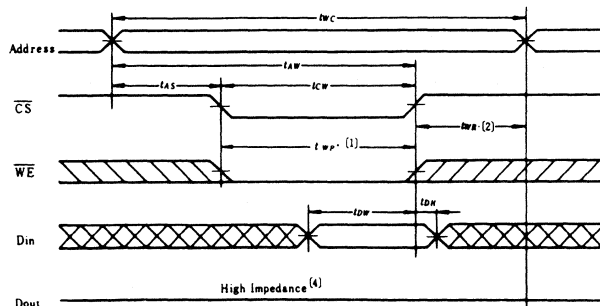
Item	Symbol	HM6148HLP-45		HM6148HLP-55		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	45	—	55	—	ns
Chip Selection to End of Write	t_{CW}	40	—	50	—	ns
Address Valid to End of Write	t_{AW}	40	—	50	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	40	—	ns
Write Recovery Time	t_{WR}	5	—	5	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load B.
 This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO.2 (\overline{CS} Controlled)



Notes of Timing Waveform of Write :

1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . (t_{WP})
2. t_{WZ} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output buffers remain in a high impedance state.
5. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
6. D_{out} is the same phase of write data of this write cycle.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

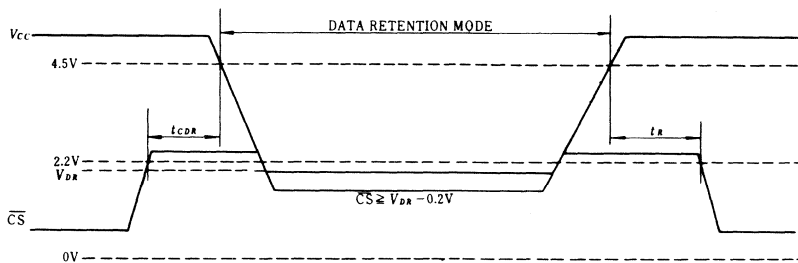
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{iA} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{iA} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		$t_{RC(1)}$	—	—	ns

Note) 1. t_{RC} —Read Cycle Time.

* $V_{CC} = 3.0\text{V}$

** $V_{CC} = 2.0\text{V}$

● LOW V_{CC} DATA RETENTION WAVEFORM



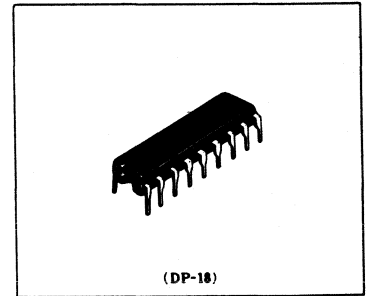
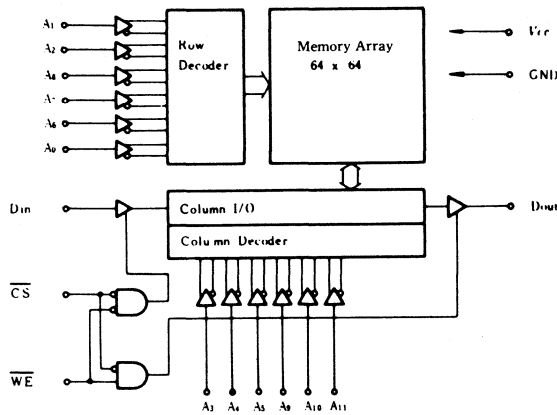
HM6147HP Series

4096-word×1-bit High Speed Static CMOS RAM

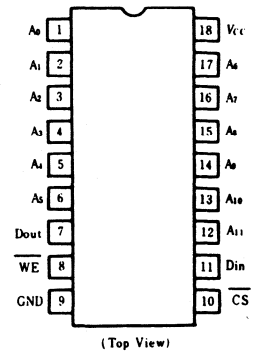
■FEATURES

- High Speed: Fast Access Time 35ns/45ns/55ns Max.
- Low Power Standby and Low Power Operation, Standby: 100μW typ., Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory – No Clock nor Timing Strobe Required
- No Peak Power–On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible – All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_T	-3.5* to +7.0	V
DC Output Current	I_o	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature (under bias)	$T_{stg}(bias)$	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

* Pulse Width 20ns, DC : -0.5V

■ RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.0	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

* Pulse Width 20ns, DC: -0.5V

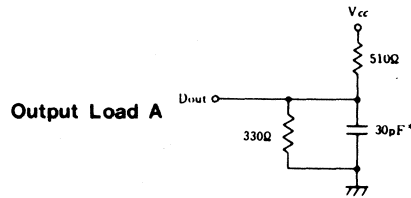
■ DC AND OPERATING CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, GND=0V)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5\text{V}$, GND to V_{CC}	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IH}$, $V_{out} = 0\text{V} \sim V_{CC}$	—	—	10	μA
Operating Power Supply Current(1)	I_{CC}	$\overline{\text{CS}} = V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current(2)	I_{CC1}	$\overline{\text{CS}} = V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current(1)	I_{SB}	$\overline{\text{CS}} = V_{IH}$, $V_{CC} = \text{Min to Max}$	—	8	20	mA
Standby Power Supply Current(2)	I_{SB1}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$, $V_{IH} \leq 0.2\text{V}$ or $V_{IH} \geq V_{CC} - 0.2\text{V}$	—	20	800	μA
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{mA}$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH} = -4\text{mA}$	2.4	—	—	V

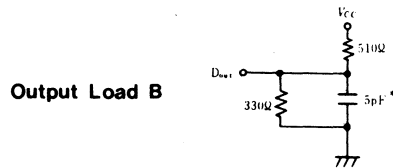
Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet minute.
2. Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^{\circ}\text{C}$ and specified loading.

■ AC TEST CONDITIONS

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels: 1.5V (HM6147HP-35)
0.8 to 2.0V (HM6147HP-45/55)



* Including scope & jig capacitance



■ CAPACITANCE ($T_a = 25^{\circ}\text{C}$, $f = 1.0\text{MHz}$)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	5	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	6	pF

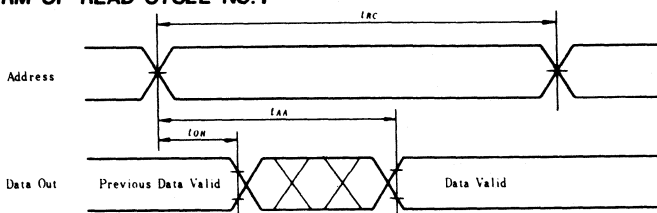
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($T_a=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5\text{V}\pm 10\%$, unless otherwise noted.)

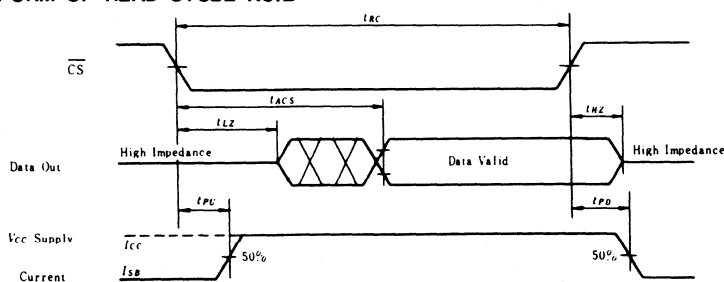
● READ CYCLE

Parameter	Symbol	HM6147HP-35		HM6147HP-45		HM6147HP-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns	[1]
Address Access Time	t_{AA}	—	35	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	[2], [3], [7]
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	[2], [3], [7]
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 ^{(4) (5)}



● TIMING WAVEFORM OF READ CYCLE NO.2 ^{(4) (6)}

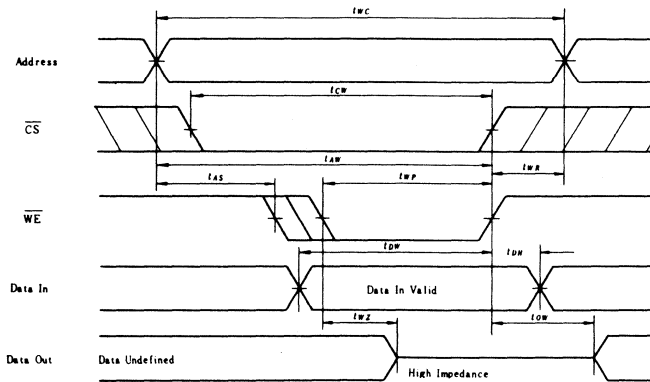


- Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is high for READ Cycle.
 5. Device is continuously selected, $\overline{CS}=V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

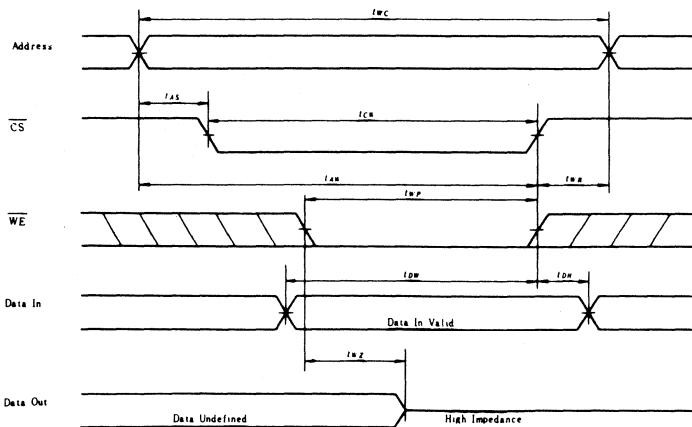
● WRITE CYCLE

Parameter	Symbol	HM6147HP-35		HM6147HP-45		HM6147HP-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns	(2)
Chip Selection to End of Write	t_{CW}	35	—	45	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	10	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	(3), (4)

● TIMING WAVEFORM OF WRITE CYCLE (\overline{WE} Controlled)



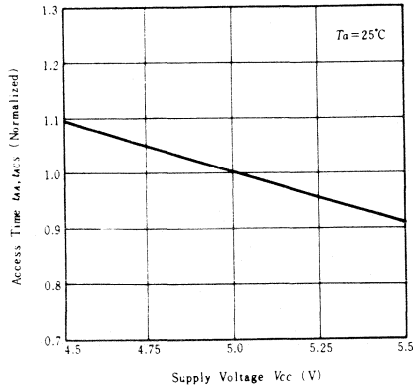
● TIMING WAVEFORM OF WRITE CYCLE (\overline{CS} Controlled)



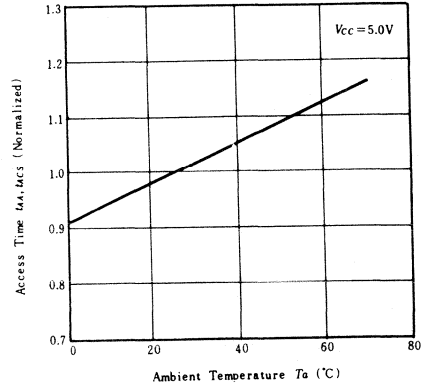
Note) \overline{CS} or \overline{WE} are High for Address Transition

- Notes:
1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

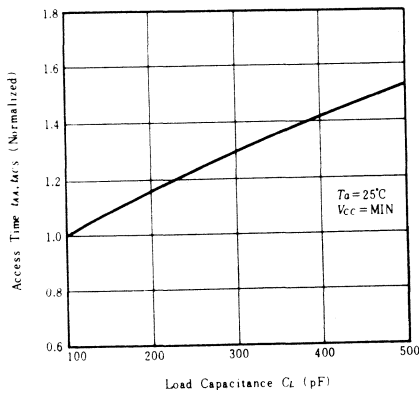
ACCESS TIME VS. SUPPLY VOLTAGE



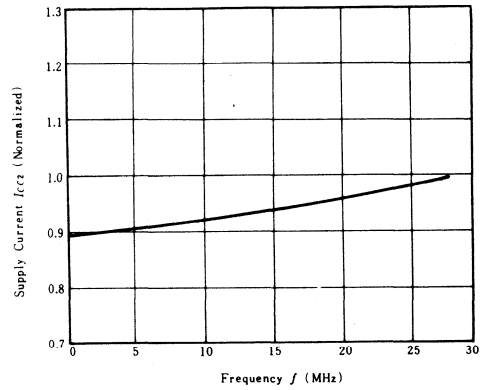
ACCESS TIME VS. AMBIENT TEMPERATURE



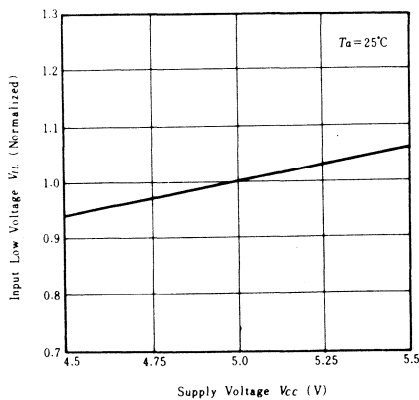
ACCESS TIME VS. LOAD CAPACITANCE



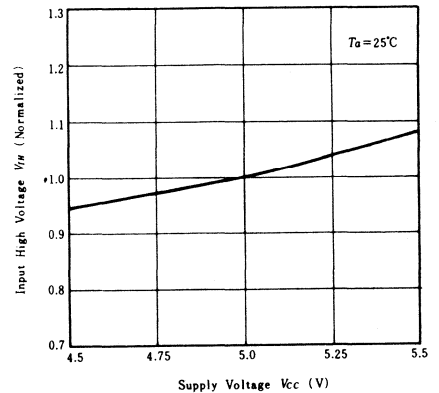
SUPPLY CURRENT VS. FREQUENCY



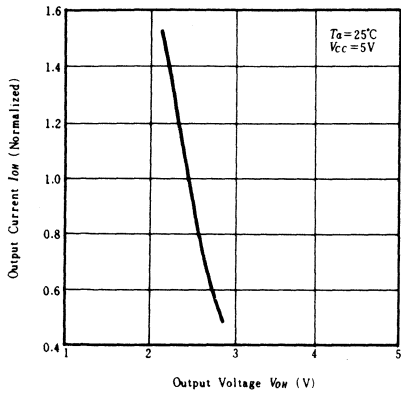
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



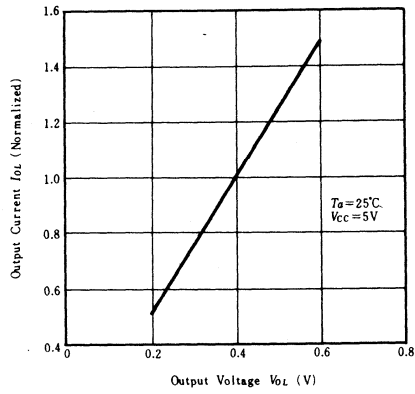
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



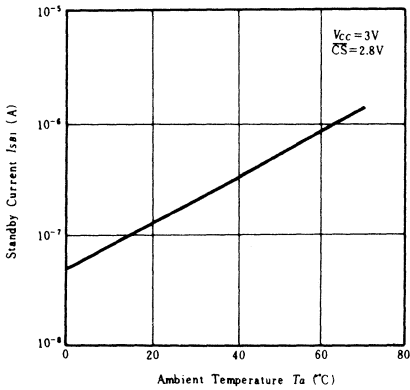
OUTPUT CURRENT VS. OUTPUT VOLTAGE



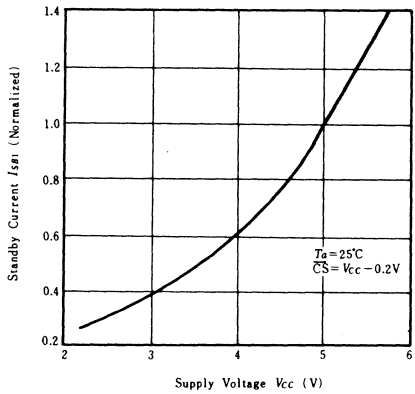
OUTPUT CURRENT VS. OUTPUT VOLTAGE



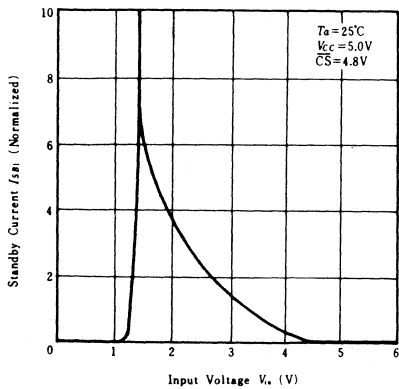
STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



STANDBY CURRENT VS. INPUT VOLTAGE

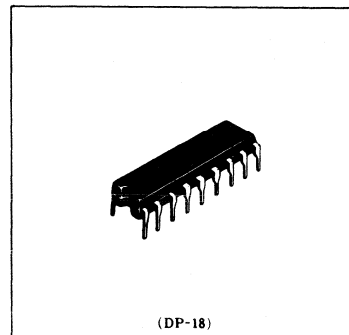


HM6147HLP Series

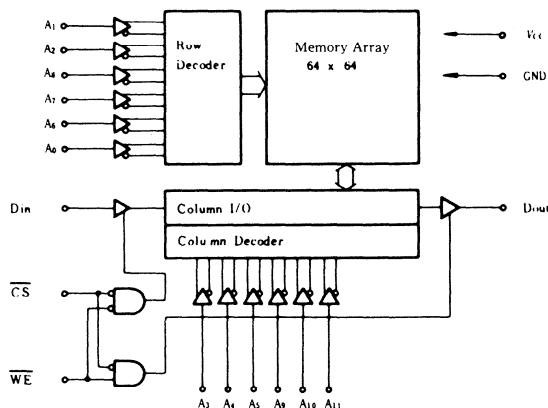
4096-word×1-bit High Speed Static CMOS RAM

FEATURES

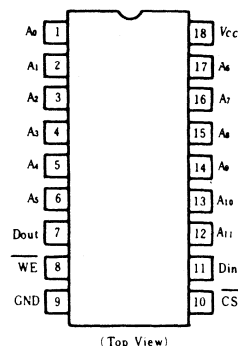
- High Speed: Fast Access Time 35ns/45ns/55ns Max.
- Low Power Standby and Low Power Operation, Standby; 5μW typ., Operation: 150mW typ.
- Single 5V Supply and High Density 18 Pin Package
- Completely Static Memory – No Clock nor Timing Strobe Required
- No Peak Power—On Current
- No Change of t_{ACS} with Short Chip Deselect Time
- Equal Access and Cycle Time
- Directly TTL Compatible – All Input and Output
- Separate Data Input and Output: Three State Output
- Plug-In Replacement with Intel 2147H NMOS STATIC RAM
- Capable of Battery Back up Operation



BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin relative to GND	V_T	-3.5* to +7.0	V
DC Output Current	I_O	20	mA
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature (under bias)	$T_{stg(bias)}$	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

* Pulse Width 20ns, DC: -0.5V

RECOMMENDED DC OPERATING CONDITIONS ($0^\circ\text{C} \leq T_{op} \leq 70^\circ\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	3.0	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.5*	—	0.8	V

* V_{IL} min = -3V (Pulse width \leq 20ns)

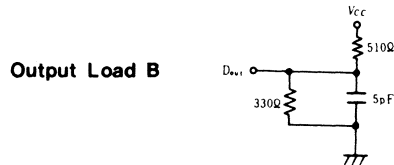
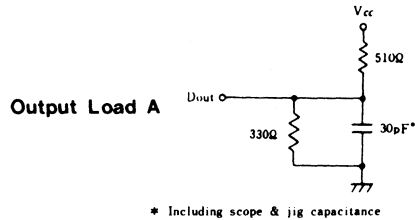
DC AND OPERATING CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$, $V_{CC}=5\text{V} \pm 10\%$, $\text{GND}=0\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{L1} $	$V_{CC}=5.5\text{V}$, GND to V_{CC}	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$, $V_{out}=0\text{V} \sim V_{CC}$	—	—	10	μA
Operating Power Supply Current(1)	I_{CC}	$\overline{\text{CS}}=V_{IL}$, Output open	—	30	80	mA
Operating Power Supply Current(2)	I_{CC1}	$\overline{\text{CS}}=V_{IL}$, Minimum Cycle	—	40	80	mA
Standby Power Supply Current(1)	I_{SB}	$\overline{\text{CS}}=V_{IH}$, $V_{CC}=\text{Min to Max}$	—	5	15	mA
Standby Power Supply Current(2)	I_{SB1}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	—	1	100	μA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.40	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

Note) 1. The operating ambient temperature range is guaranteed with transverse air flow exceeding 400 linear feet per minute.
2. Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=25^{\circ}\text{C}$ and specified loading.

AC TEST CONDITIONS

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5 ns
- Input timing reference levels: 1.5V
- Output load: See Figure
- Output timing reference levels:
1.5V (HM6147HLP-35)
0.8 to 2.0V (HM6147HLP-45/55)



CAPACITANCE ($T_a=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

Item	Symbol	Conditions	max	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	5	pF
Output Capacitance	C_{out}	$V_{out}=0\text{V}$	6	pF

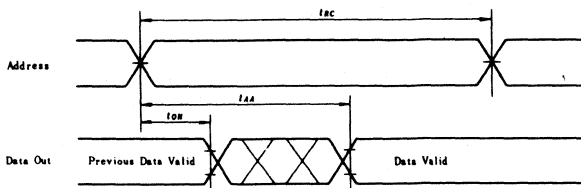
Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($T_a=0^{\circ}\text{C}$ to 70°C , $V_{CC}=5\text{V} \pm 10\%$, unless otherwise noted.)

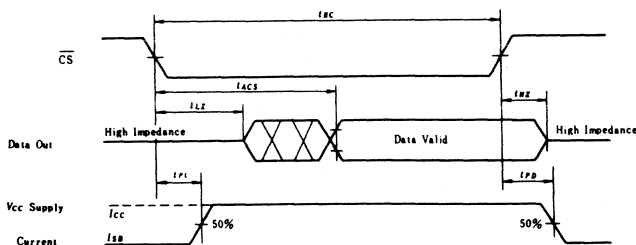
READ CYCLE

Parameter	Symbol	HM6147HLP-35		HM6147HLP-45		HM6147HLP-55		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns	(1)
Address Access Time	t_{AA}	—	35	—	45	—	55	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	(2), (3), (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	(2), (3), (7)
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	20	—	20	ns	

● TIMING WAVEFORM OF READ CYCLE NO.1 (4) (5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4) (6)

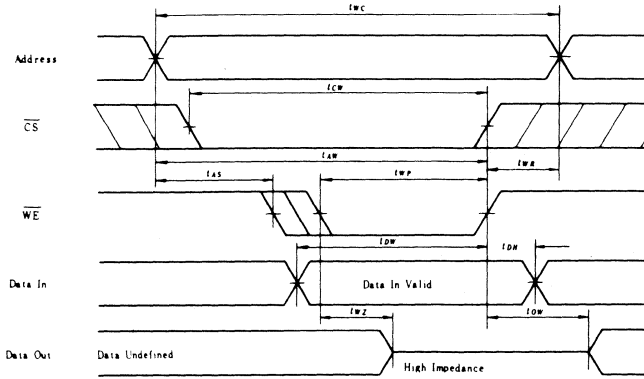


- Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is high for READ Cycle.
 5. Device is continuously selected, $\overline{CS} = V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

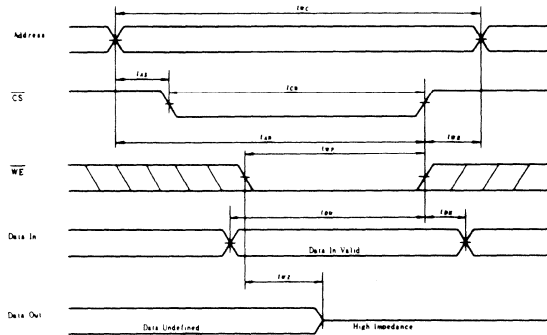
● WRITE CYCLE

Parameter	Symbol	HM6147HLP-35		HM6147HLP-45		HM6147HLP-55		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns	(2)
Chip Selection to End of Write	t_{CW}	35	—	45	—	45	—	ns	
Address Valid to End of Write	t_{AW}	35	—	45	—	45	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	25	—	ns	
Data Hold Time	t_{DH}	10	—	10	—	10	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	20	0	25	0	30	ns	(3), (4)
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	(3), (4)

● TIMING WAVEFORM OF WRITE CYCLE (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE (\overline{CS} Controlled)



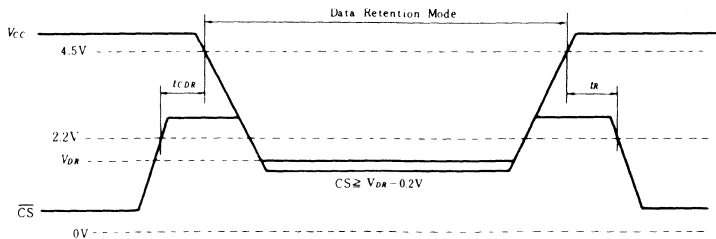
- Notes:
1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a=0^\circ\text{C}$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{IN} \geq V_{CC} - 0.2\text{V}$ or $V_{IN} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0\text{V}$, $\overline{CS} \geq 2.8\text{V}$ $V_{IN} \geq 2.8\text{V}$ or $V_{IN} \leq 0.2\text{V}$	—	—	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^*	—	—	ns

* t_{RC} - Read Cycle Time.

● LOW V_{CC} DATA RETENTION WAVEFORM



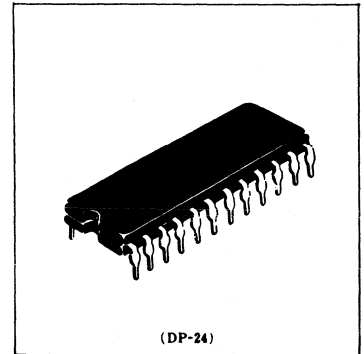
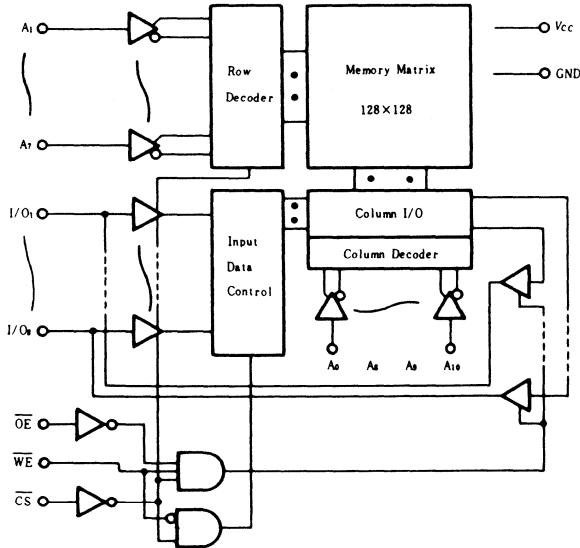
HM6116P Series

2048-word × 8-bit High Speed Static CMOS RAM

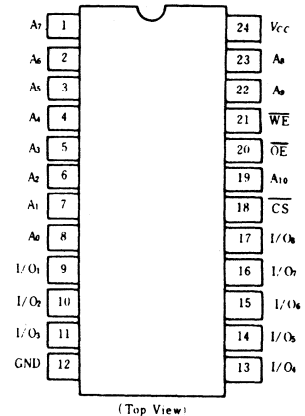
FEATURES

- Single 5V Supply
- High speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 100μW (typ.)
- Low Power Operation Operation: 180mW (typ.)
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	$T_{b,max}$	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : -3.5V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	x	x	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, GND=0V, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	HM6116P-2			HM6116P-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V$, $V_{iA}=\text{GND to } V_{CC}$	—	—	10	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$ or $\overline{\text{OE}}=V_{IH}$, $V_{iO}=\text{GND to } V_{CC}$	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}$, $I_{iO}=0\text{mA}$	—	40	80	—	35	70	mA
	I_{CC1}^{**}	$V_{IH}=3.5V$, $V_{IL}=0.6V$, $I_{iO}=0\text{mA}$	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty = 100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{\text{CS}} \geq V_{CC}-0.2V$, $V_{iA} \geq V_{CC}-0.2V$ or $V_{iA} \leq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	—	—	0.4	—	—	—	V
		$I_{OL}=2.1\text{mA}$	—	—	—	—	—	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	—	—	2.4	—	—	V

* $V_{CC}=5V$, $T_a=25^\circ\text{C}$

** Reference Only

AC CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CNZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{ONZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116P-2		HM6116P-3		HM6116P-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{wc}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{cw}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{aw}	105	—	120	—	140	—	ns
Address Set Up Time	t_{as}	20	—	20	—	20	—	ns
Write Pulse Width	t_{wp}	70	—	90	—	120	—	ns
Write Recovery Time	t_{wr}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{onz}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{wz}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{dw}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{dh}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{ow}	5	—	10	—	10	—	ns

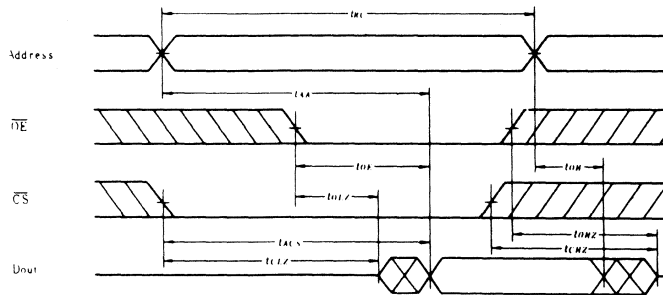
■ CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{i/o}$	$V_{i/o}=0\text{V}$	5	7	pF

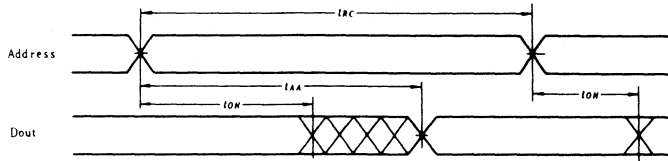
Note: This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

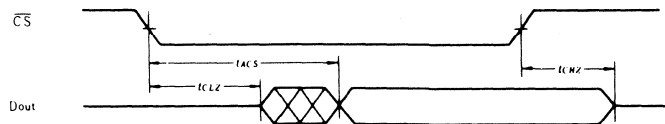
● READ CYCLE (1) ⁽¹⁾



● READ CYCLE (2) ⁽¹⁾⁽²⁾⁽⁴⁾

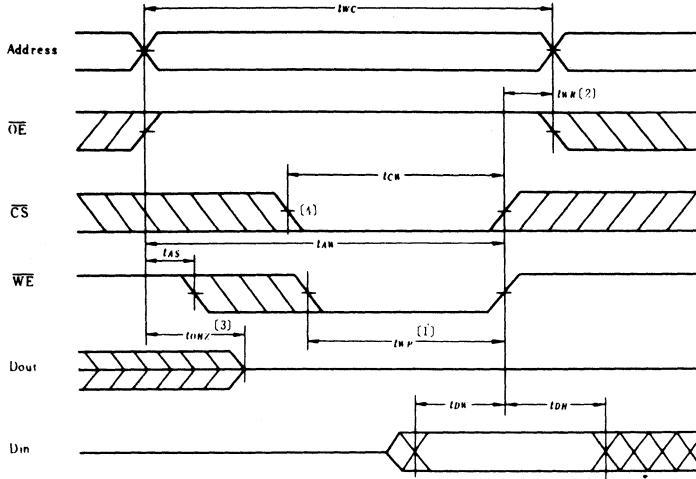
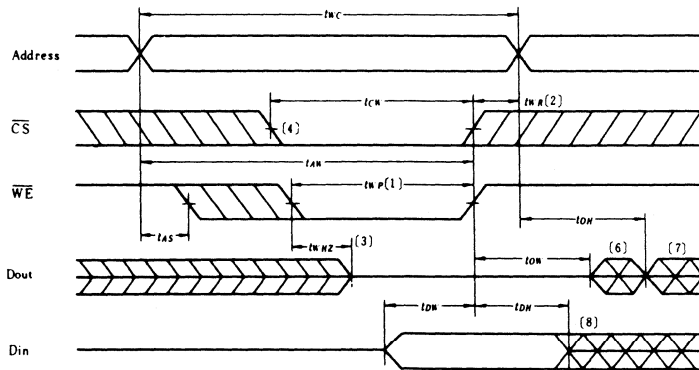


● READ CYCLE (3) ⁽¹⁾⁽³⁾⁽⁴⁾



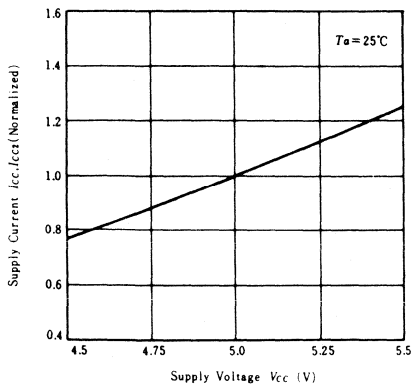
- NOTES: 1. \overline{WE} is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

WRITE CYCLE (1)

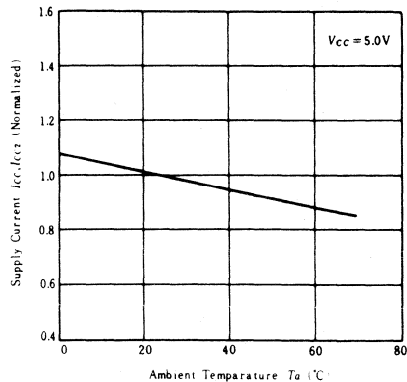
● WRITE CYCLE (2) ⁽⁵⁾

- NOTES:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
 5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 6. D_{out} is the same phase of write data of this write cycle.
 7. D_{out} is the read data of next address.
 8. If \overline{CS} is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

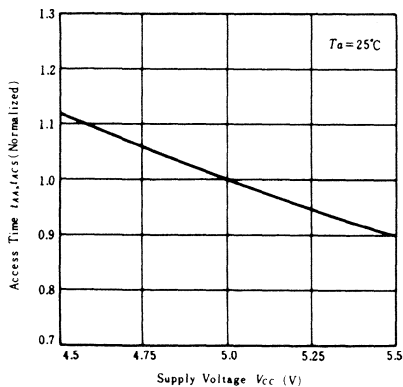
**SUPPLY CURRENT
vs. SUPPLY VOLTAGE**



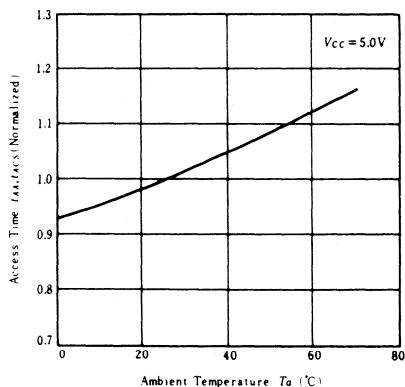
**SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**



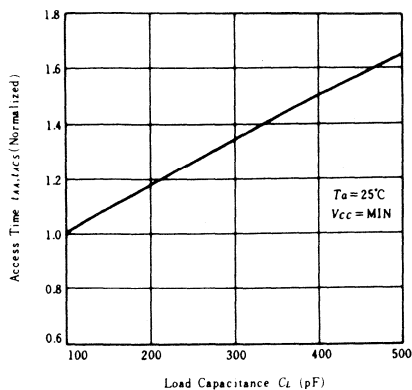
**ACCESS TIME
vs. SUPPLY VOLTAGE**



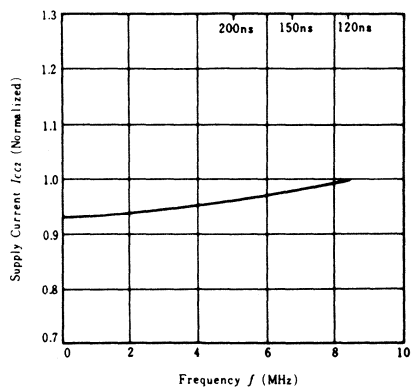
**ACCESS TIME
vs. AMBIENT TEMPERATURE**



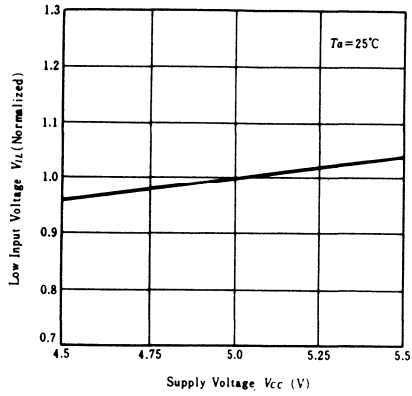
**ACCESS TIME
vs. LOAD CAPACITANCE**



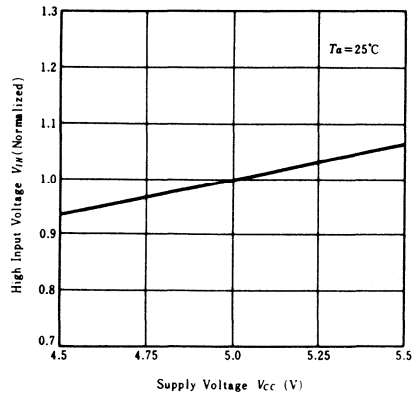
**SUPPLY CURRENT
vs. FREQUENCY**



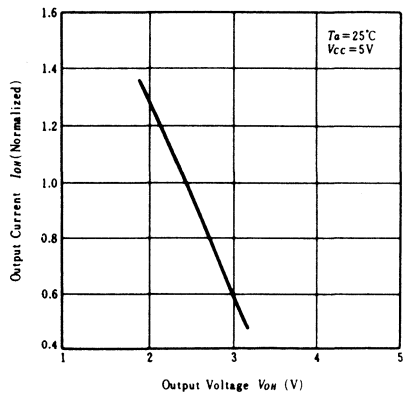
**LOW INPUT VOLTAGE
vs. SUPPLY VOLTAGE**



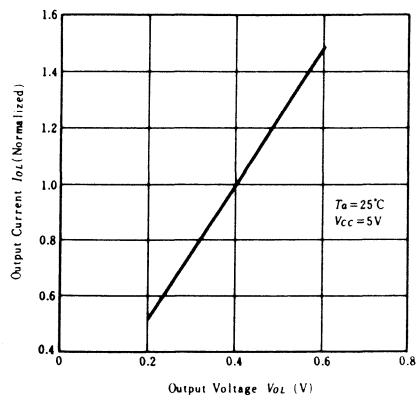
**HIGH INPUT VOLTAGE
vs. SUPPLY VOLTAGE**



**OUTPUT CURRENT
vs. OUTPUT VOLTAGE**



**OUTPUT CURRENT
vs. OUTPUT VOLTAGE**



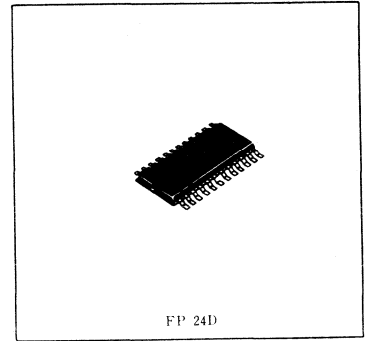
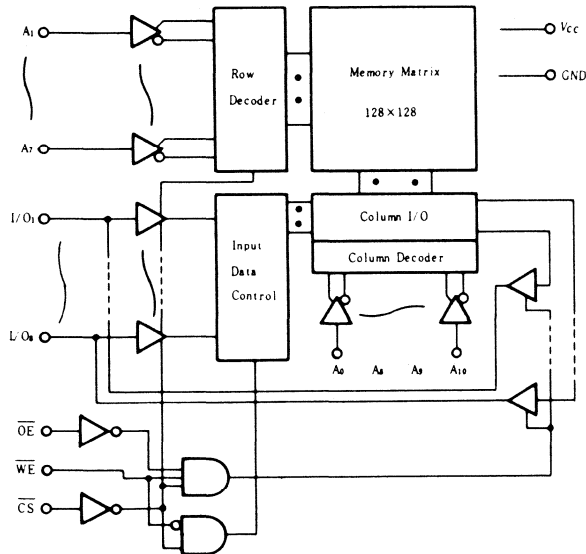
HM6116FP Series

2048-word × 8-bit High Speed Static CMOS RAM

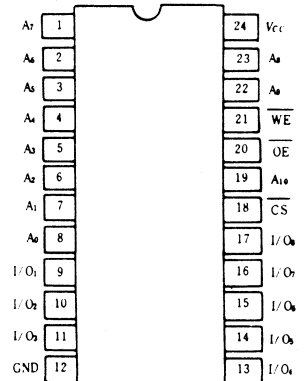
■ FEATURES

- High Density Small-Sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby Standby: 100μW (typ.)
- Low Power Operation; Operation: 180mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

■ FUNCTIONAL BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	$T_{i,b}$	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : 3.5V

■ TRUTH TABLE

\overline{CS}	\overline{OE}	WE	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	x	x	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle(1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle(1)
L	L	L	Write	I_{CC}	Din	Write Cycle(2)

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	—	0.8	V

* Pulse Width : 50ns, DC : V_{IL} min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $GND=0V$, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	HM6116FP-2			HM6116FP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V$, $V_{in}=GND$ to V_{CC}	—	—	10	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$ $V_{LO}=GND$ to V_{CC}	—	—	10	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{LO}=0\text{mA}$	—	40	80	—	35	70	mA
	I_{CC1}^{**}	$V_{IH}=3.5V$, $V_{IL}=0.6V$, $I_{LO}=0\text{mA}$	—	35	—	—	30	—	mA
Average Operating Current	I_{CC2}	Min. cycle, duty = 100%	—	40	80	—	35	70	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	15	—	5	15	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{in}\geq V_{CC}$ $-0.2V$ or $V_{in}\leq 0.2V$	—	0.02	2	—	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	—	—	0.4	—	—	—	V
		$I_{OL}=2.1\text{mA}$	—	—	—	—	—	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	—	—	2.4	—	—	V

* $V_{CC}=5V$, $T_a=25^\circ\text{C}$

** Reference Only

AC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116FP-2		HM6116FP-3		HM6116FP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DOW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

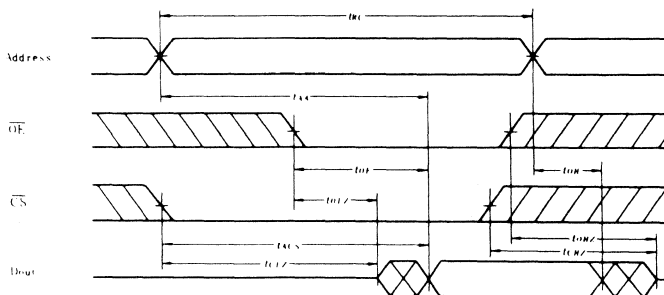
■ CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	5	7	pF

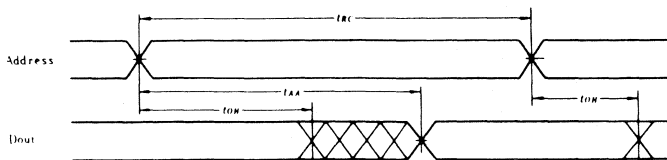
Note. This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

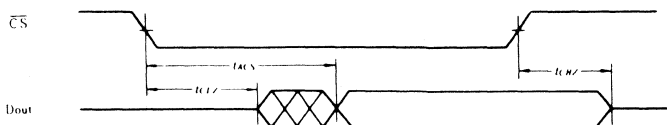
● READ CYCLE (1)⁽¹⁾



● READ CYCLE (2)⁽¹⁾⁽²⁾⁽⁴⁾



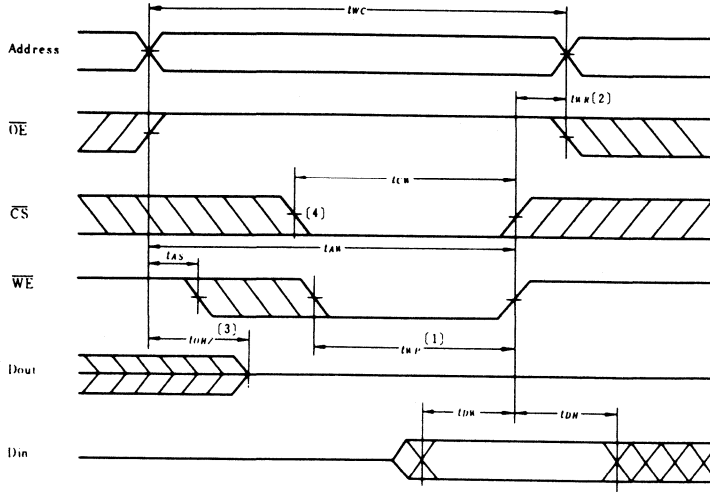
● READ CYCLE (3)⁽¹⁾⁽³⁾⁽⁴⁾



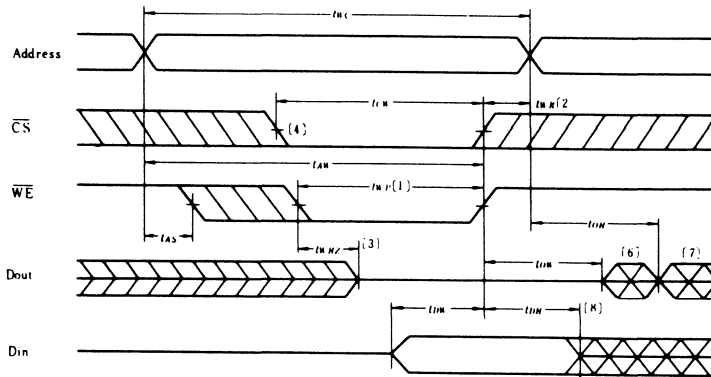
- NOTES: 1. \overline{WE} is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

■ TIMING WAVEFORM

● WRITE CYCLE (1) ⁽¹⁾

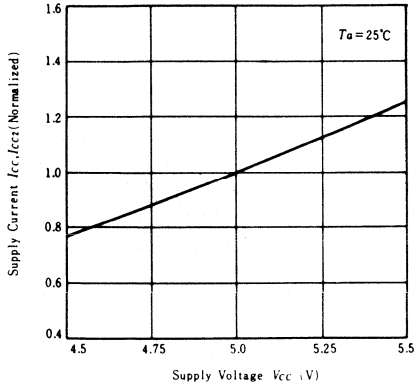


● WRITE CYCLE (2) ⁽⁵⁾

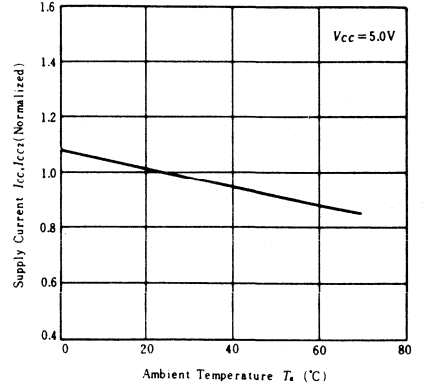


- NOTES:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
 5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 6. D_{out} is the same phase of write data of this write cycle.
 7. D_{out} is the read data of next address.
 8. If \overline{CS} is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

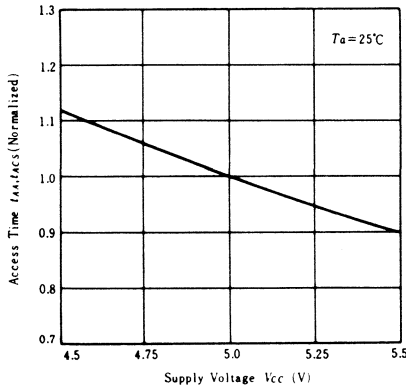
**SUPPLY CURRENT
vs. SUPPLY VOLTAGE**



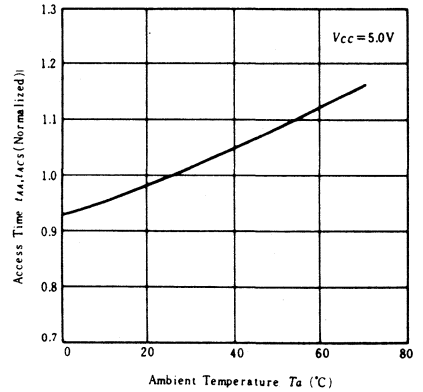
**SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**



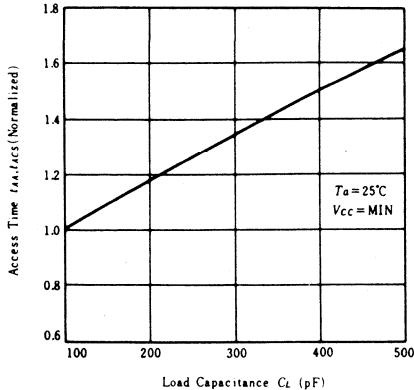
**ACCESS TIME
vs. SUPPLY VOLTAGE**



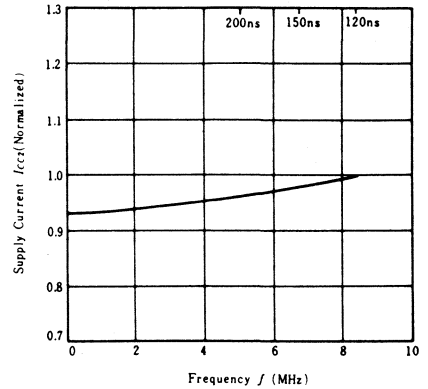
**ACCESS TIME
vs. AMBIENT TEMPERATURE**



**ACCESS TIME
vs. LOAD CAPACITANCE**



**SUPPLY CURRENT
vs. FREQUENCY**



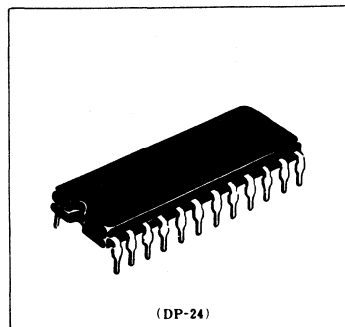
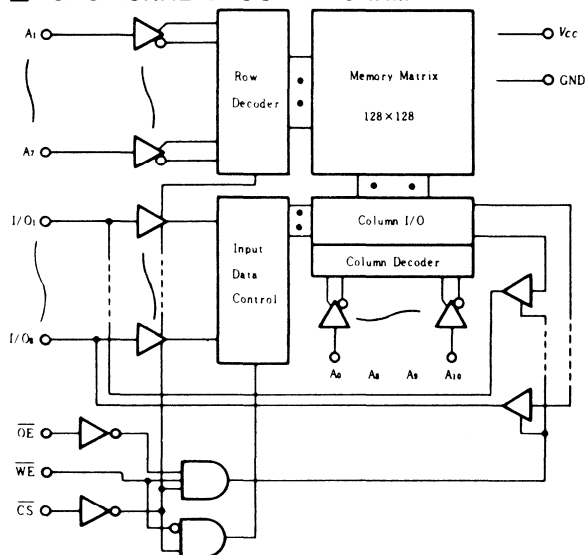
HM6116LP Series

2048-word × 8-bit High Speed Static CMOS RAM

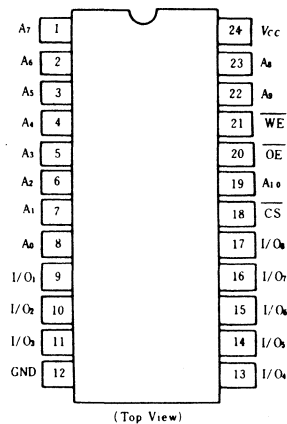
FEATURES

- Single 5V Supply and High Density 24 Pin Package
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 10 μ W (typ.)
Low Power Operation; Operation: 160mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	$T_{v,bb}$	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : 3.5V

TRUTH TABLE

CS	OE	WE	Mode	V_{cc} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{sb}, I_{sb1}	High Z	
L	L	H	Read	I_{cc}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{cc}	Din	Write Cycle (1)
L	L	L	Write	I_{cc}	Din	Write Cycle (2)

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $GND=0\text{V}$, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	HM6116LP-2			HM6116LP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{in}=GND$ to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{io}=GND$ to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{io}=0\text{mA}$	—	35	70	—	30	60	mA
	I_{CC1}^{**}	$V_{IH}=3.5\text{V}$, $V_{IL}=0.6\text{V}$, $I_{io}=0\text{mA}$	—	30	—	—	25	—	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$, $V_{in} \geq V_{CC} - 0.2\text{V}$ or $V_{in} \leq 0.2\text{V}$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	—	—	0.4	—	—	—	V
		$I_{OL}=2.1\text{mA}$	—	—	—	—	—	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	—	—	2.4	—	—	V

* : $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

** : Reference Only

AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116LP-2		HM6116LP-3		HM6116LP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{ONZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WNZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

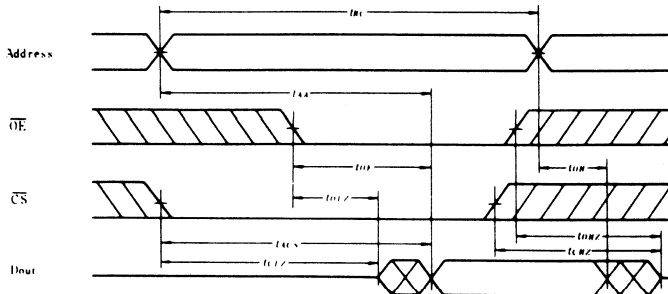
■ CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{i1}	$V_{i1} = 0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{i/o}$	$V_{i/o} = 0\text{V}$	5	7	pF

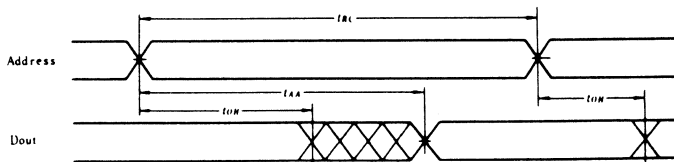
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

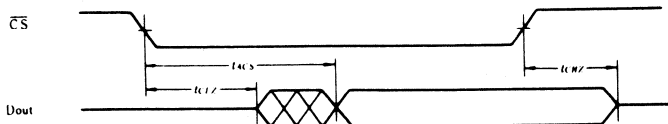
● Read Cycle (1) ⁽¹⁾



● Read Cycle (2) ^{(1), (2), (4)}

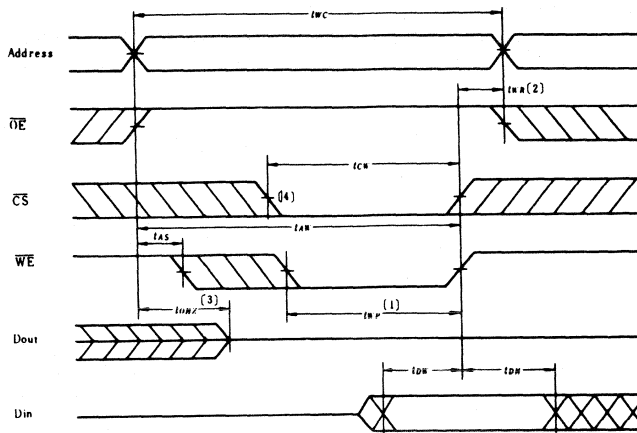


● Read Cycle (3) ^{(1), (3), (4)}

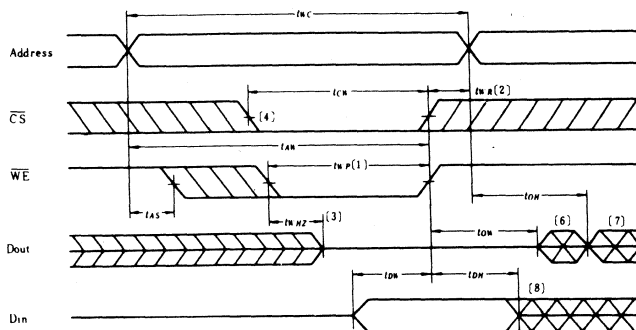


- NOTES: 1. \overline{WE} is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

● Write Cycle (1)



● Write Cycle (2) (5)



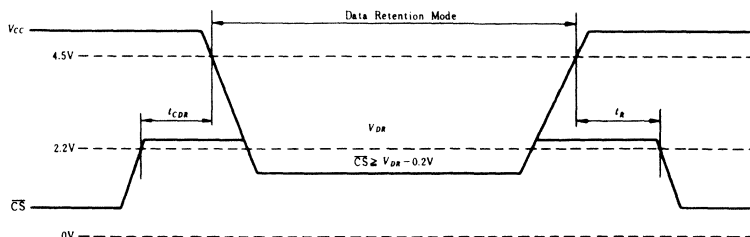
- NOTES:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
 5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 6. D_{out} is the same phase of write data of this write cycle.
 7. D_{out} is the read data of next address.
 8. If \overline{CS} is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{cc} DATA RETENTION CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$)

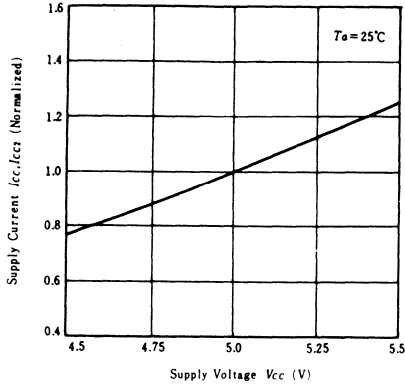
Item	Symbol	Test Conditions	min	typ	max	Unit
V_{cc} for Data Retention	V_{DR}	$\overline{CS} \geq V_{cc} - 0.2V, V_{i1} \geq V_{cc} - 0.2V$ or $V_{i1} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}^*	$V_{cc} = 3.0V, \overline{CS} \geq 2.8V, V_{i1} \geq 2.8V$ or $V_{i1} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^{**}	—	—	ns

* $10 \mu\text{A}$ max at $T_a=0^\circ\text{C}$ to $+40^\circ\text{C}$, V_{i1} min = $-0.3V$
 ** t_{RC} = Read Cycle Time.

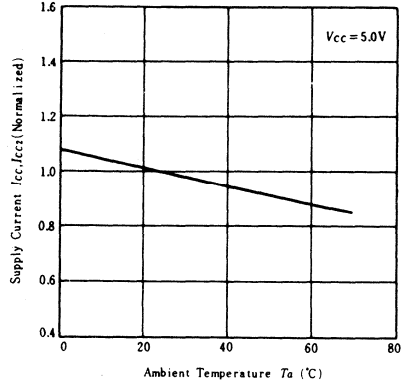
● Low V_{cc} Data Retention Waveform



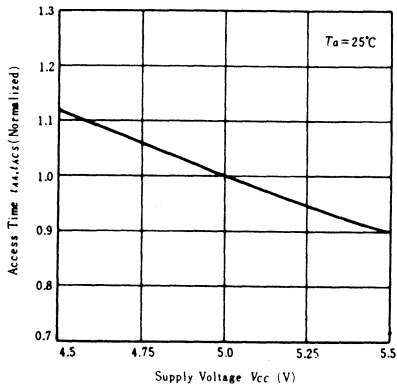
SUPPLY CURRENT vs. SUPPLY VOLTAGE



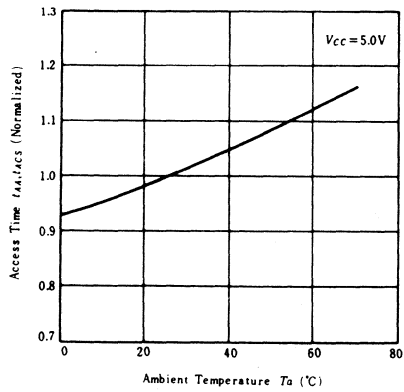
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



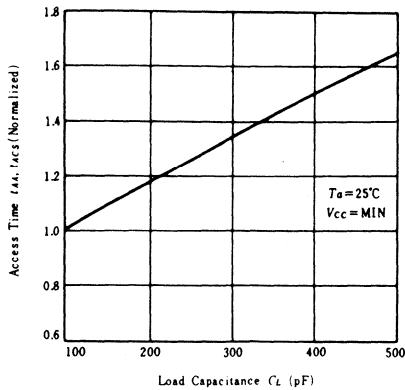
ACCESS TIME vs. SUPPLY VOLTAGE



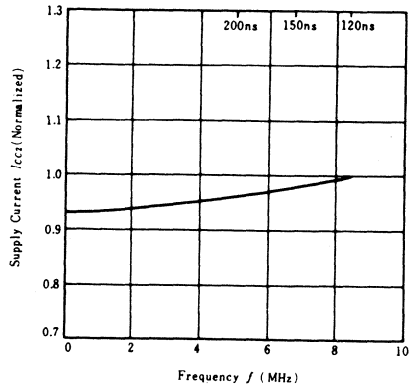
ACCESS TIME vs. AMBIENT TEMPERATURE



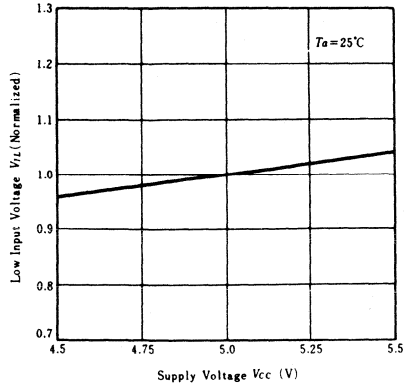
ACCESS TIME vs. LOAD CAPACITANCE



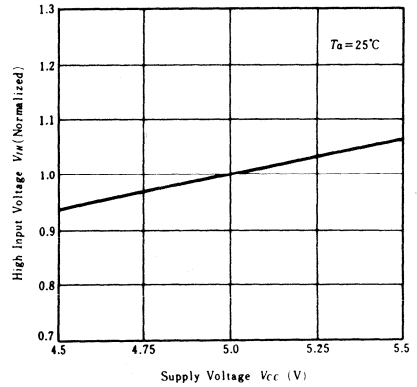
SUPPLY CURRENT vs. FREQUENCY



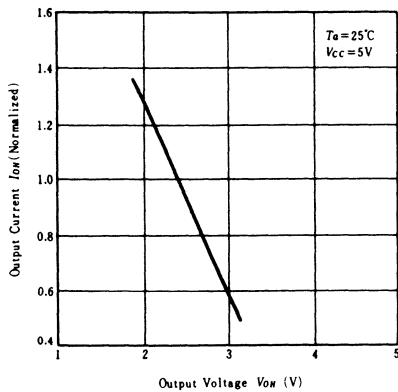
LOW INPUT VOLTAGE vs. SUPPLY VOLTAGE



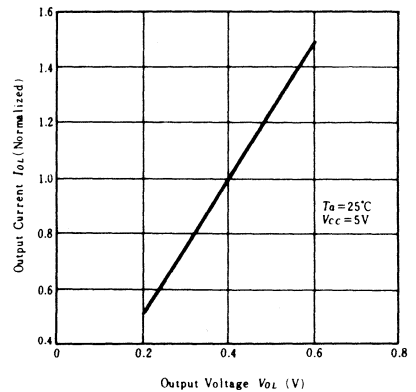
HIGH INPUT VOLTAGE vs. SUPPLY VOLTAGE



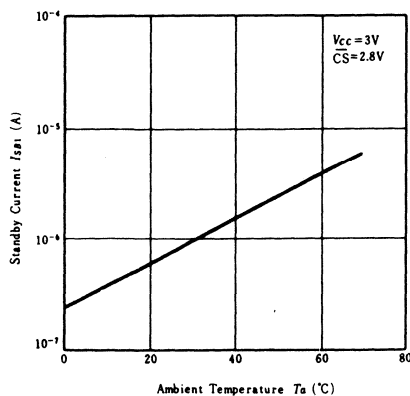
OUTPUT CURRENT vs. OUTPUT VOLTAGE



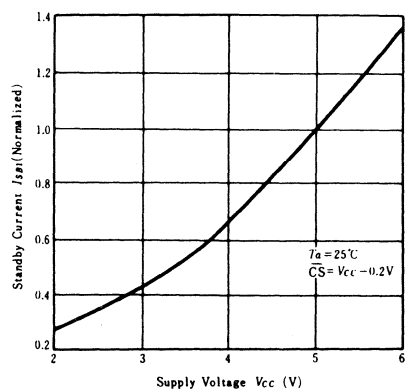
OUTPUT CURRENT vs. OUTPUT VOLTAGE



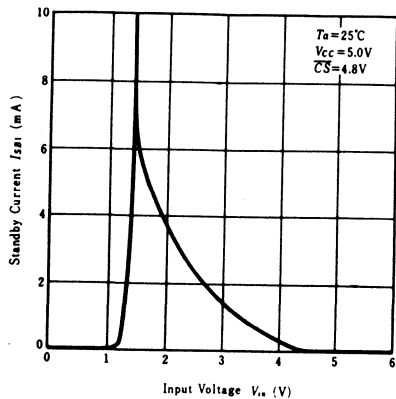
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



**STANDBY CURRENT vs.
INPUT VOLTAGE**

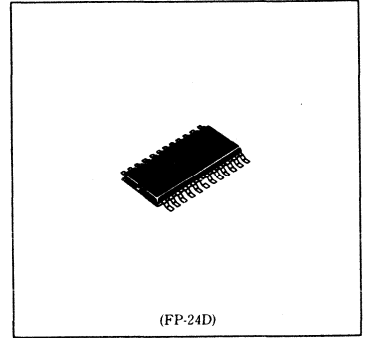


HM6116LFP Series

2048-word × 8-bit High Speed Static CMOS RAM

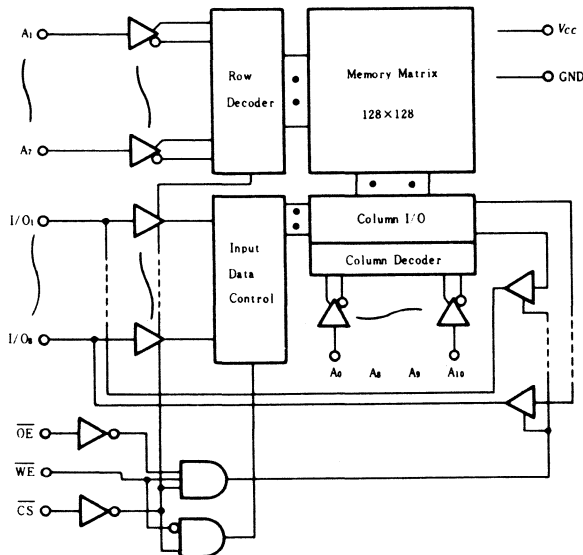
FEATURES

- High Density Small-sized Package
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- Single 5V Supply
- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 10μW (typ.)
- Low Power Operation; Operation: 160mW (typ.)
- Completely Static RAM: No Clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time
- Capability of Battery Back up Operation

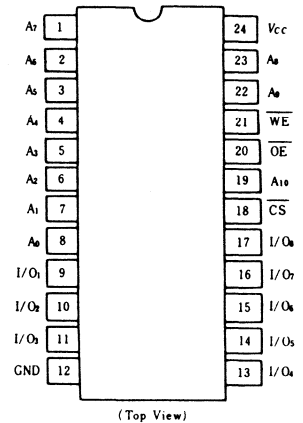


(FP-24D)

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{mb}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse width 50ns : - 3.5V

TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	—	0.8	V

* Pulse Width: 50ns, DC: V_{IL} min = -0.3V.

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, GND=0V, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	HM6116LFP-2			HM6116LFP-3/-4			Unit
			min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V$, $V_{i,s}=GND$ to V_{CC}	—	—	2	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{i,o}=GND$ to V_{CC}	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{i,o}=0\text{mA}$	—	35	70	—	30	60	mA
	I_{CC1}^{**}	$V_{IH}=3.5V$, $V_{IL}=0.6V$, $I_{i,o}=0\text{mA}$	—	30	—	—	25	—	mA
Average Operating Current	I_{CCz}	Min cycle, duty=100%	—	35	70	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	4	12	—	4	12	mA
	I_{SB1}	$\overline{CS}\geq V_{CC}-0.2V$, $V_{i,s}\geq V_{CC}-0.2V$ or $V_{i,s}\leq 0.2V$	—	2	50	—	2	50	μA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	—	—	0.4	—	—	—	V
		$I_{OL}=2.1\text{mA}$	—	—	—	—	—	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	—	—	2.4	—	—	V

* : $V_{CC}=5V$, $T_a=25^\circ\text{C}$

** : Reference Only

AC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	200	—	ns
Address Access Time	t_{AA}	—	120	—	150	—	200	ns
Chip Select Access Time	t_{ACS}	—	120	—	150	—	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	15	—	15	—	ns
Output Enable to Output Valid	t_{OE}	—	80	—	100	—	120	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	15	—	15	—	ns
Chip deselection to Output in High Z	t_{CNZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{ONZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	—	15	—	15	—	ns

● WRITE CYCLE

Item	Symbol	HM6116LFP-2		HM6116LFP-3		HM6116LFP-4		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	20	—	20	—	20	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	120	—	ns
Write Recovery Time	t_{WR}	5	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	50	0	60	0	60	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	60	—	ns
Data Hold from Write Time	t_{DH}	5	—	10	—	10	—	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

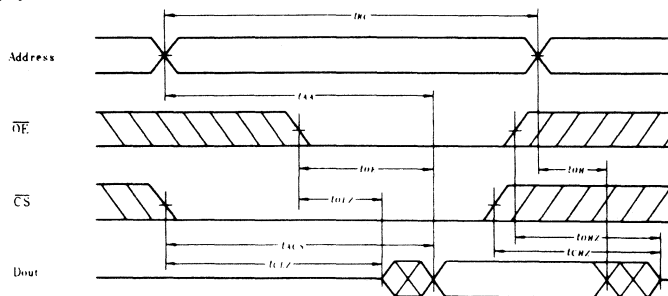
■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{i/o}$	$V_{i/o} = 0\text{V}$	5	7	pF

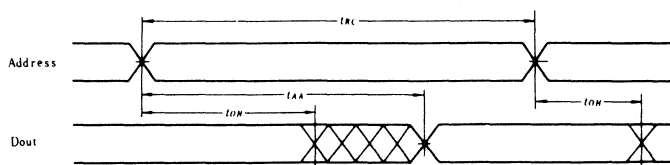
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

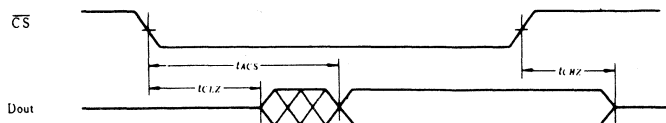
● READ CYCLE (1) ⁽¹⁾



● READ CYCLE (2) ^{(1) (2) (4)}

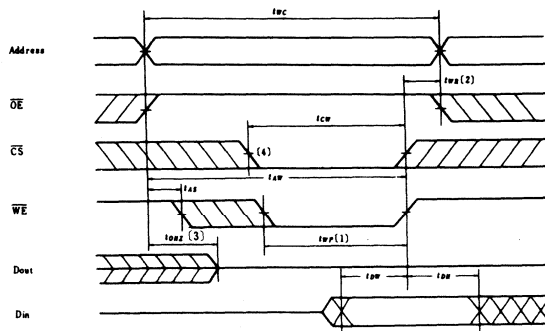


● READ CYCLE (3) ^{(1) (3) (4)}

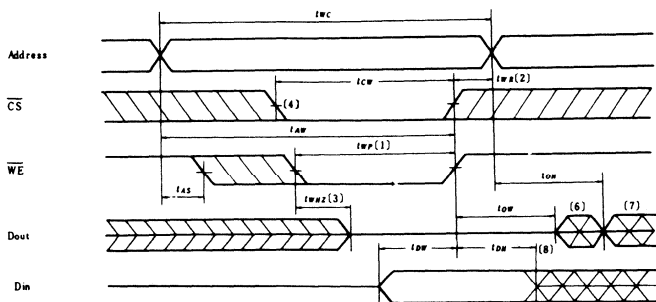


- NOTES:
1. \overline{WE} is High for Read Cycle
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $OE = V_{IL}$.

● WRITE CYCLE (1)



● WRITE CYCLE (2) (5)



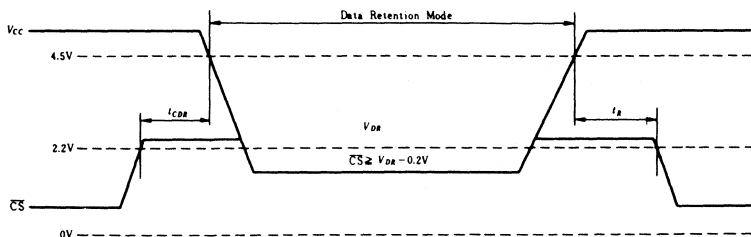
- NOTES: 1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
 5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 6. D_{out} is the same phase of write data of this write cycle.
 7. D_{out} is the read data of next address.
 8. If \overline{CS} is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2V$ $V_{IN} \geq V_{CC} - 0.2V$ or $V_{IN} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}^*	$V_{CC} = 3.0V$, $\overline{CS} \geq 2.8V$ $V_{IN} \geq 2.8V$ or $V_{IN} \leq 0.2V$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R	See Retention Waveform	—	—	—	ns

* V_{IL} min = $-0.3V$, $10 \mu A$ max (at $T_a=0$ to $+40^\circ\text{C}$)
 ** t_{RC} - Read Cycle Time.

● Low V_{CC} DATA RETENTION WAVEFORM



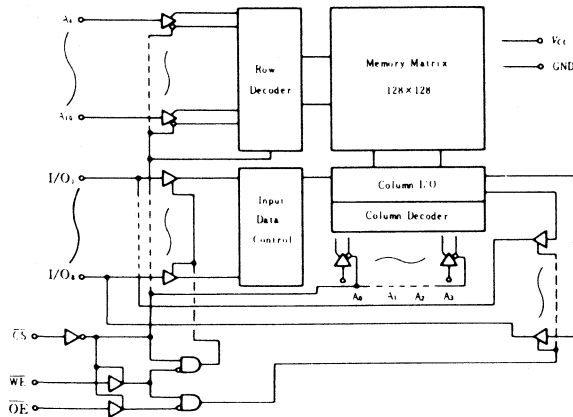
HM6116AP Series, HM6116ASP Series

2048-word × 8-bit High Speed Static CMOS RAM

■ FURTURES

- High speed: Fast Access Time 120ns/150ns/200ns. (max.)
- Low Power Standby and Standby: 100 μ W (typ.)
Low Power Operation Operation: 15mW (typ.) (f = 1MHz)
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock or Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

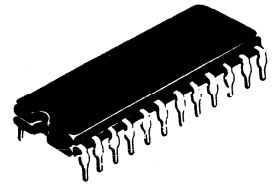
Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_I	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{mb}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* Pulse Width 50ns : 3.5V

■ TRUTH TABLE

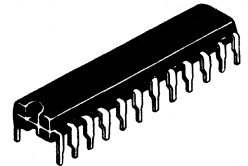
CS	OE	WE	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	x	x	Not Selected	I_{SB}, I_{SB1}	High Z	
L	L	H	Read	I_{CC}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{CC}	Din	Write Cycle (1)
L	L	L	Write	I_{CC}	Din	Write Cycle (2)

HM6116AP Series



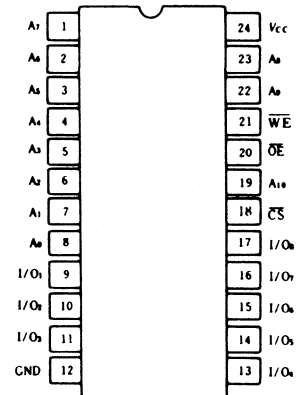
(DP-24)

HM6116ASP Series



(DP-24N)

■ PIN ARRANGEMENT



(Top View)

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	-	0.8	V

 * Pulse Width: 50ns, DC: V_{IL} min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, GND = 0V, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	HM6116AP/ ASP-12			HM6116AP/ ASP-15			HM6116AP/ ASP-20			Unit
			min	typ*	max	min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND}$ to V_{CC}	-	-	2	-	-	2	-	-	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}$ or $\overline{\text{OE}}=V_{IH}$, $V_{I/O}=\text{GND}$ to V_{CC}	-	-	2	-	-	2	-	-	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}$, $I_{I/O}=0\text{mA}$ $V_{in}=V_{IH}$ or V_{IL}	-	5	15	-	5	15	-	5	15	mA
	I_{CC1}	$V_{IH}=V_{CC}$, $V_{IL}=0\text{V}$, $\overline{\text{CS}}=V_{IL}$, $I_{I/O}=0\text{mA}$, $f=1\text{MHz}$	-	3	6	-	3	6	-	3	6	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	-	35	60	-	25	45	-	20	35	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	-	1	4	-	1	4	-	1	4	mA
	I_{SB1}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$	-	0.02	2	-	0.02	2	-	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	-	-	0.4	-	-	0.4	-	-	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	-	-	2.4	-	-	2.4	-	-	V

 * $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$
AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

 Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116AP/ ASP-12		HM6116AP/ ASP-15		HM6116AP/ ASP-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
Chip Select Access Time	t_{ACS}	-	120	-	150	-	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	ns
Output Enable to Output Valid	t_{OE}	-	55	-	60	-	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	-	10	-	10	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	-	15	-	20	-	ns

● WRITE CYCLE

Item	Symbol	HM6116AP/ ASP-12		HM6116AP/ ASP-15		HM6116AP/ ASP-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	70	—	80	—	100	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	50	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	10	—	ns

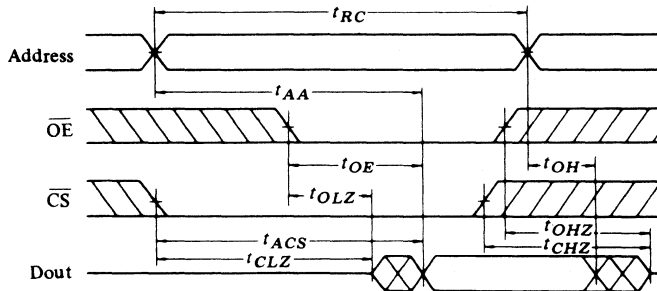
■ CAPACITANCE ($f=1\text{MHz}$, $T_a=25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	$C_{i\cdot}$	$V_{i\cdot}=0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{i/o}$	$V_{i/o}=0\text{V}$	5	7	pF

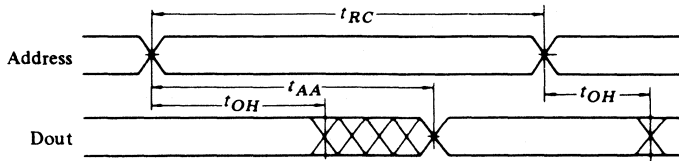
Note) This parameter is sampled and not 100% tested.

■ TIMING WAVEFORM

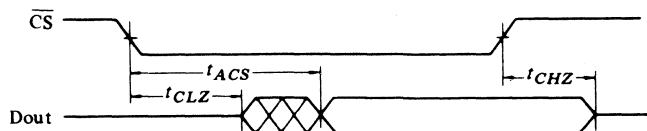
● READ CYCLE (1) ⁽¹⁾



● READ CYCLE (2) ⁽¹⁾⁽²⁾⁽⁴⁾

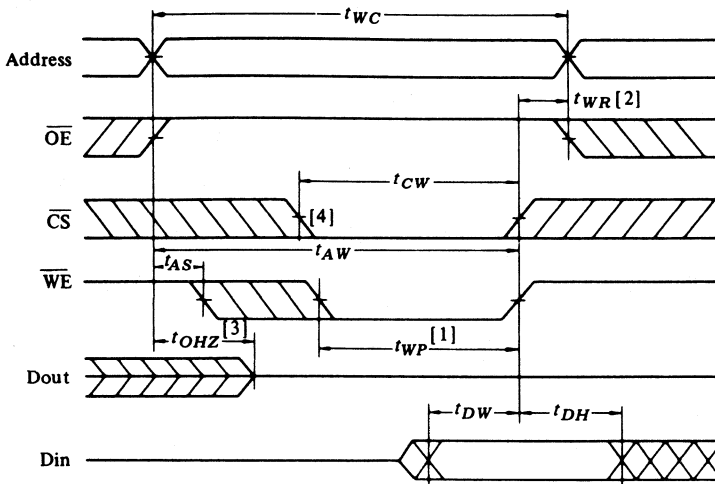


● READ CYCLE (3) ⁽¹⁾⁽³⁾⁽⁴⁾

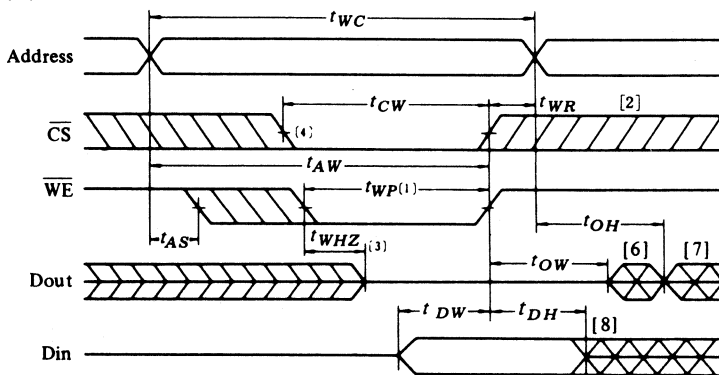


- NOTES: 1. WE is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

● WRITE CYCLE(1)

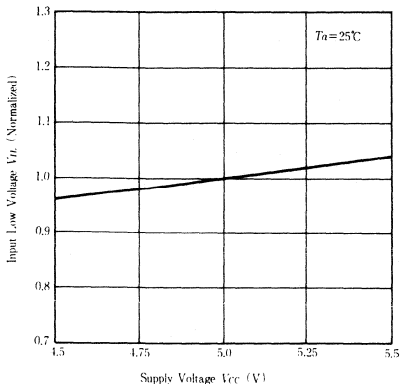


● WRITE CYCLE(2)⁽⁵⁾

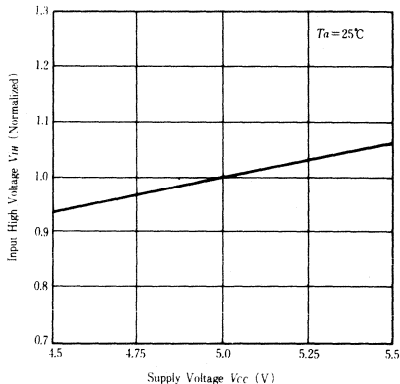


- NOTES:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE} transition, output remain in a high impedance state.
 5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 6. D_{out} is the same phase of write data of this write cycle.
 7. D_{out} is the read data of next address.
 8. If \overline{CS} is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

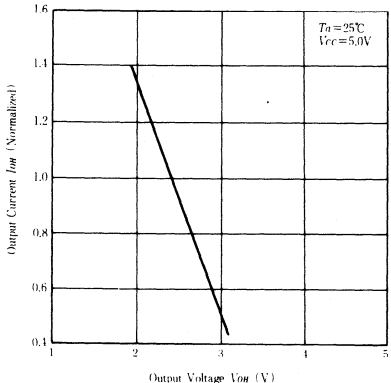
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



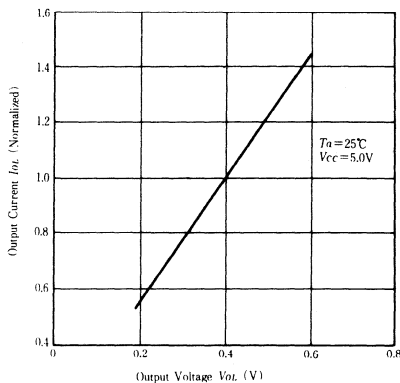
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



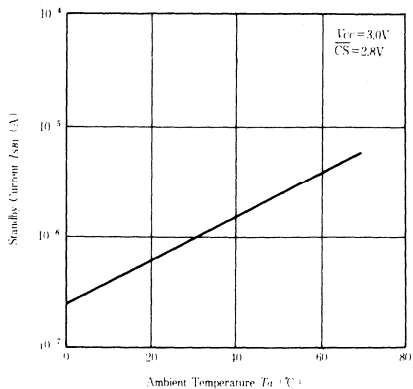
OUTPUT CURRENT VS. OUTPUT VOLTAGE



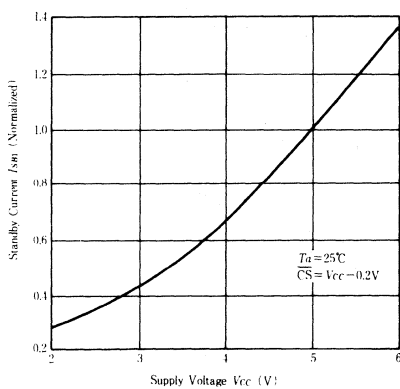
OUTPUT CURRENT VS. OUTPUT VOLTAGE



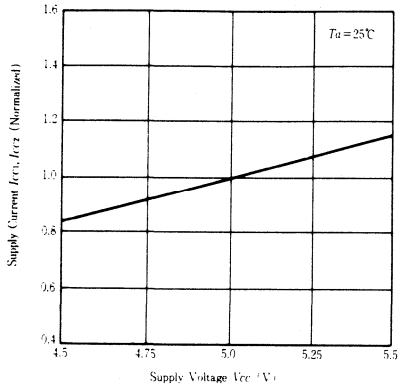
STANDBY CURRENT VS. AMBIENT TEMPERATURE



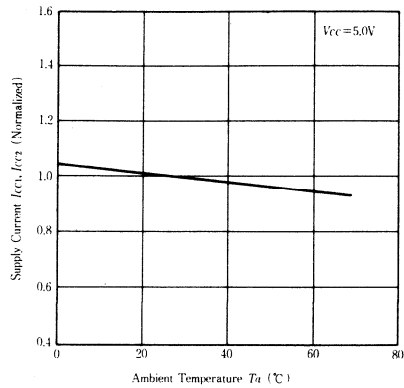
STANDBY CURRENT VS. SUPPLY VOLTAGE



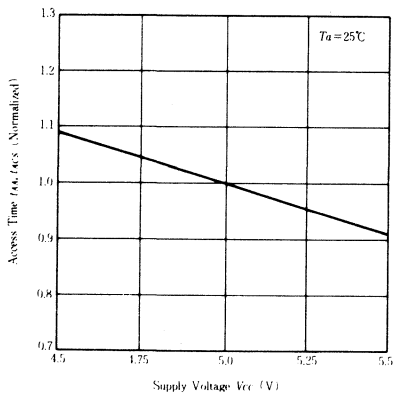
SUPPLY CURRENT VS. SUPPLY VOLTAGE



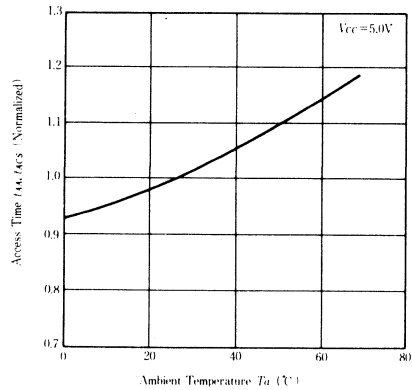
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



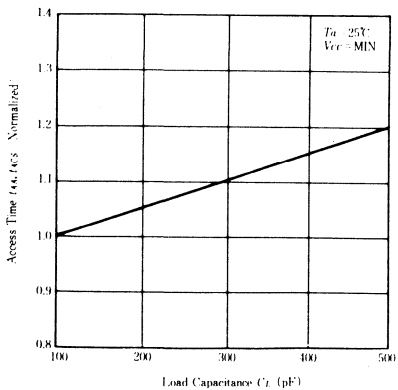
ACCESS TIME VS. SUPPLY VOLTAGE



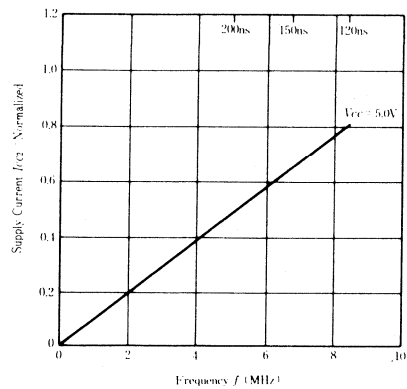
ACCESS TIME VS. AMBIENT TEMPERATURE



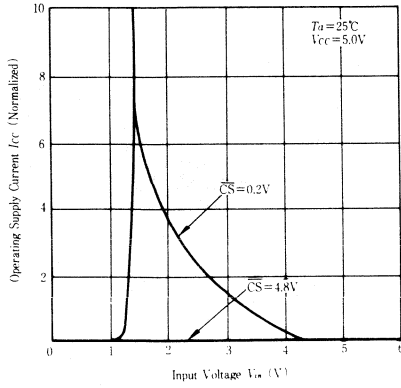
ACCESS TIME VS. LOAD CAPACITANCE



SUPPLY CURRENT VS. FREQUENCY



OPERATING SUPPLY CURRENT VS. INPUT VOLTAGE



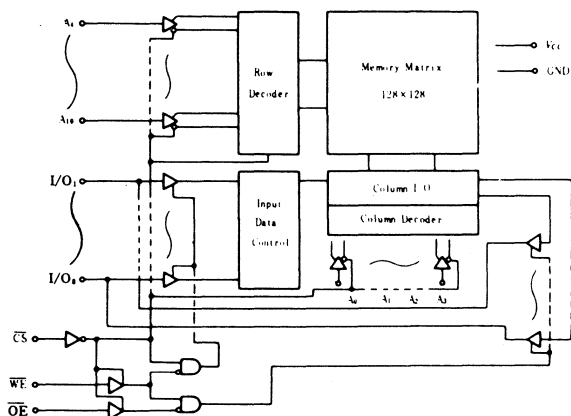
HM6116ALP Series, HM6116ALSP Series

2048-word × 8-bit High Speed Static CMOS RAM

■ FEATURES

- High Speed: Fast Access Time 120ns/150ns/200ns (max.)
- Low Power Standby and Standby: 5μW (typ.)
Low Power Operation; Operation: 10mW (typ.) (f = 1MHz)
- Capability of Battery Back up Operation
- Single 5V Supply and High Density 24 Pin Package
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Pin Out Compatible with Standard 16K EPROM/MASK ROM
- Equal Access and Cycle Time

■ FUNCTIONAL BLOCK DIAGRAM



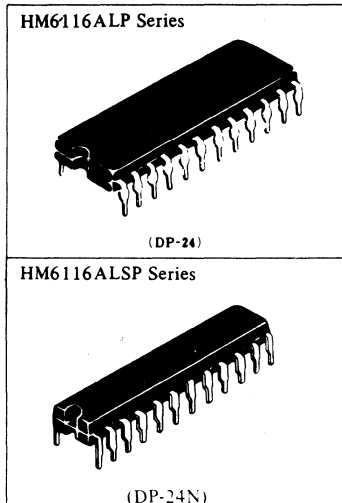
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_T	-0.5* to +7.0	V
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{sib}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

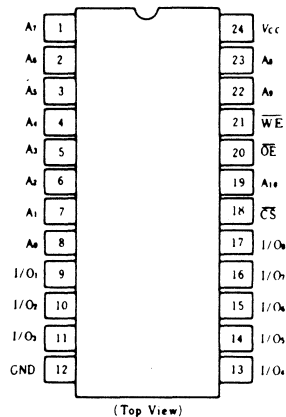
* Pulse Width 50ns : -3.5V

■ TRUTH TABLE

CS	OE	WE	Mode	V_{cc} Current	I/O Pin	Ref. Cycle
H	x	x	Not Selected	I_{sa}, I_{sb}	High Z	
L	L	H	Read	I_{cc}	Dout	Read Cycle (1)~(3)
L	H	L	Write	I_{cc}	Din	Write Cycle (1)
L	L	L	Write	I_{cc}	Din	Write Cycle (2)



■ PIN ARRANGEMENT



RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	3.5	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width 50ns, DC: V_{IL} min = -0.3V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, GND = 0V, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	HM6116ALP/ ALSP-12			HM6116ALP/ ALSP-15			HM6116ALP/ ALSP-20			Unit
			min	typ*	max	min	typ*	max	min	typ*	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND}$ to V_{CC}	-	-	2	-	-	2	-	-	2	μA
Output Leakage Current	I_{LO}	$\overline{\text{CS}}=V_{IH}$ or $\text{OE}=V_{IH}$, $V_{I/O}=\text{GND}$ to V_{CC}	-	-	2	-	-	2	-	-	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}$, $I_{I/O}=0\text{mA}$ $V_{in}=V_{IH}$ or V_{IL}	-	4	12	-	4	12	-	4	12	mA
	I_{CC1}	$V_{IH}=V_{CC}$, $V_{IL}=0\text{V}$ $\overline{\text{CS}}=V_{IL}$, $I_{I/O}=0\text{mA}$, $f=1\text{MHz}$	-	2	5	-	2	5	-	2	5	mA
Average Operating Current	I_{CC2}	min. cycle, duty = 100%	-	30	50	-	20	40	-	15	30	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	-	0.5	3	-	0.5	3	-	0.5	3	mA
	I_{SB1}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}$	-	1	50	-	1	50	-	1	50	μA
Output Voltage	V_{OL}	$I_{OL}=4\text{mA}$	-	-	0.4	-	-	0.4	-	-	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	-	-	2.4	-	-	2.4	-	-	V

* $V_{CC}=5\text{V}$, $T_a=25^\circ\text{C}$

AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10 ns

Input and Output Timing Reference Levels: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

READ CYCLE

Item	Symbol	HM6116ALP/ ALSP-12		HM6116ALP/ ALSP-15		HM6116ALP/ ALSP-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	-	150	-	200	-	ns
Address Access Time	t_{AA}	-	120	-	150	-	200	ns
Chip Select Access Time	t_{ACS}	-	120	-	150	-	200	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	10	-	10	-	ns
Output Enable to Output Valid	t_{OE}	-	55	-	60	-	70	ns
Output Enable to Output in Low Z	t_{OLZ}	10	-	10	-	10	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	40	0	50	0	60	ns
Chip Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	-	15	-	20	-	ns

● WRITE CYCLE

Item	Symbol	HM6116ALP/ ALSP-12		HM6116ALP/ ALSP-15		HM6116ALP/ ALSP-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	70	—	90	—	120	—	ns
Address Valid to End of Write	t_{AW}	105	—	120	—	140	—	ns
Address Set Up Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	70	—	80	—	100	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Write to Output in High Z	t_{WOH}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	35	—	40	—	50	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	10	—	10	—	10	—	ns

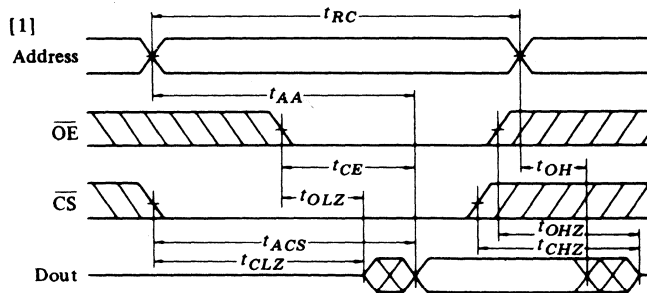
■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	typ	max	Unit
Input Capacitance	$C_{i.}$	$V_{i.} = 0\text{V}$	3	5	pF
Input/Output Capacitance	$C_{i.o}$	$V_{i.o} = 0\text{V}$	5	7	pF

Note) This parameter is sampled and not 100% tested.

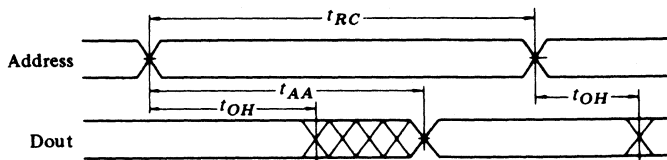
■ TIMING WAVEFORM

● Read Cycle (1)



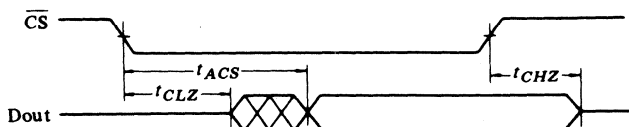
● Read Cycle (2)

[1], [2], [4]



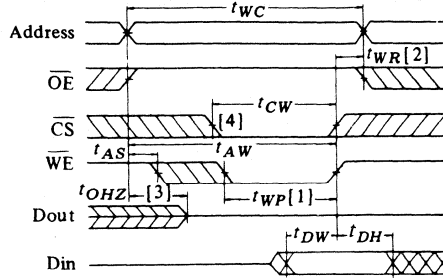
● Read Cycle (3)

[1], [3], [4]

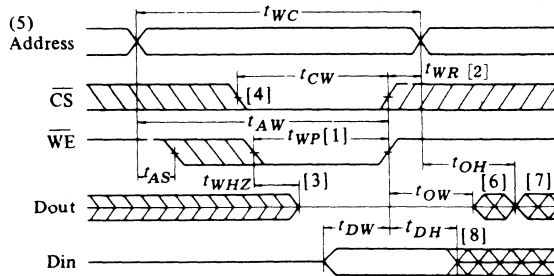


- NOTES: 1. \overline{WE} is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

● Write Cycle (1)



● Write Cycle (2)



- NOTES:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transitions or after the \overline{WE}

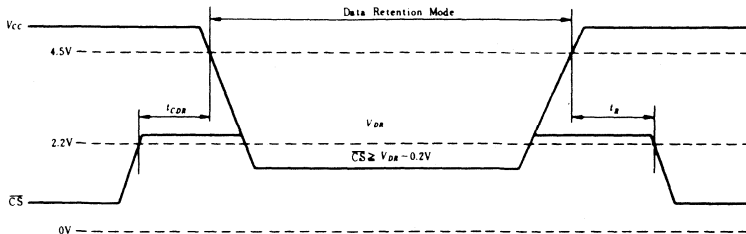
5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
6. D_{out} is the same phase of write data of this write cycle.
7. D_{out} is the read data of next address.
8. If \overline{CS} is Low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}^*	$V_{CC} = 3.0\text{V}$, $\overline{CS} \geq 2.8\text{V}$	—	—	30	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^{**}	—	—	—

* $10 \mu\text{A}$ max at $T_a = 0^\circ\text{C}$ to $+40^\circ\text{C}$, V_{IL} min = -0.3V
 ** t_R - Read Cycle Time.

● Low V_{CC} Data Retention Waveform

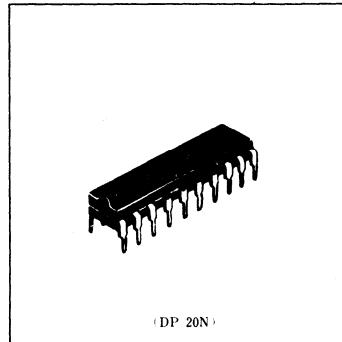


HM6168HP Series

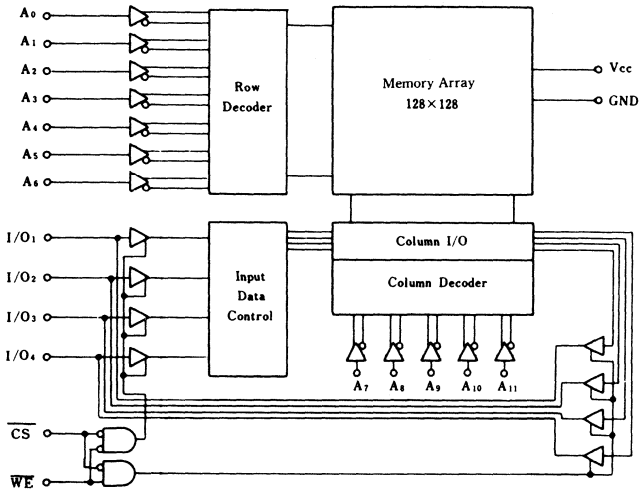
4096-word × 4-bit High Speed Static CMOS RAM

FEATURES

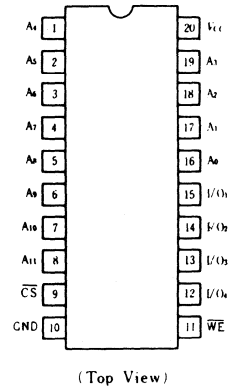
- High Speed: Fast Access Time 45/55/70 ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
100 μ W typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs



FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature (Ceramic)	T_{stc}	-65 to +150	°C
Storage Temperature (Plastic)	T_{stc}	-55 to +125	°C
Temperature under Bias	T_{bias}	-10 to +85	°C

* Pulse Width 20ns, DC - 0.5V

■ TRUTH TABLE

CS	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-3.0*	–	0.8	V

* Pulse width; 20 ns, DC; V_{IL} , min = -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $\text{GND}=0\text{V}$, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND to } V_{CC}$	–	–	2.0	μA
Output Leakage Current	I_{LO}	$\text{CS}=V_{IH}$, $V_{I/O}=\text{GND to } V_{CC}$	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\text{CS}=V_{IL}$, $I_{I/O}=0\text{mA}$	–	40	90	mA
Standby Power Supply Current	I_{SB}	$\text{CS}=V_{IH}$	–	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\text{CS}=V_{CC}-0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	–	0.02	2.0	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	–	–	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4\text{mA}$	2.4	–	–	V

Note: Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

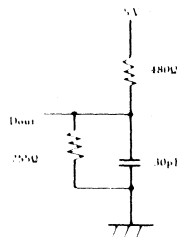
Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	$V_{IN}=0\text{V}$		6	pF^*
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$		8	pF^*

Note: * This parameters are sampled and not 100% tested.

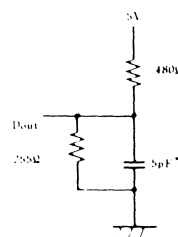
■ AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$, unless otherwise noted.)

● AC TEST CONDITION

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 5ns
- Input and Output timing reference levels: 1.5V
- Output load: See Figure



Output Load (A)



Output Load (B)

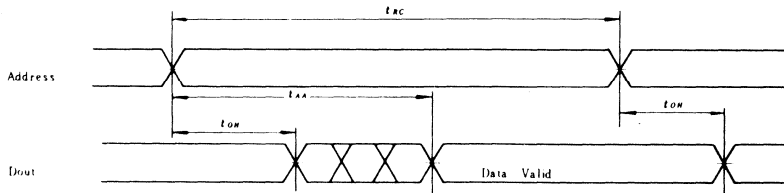
* Including scope and jig. (for t_{HZ} , t_{LZ} , t_{WZ} , t_{OW})

● READ CYCLE

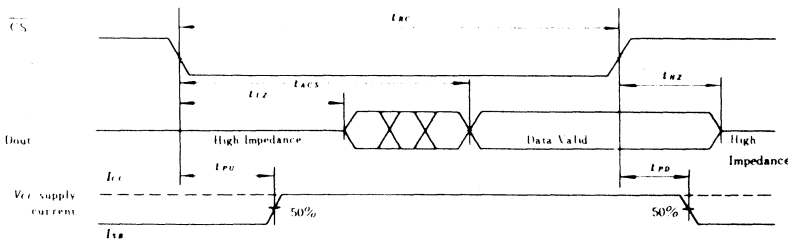
Item	Symbol	HM6168HP-45		HM6168HP-55		HM6168HP-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	—	55	—	70	—	ns
Address Access Time	t_{AA}	—	45	—	55	—	70	ns
Chip Select Access Time	t_{ACS}	—	45	—	55	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	—	20	—	20	—	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	—	30	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1^{(1), (2)}



● TIMING WAVEFORM OF READ CYCLE NO. 2^{(1), (3)}



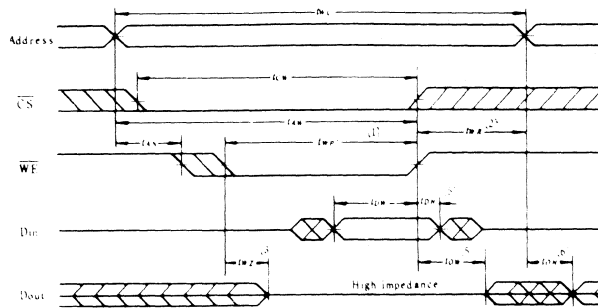
- Notes) 1. \overline{WE} is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with \overline{CS} transition Low.

● WRITE CYCLE

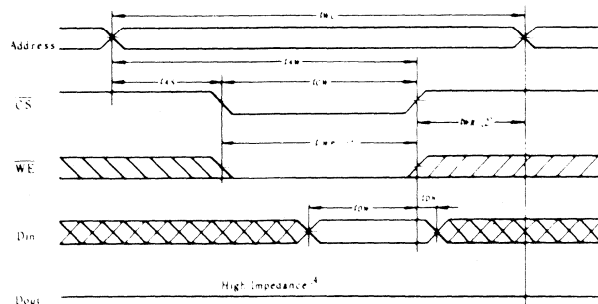
Item	Symbol	HM6168HP-45		HM6168HP-55		HM6168HP-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	—	55	—	70	—	ns
Chip Selection to End of Write	t_{CW}	40	—	50	—	60	—	ns
Address Valid to End of Write	t_{AW}	40	—	50	—	60	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	45	—	55	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	20	—	25	—	30	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	0	—	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ Controlled)

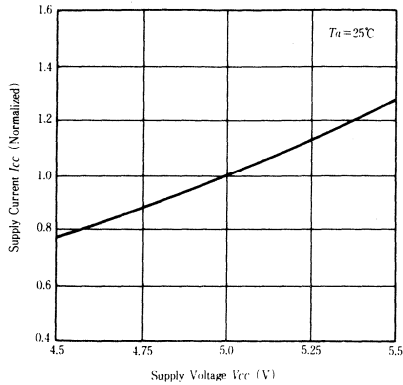


● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ Controlled)

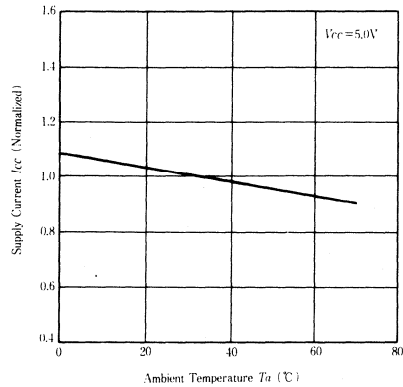


- Notes) 1. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$. (t_{WP})
 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition, the output buffer buffers remain in a high impedance state.
 5. If $\overline{\text{CS}}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 6. Dout is the same phase of Write data of this write cycle.

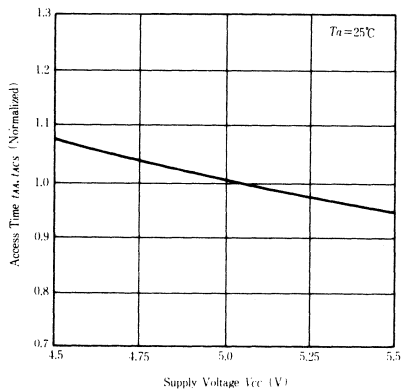
SUPPLY CURRENT VS. SUPPLY VOLTAGE



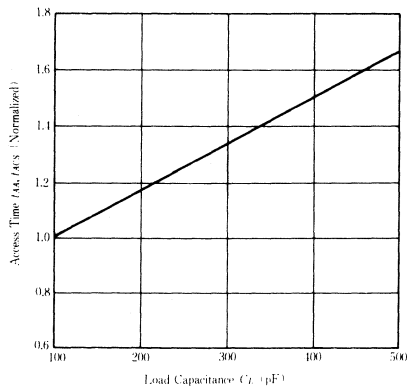
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



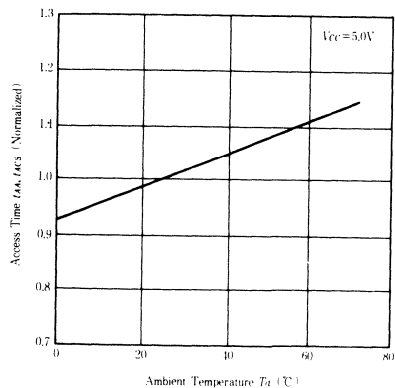
ACCESS TIME VS. SUPPLY VOLTAGE



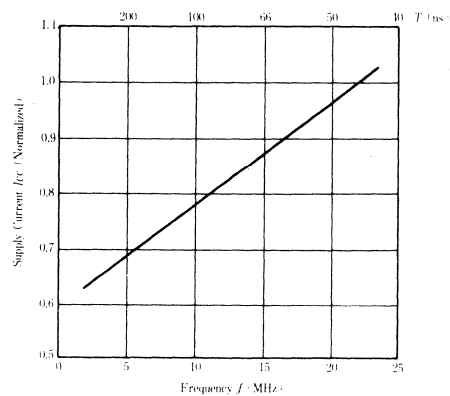
ACCESS TIME VS. LOAD CAPACITANCE



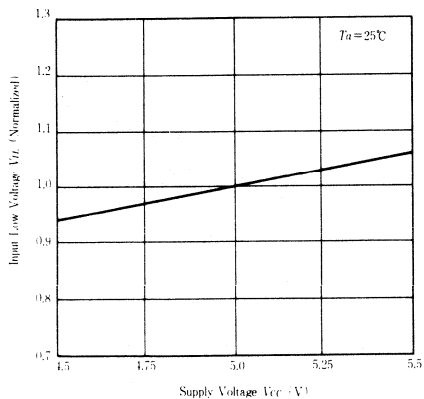
ACCESS TIME VS. AMBIENT TEMPERATURE



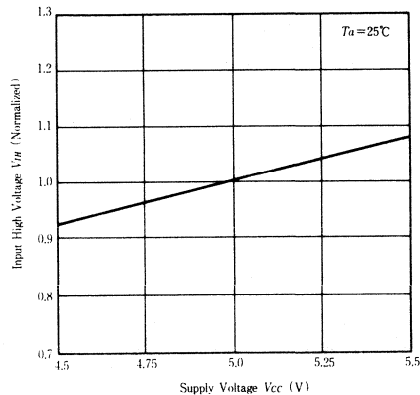
SUPPLY CURRENT VS. FREQUENCY



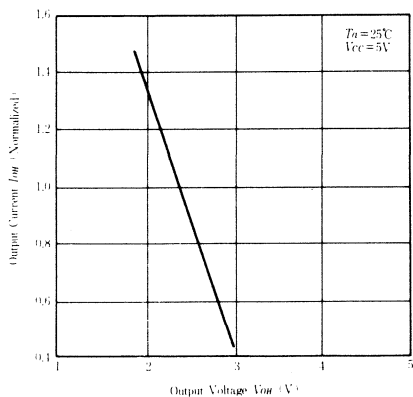
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



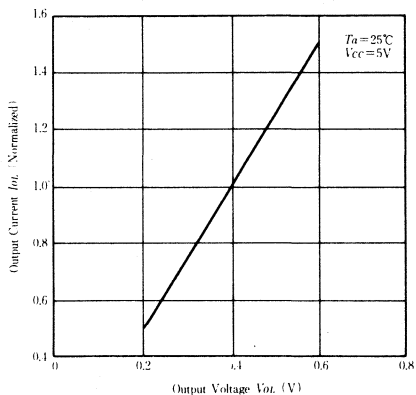
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



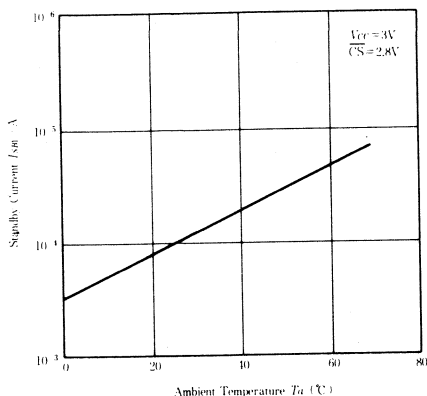
OUTPUT CURRENT VS. OUTPUT VOLTAGE



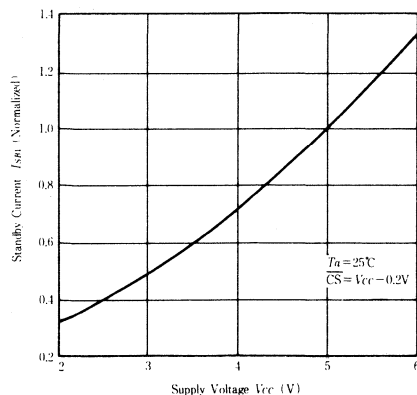
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



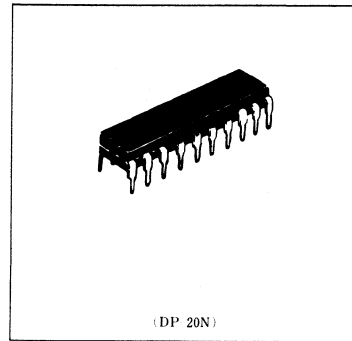
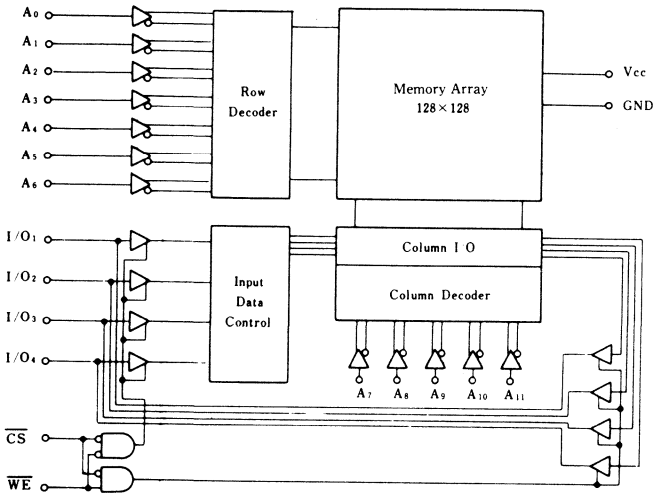
HM6168HLP Series

4096-word × 4-bit High Speed Static CMOS RAM

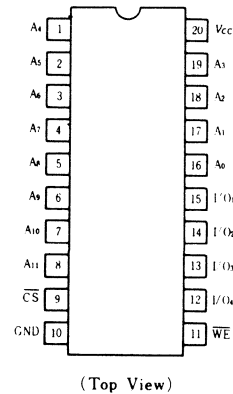
FEATURES

- High Speed: Fast Access Time 45/55/70ns (max.)
- Single +5V Supply and High Density 20 Pin Package
- Low Power Standby and Low Power Operation;
5μW typ. (Standby), 200mW typ. (Operation)
- Completely Static Memory
No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible—All Inputs and Outputs
- Capable of Battery back up Operation

FUNCTIONAL BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IV}	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{bias}	-10 to +85	°C

* Pulse Width 20ns, DC = -0.5V

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	Din	Write Cycle 1, 2

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse width; 20 ns, DC; V_{IL} min = -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $\text{GND}=0\text{V}$, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND to } V_{CC}$	-	-	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$, $V_{I/O}=\text{GND to } V_{CC}$	-	-	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0\text{mA}$	-	40	90	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	-	15	25	mA
Standby Power Supply Current(1)	I_{SB1}	$\overline{CS}=V_{CC}-0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	-	1	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	-	-	V

Note: Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}$ $f=1\text{MHz}$)

Item	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{in}	$V_{IN}=0\text{V}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	-	8	pF

Note: This parameters are sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$, unless otherwise noted)

● AC TEST CONDITIONS

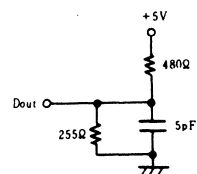
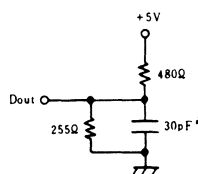
Input pulse levels: GND to 3.0V

Input rise and fall times: 5 ns

Input timing reference levels: 1.5V

Output reference levels: 1.5V

Output load: See Figure



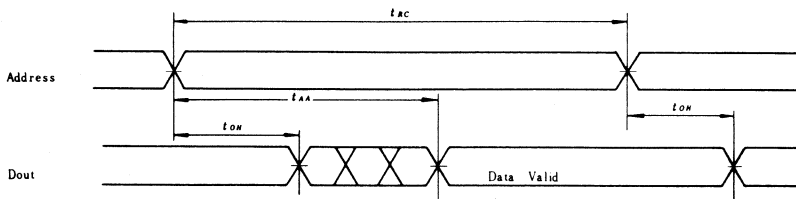
Output Load (A) * Including scope and jig. Output Load (B)
(for t_{HZ} , t_{LZ} , t_{WZ} , t_{OW})

● READ CYCLE

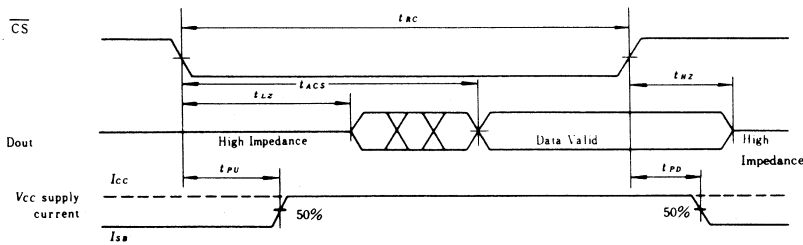
Item	Symbol	HM6168HLP-45		HM6168HLP-55		HM6168HLP-70		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	45	—	55	—	70	—	ns
Address Access Time	t_{AA}	—	45	—	55	—	70	ns
Chip Select Access Time	t_{ACS}	—	45	—	55	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z*	t_{LZ}	20	—	20	—	20	—	ns
Chip Deselection to Output in High Z*	t_{HZ}	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	—	30	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load (B).
 This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1^{(1), (2)}



● TIMING WAVEFORM OF READ CYCLE NO. 2^{(1), (3)}



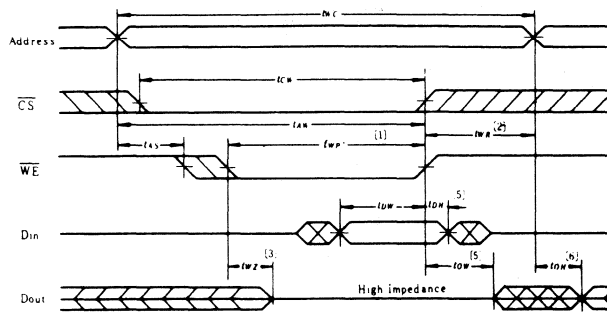
- Notes) 1. $\overline{\text{WE}}$ is High for Read Cycle.
 2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.
 3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low.

● WRITE CYCLE

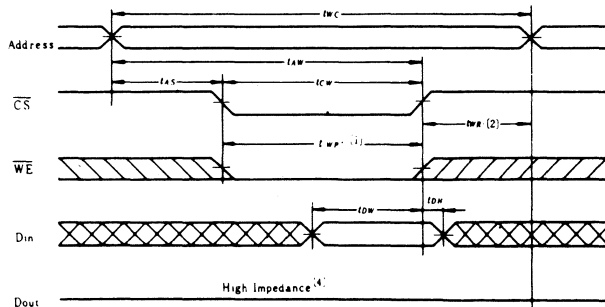
Item	Symbol	HM6168HLP-45		HM6168HLP-55		HM6168HLP-70		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	45	—	55	—	70	—	ns
Chip Selection to End of Write	t_{CW}	40	—	50	—	60	—	ns
Address Valid to End of Write	t_{AW}	40	—	50	—	60	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	35	—	45	—	55	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	20	—	25	—	30	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z*	t_{WZ}	0	15	0	20	0	25	ns
Output Active from End of Write*	t_{OW}	0	—	0	—	0	—	ns

* Transition is measured $\pm 500\text{mV}$ from steady state voltage with Load (B).
 This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 ($\overline{\text{WE}}$ Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 ($\overline{\text{CS}}$ Controlled)



- Notes) 1. A write occurs during the overlap of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$, (t_{WP})
 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ transition, the output buffer remains in a high impedance state.
 5. If $\overline{\text{CS}}$ is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 6. Dout is the same phase of Write data of this write cycle.

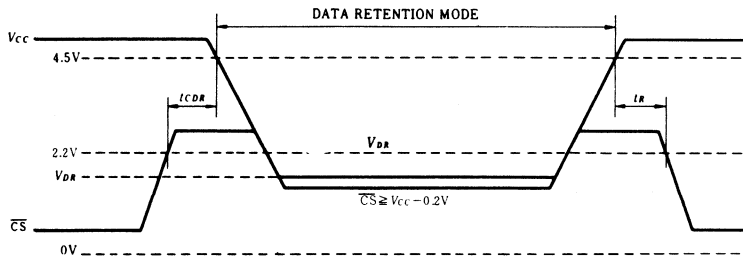
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$CS \geq V_{CC} - 0.2V$ $V_{in} \geq V_{CC} - 0.2V$ or $0V \leq V_{in} \leq 0.2V$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		$t_{RC(1)}$	—	—	ns

Note: 1. t_{RC} —Read Cycle Time.

* $V_{CC}=3.0V$
** $V_{CC}=2.0V$

● LOW V_{CC} DATA RETENTION WAVEFORM

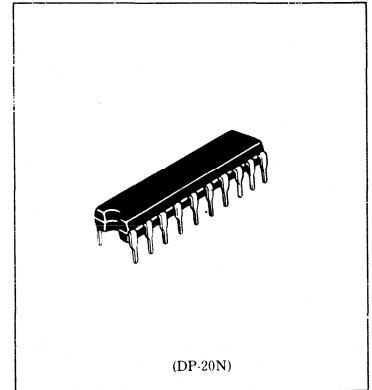
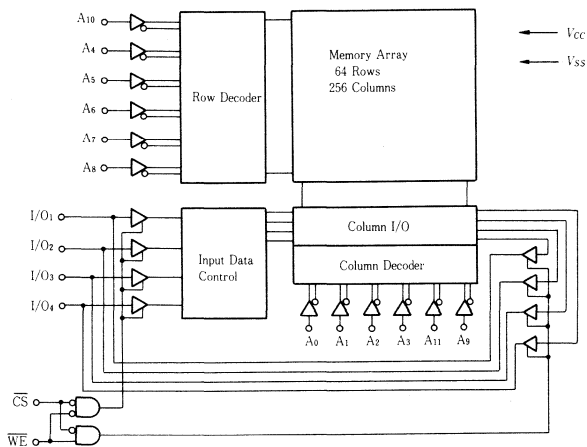


4096-word x 4-bit High Speed Static CMOS RAM

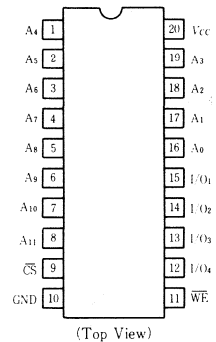
■ FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35ns (max.)
- Low Power Standby and Low Power Operation
100 μ W typ. (Standby), 250mW typ. (Op.).
- Completely Static Memory: No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{bys}	-10 to +85	°C

* Pulse Width 20ns, DC = -0.5V

(Top View)

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

RECOMMENDED OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

* Pulse width 10ns, DC: -0.5V

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $\text{GND}=0\text{V}$, $T_a=0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=\text{MAX. } V_{in}=\text{GND to } V_{CC}$	—	—	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}, V_{I/O}=\text{GND to } V_{CC}$	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}, I_{I/O}=0\text{mA}$	—	50	90	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	15	25	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}, V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC}-0.2\text{V}$	—	0.02	1.0	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

Note: 1. Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^\circ\text{C}$ and specified loading

CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1.0\text{MHz}$)

Parameter	Svmbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	$V_{IN}=0\text{V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	—	9	pF

Note: This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$, unless otherwise noted.)

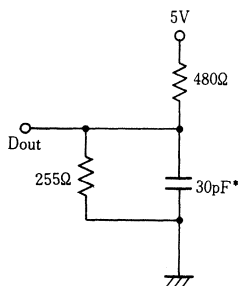
AC Test Conditions

Input pulse levels: GND to 3.0V

Input rise and fall times: 5ns

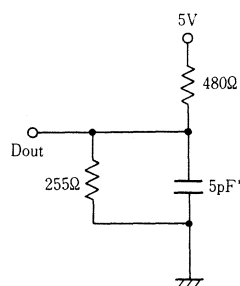
Input and Output timing reference levels: 1.5V

Output load: See Figure



* Including scope and jig.

Output Load (A)



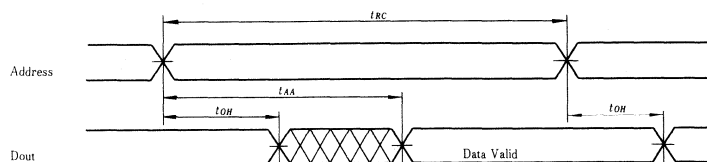
Output Load (B)
(for t_{HZ} , t_{LZ} , t_{WZ} & t_{OW})

● READ CYCLE

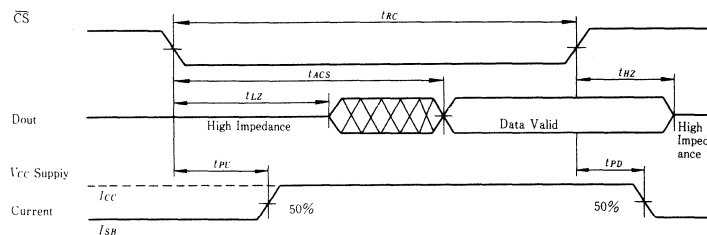
Parameter	Symbol	HM6268P-25		HM6268P-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}^*	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}^*	0	15	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1^{(1),(2)}



● Timing Waveform of Read Cycle No. 2^{(1),(3)}



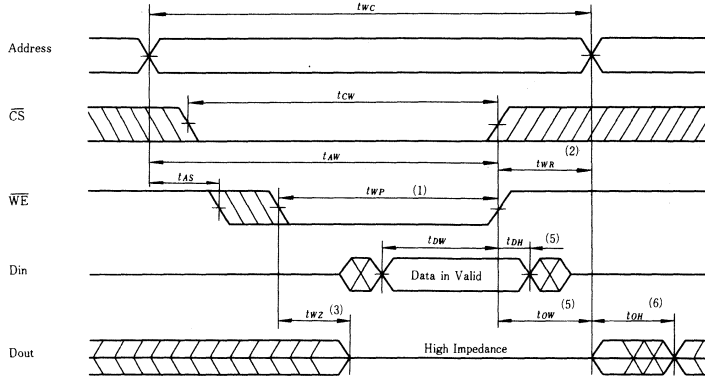
- Notes: 1. \overline{WE} is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with \overline{CS} transition Low.

● WRITE CYCLE

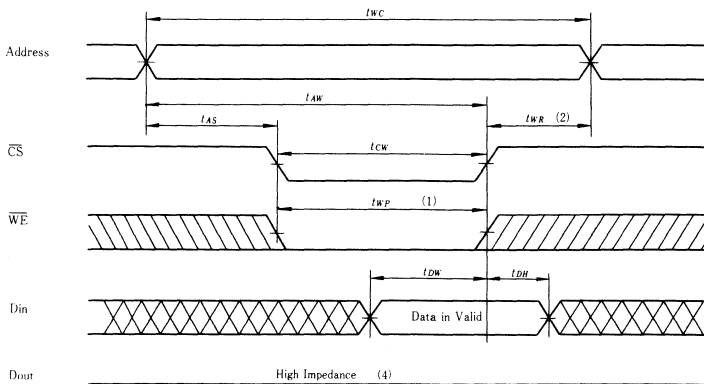
Parameter	Symbol	HM6268P-25		HM6268P-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}^*	0	8	0	10	ns
Output Active from End of Write	t_{OW}^*	0	—	0	—	ns

* Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled)



● Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled)



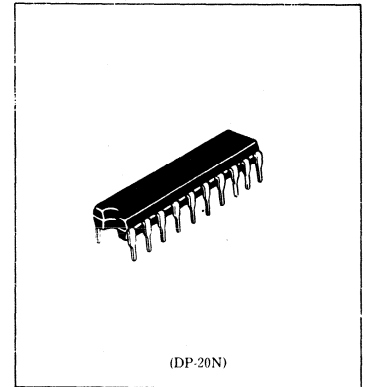
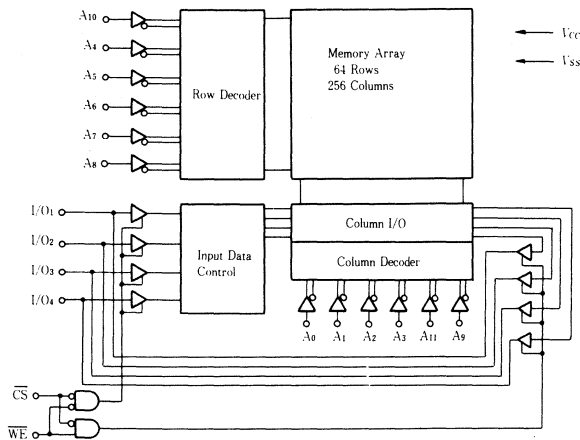
- Notes:
1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . (t_{WPP}).
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output buffers remain in a high impedance state.
 5. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 6. D_{out} is the same phase of write data of this write cycle.

4096-word x 4-bit High Speed Static CMOS RAM

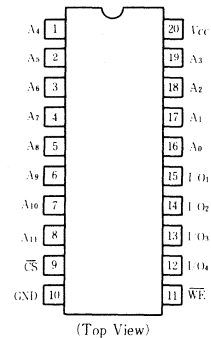
FEATURES

- Single 5V Supply and High Density 20 Pin Package.
- High Speed: Fast Access Time 25/35ns (max.)
- Low Power Standby and Low Power Operation
5 μ W typ. (Standby), 250mW typ. (Op.).
- Completely Static Memory: No Clock or Timing
Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible – All Inputs and Outputs
- Capable of Battery Back Up Operation

BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{bys}	-10 to +85	°C

* Pulse Width 20ns, DC - -0.5V

TRUTH TABLE

CS	WE	Mode	Vcc Current	I/O Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{cc}	Dout	Read Cycle
L	L	Write	I_{cc}	Din	Write Cycle

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications

■ RECOMMENDED OPERATING CONDITIONS ($T_a=0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

* Pulse width 10ns, [DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $\text{GND}=0\text{V}$, $T_a=0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=\text{MAX. } V_{in}=\text{GND to } V_{CC}$	—	—	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}=V_{IH}, V_{I/O}=\text{GND to } V_{CC}$	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}=V_{IL}, I_{I/O}=0\text{mA}$	—	50	90	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}=V_{IH}$	—	15	25	mA
Standby Power Supply Current (I)	I_{SB1}	$\overline{\text{CS}} \geq V_{CC}-0.2\text{V}, V_{IS} \leq 0.2\text{V}$ or $V_{IS} \geq V_{CC}-0.2\text{V}$	—	1.0	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

Note: 1. Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^{\circ}\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IX}	$V_{IX}=0\text{V}$	—	6	pF
Input /Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	—	9	pF

Note: This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC}=5\text{V} \pm 10\%$, $T_a=0$ to $+70^{\circ}\text{C}$, unless otherwise noted.)

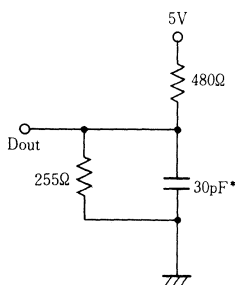
● AC Test Conditions

Input pulse levels: GND to 3.0V

Input rise and fall times: 5ns

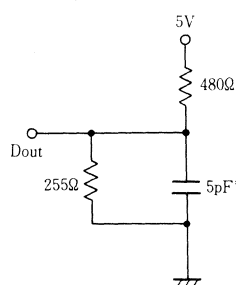
Input and Output timing reference levels: 1.5V

Output load: See Figure



* Including scope and jig.

Output Load (A)



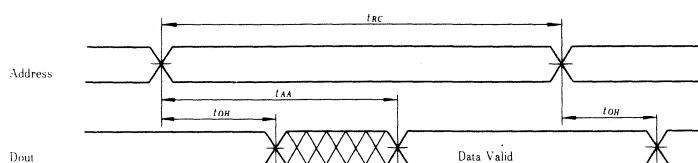
Output Load (B)
(for t_{HZ} , t_{LZ} , t_{WZ} & t_{OW})

● READ CYCLE

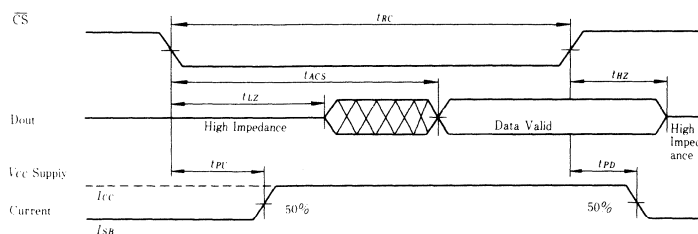
Parameter	Symbol	HM6268LP-25		HM6268LP-35		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	25	—	35	—	ns
Address Access Time	t_{AA}	—	25	—	35	ns
Chip Select Access Time	t_{ACS}	—	25	—	35	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}^*	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}^*	0	15	0	20	ns
Chip Selection to Power Up Time	t_{PC}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	25	—	25	ns

* Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Read Cycle No. 1^{(1),(2)}



● Timing Waveform of Read Cycle No. 2^{(1),(3)}



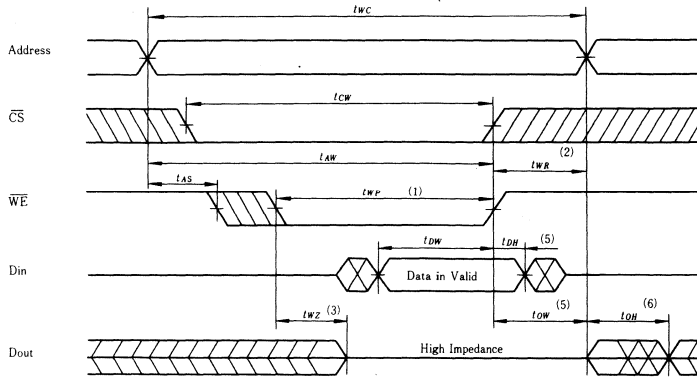
- Notes: 1. \overline{CS} is High for Read Cycle.
2. Device is continuously selected, $\overline{CS} = V_{IL}$.
3. Address Valid prior to or coincident with \overline{CS} transition Low.

● WRITE CYCLE

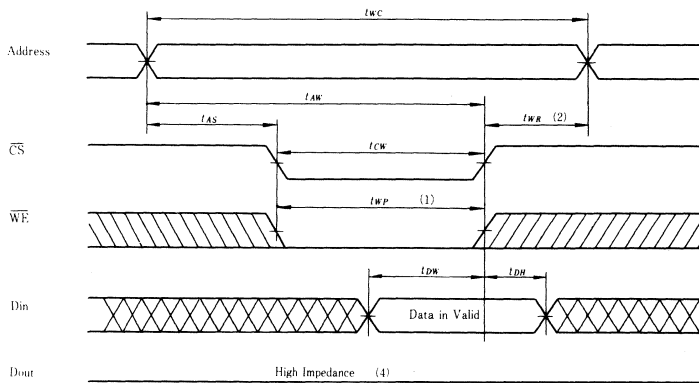
Parameter	Symbol	HM6268LP-25		HM6268LP-35		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	25	—	35	—	ns
Chip Selection to End of Write	t_{CW}	20	—	30	—	ns
Address Valid to End of Write	t_{AW}	20	—	30	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Write Pulse Width	t_{WP}	20	—	30	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	12	—	20	—	ns
Data Hold Time	t_{DH}	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}^*	0	8	0	10	ns
Output Active from End of Write	t_{OW}^*	0	—	0	—	ns

* Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled)



● Timing Waveform of Write Cycle No. 2 (\overline{CS} Controlled)



- Notes:
1. A write occurs during the overlap of a low \overline{CS} and a low \overline{WE} . (t_{wp}).
 2. t_{wh} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} transition, the output buffers remain in a high impedance state.
 5. If \overline{CS} is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 6. D_{out} is the same phase of write data of this write cycle.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

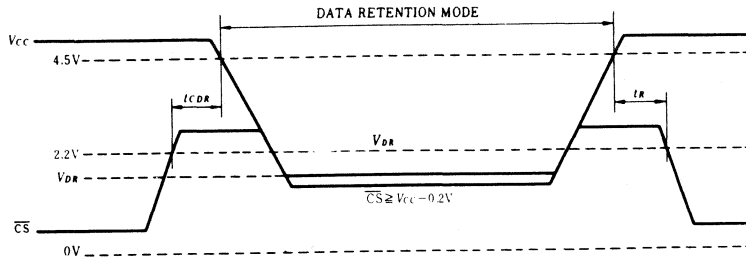
Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{in} \geq V_{CC} - 0.2\text{V}$ or	2.0	—	—	V
Data Retention Current	I_{CCDR}		$0\text{V} \leq V_{in} \leq 0.2\text{V}$	—	—	30* 20**
Chip Deselect to Data Retention Time	t_{CDR}	$0\text{V} \leq V_{in} \leq 0.2\text{V}$	0	—	—	ns
Operation Recovery Time	t_R		$t_{RC(1)}$	—	—	—

Note: 1. t_R - Read Cycle Time.

* $V_{CC} = 3.0\text{V}$

** $V_{CC} = 2.0\text{V}$

● LOW V_{CC} DATA RETENTION WAVEFORM

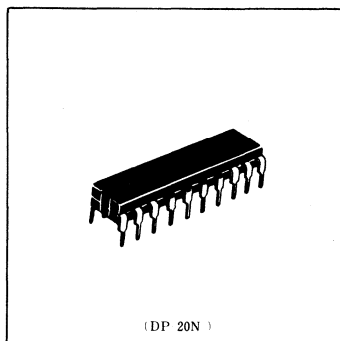


HM6167P Series

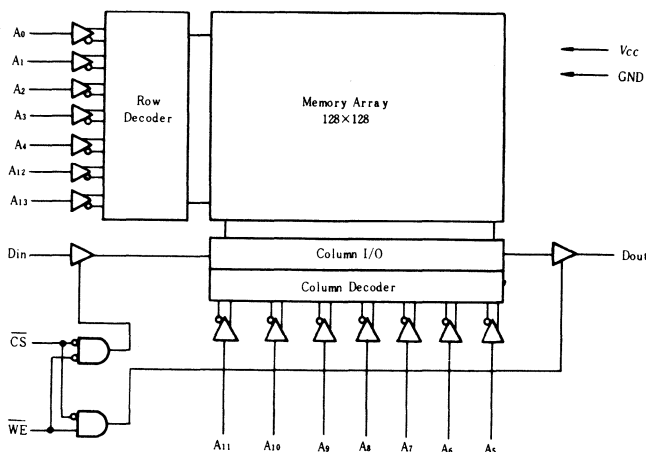
16384-word × 1-bit High Speed Static CMOS RAM

FEATURES

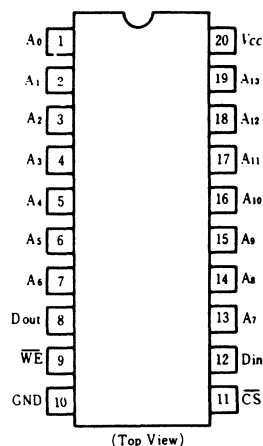
- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time – 85ns/100ns
- Low Power Stand-by and Low Power Operation
Stand-by 100μW Typ. and Operating 150mW Typ.
- Completely Static Memory No Clock nor Refresh Required
- Fully TTL Compatible – All Inputs and Output
- Separate Data Input and Output Three State Output
- Pin-Out Compatible with Intel 2167 Series



BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	-0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature**	$T_{stg}(bias)$	-10 to +85	°C

* Pulse width 20ns : -3.5V **under bias

RECOMMENDED DC OPERATING CONDITIONS

(0 °C ≤ T_a ≤ 70 °C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-3.0*	—	0.8	V

* Pulse width 20ns, DC : V_{IL} min = -0.3V

TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0^\circ\text{C}$ to $+70^\circ\text{C}$)

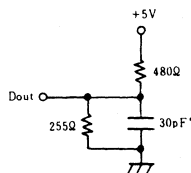
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V$, $V_{IN}=0V \sim V_{CC}$	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$, $V_{OUT}=0V \sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{L}$, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	20	mA
	I_{SB1}	$\overline{CS}=V_{CC}-0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	0.02	2	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4\text{mA}$	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $T_a=25^\circ\text{C}$ and specified loading.

AC TEST CONDITIONS

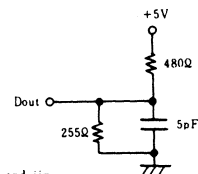
Input pulse levels: GND to 3.0V
 Input rise and fall times: 5 ns
 Input timing reference levels: 1.5V
 Output reference levels: 1.5V
 Output load: See Figure

Output Load A



Output Load B

(for t_{HZ} , t_{LZ} , t_{wz} & t_{ow})



* Including scope and jig.

CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1.0\text{MHz}$)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	6	pF	$V_{OUT}=0V$

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0^\circ\text{C}$ to 70°C , unless otherwise noted.)

READ CYCLE

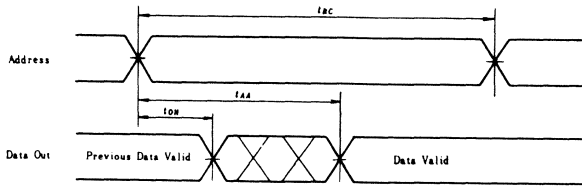
Item	Symbol	HM6167P-6		HM6167P-8		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	85	—	100	—	ns
Address Access Time	t_{AA}	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	40	—	45	ns

● WRITE CYCLE

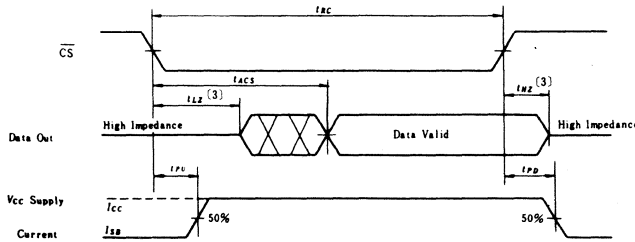
Item	Symbol	HM6167P-6		HM6167P-8		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

- Notes) 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance state.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO.1¹⁾

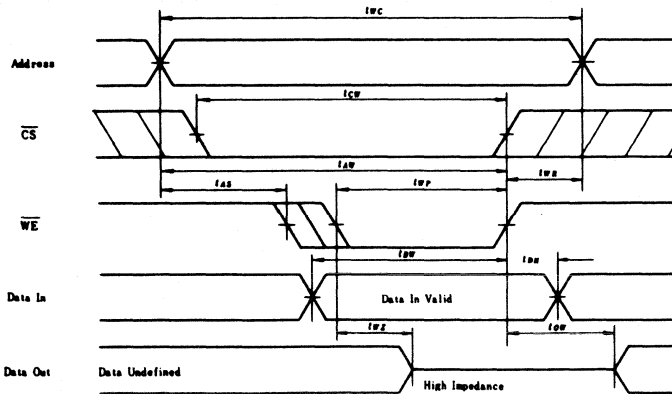


● TIMING WAVEFORM OF READ CYCLE NO.2^{1), 3)}



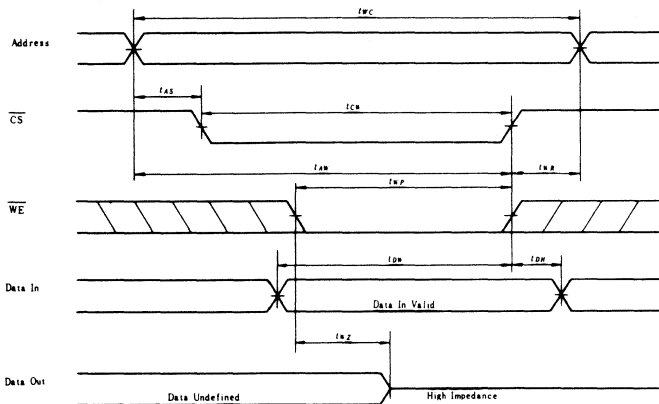
- NOTES: 1. \overline{WE} is high and \overline{CS} is low for READ cycle.
 2. Addresses valid prior to or coincident with \overline{CS} transition low.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 (\overline{WE} Controlled)



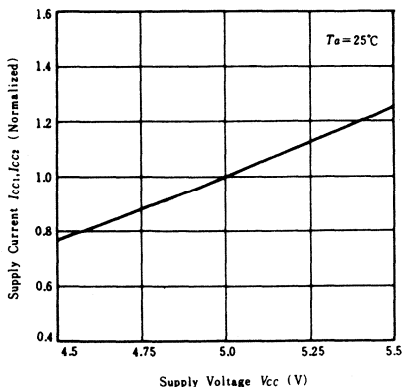
NOTE: 1. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE No. 2 (\overline{CS} Controlled)

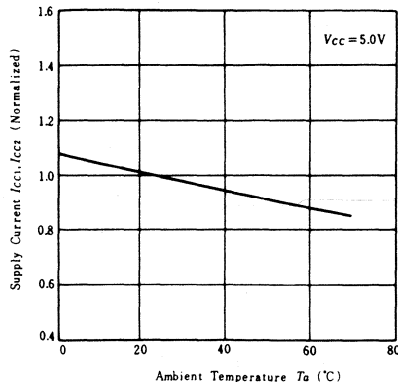


Note) Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

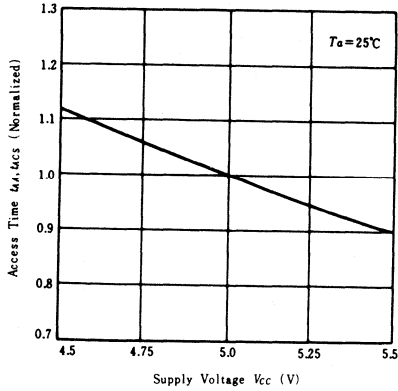
SUPPLY CURRENT vs. SUPPLY VOLTAGE



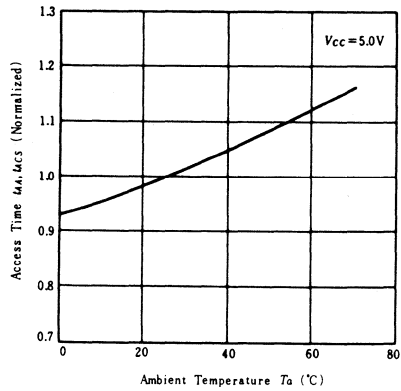
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



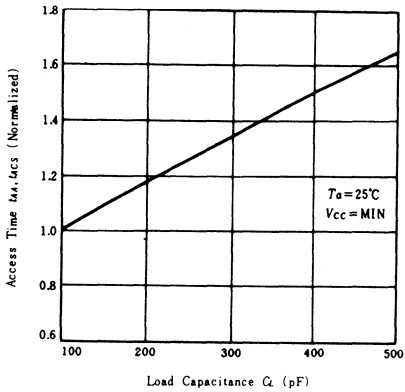
ACCESS TIME vs. SUPPLY VOLTAGE



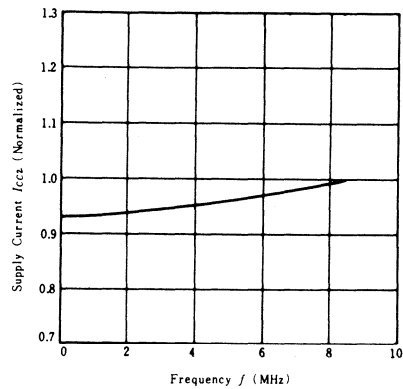
ACCESS TIME vs. AMBIENT TEMPERATURE



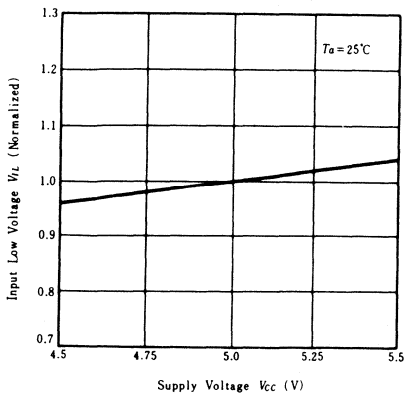
ACCESS TIME vs. LOAD CAPACITANCE



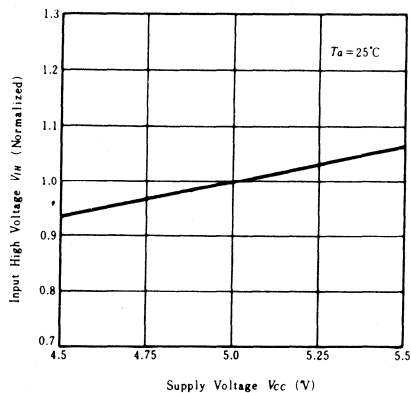
SUPPLY CURRENT vs. FREQUENCY



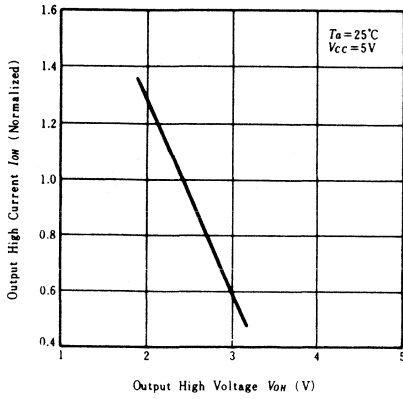
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



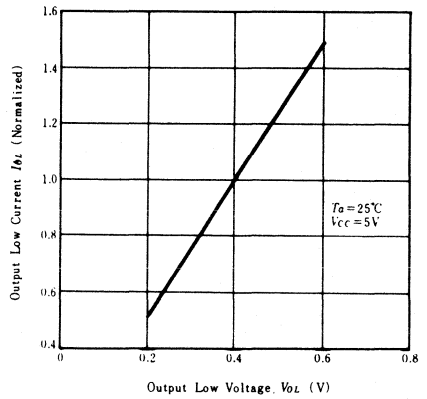
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



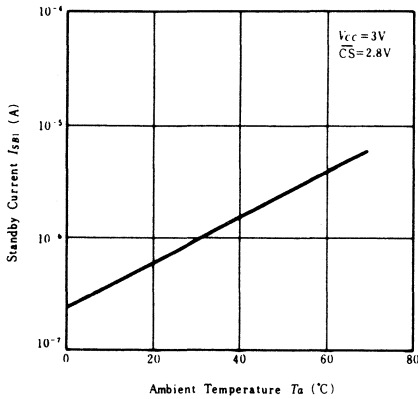
**OUTPUT HIGH CURRENT vs.
OUTPUT HIGH VOLTAGE**



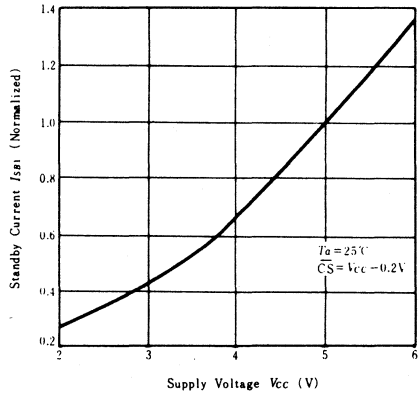
**OUTPUT LOW CURRENT vs.
OUTPUT LOW VOLTAGE**



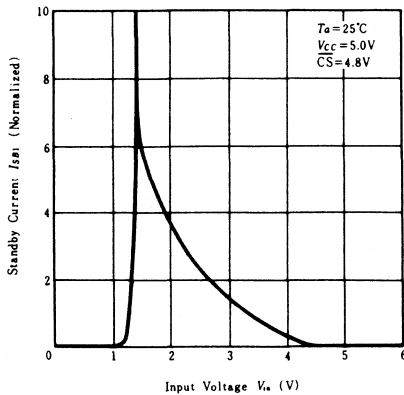
**STANDBY CURRENT vs.
AMBIENT TEMPERATURE**



**STANDBY CURRENT vs.
SUPPLY VOLTAGE**



**STANDBY CURRENT vs.
INPUT VOLTAGE**



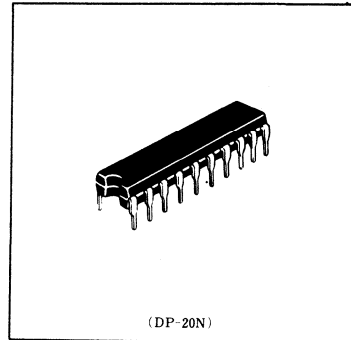
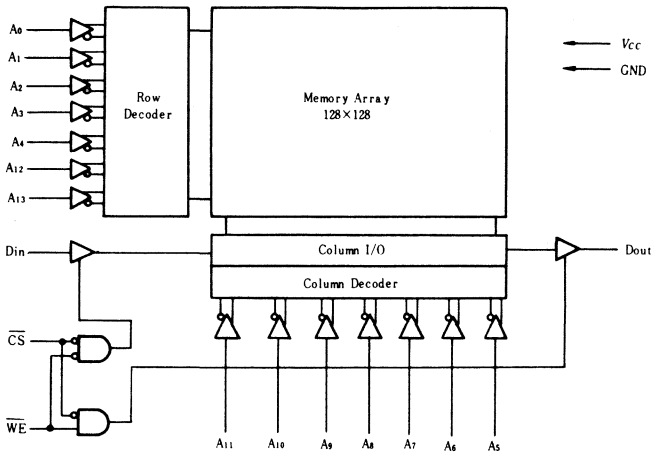
HM6167LP Series

16384-word × 1-bit High Speed Static CMOS RAM

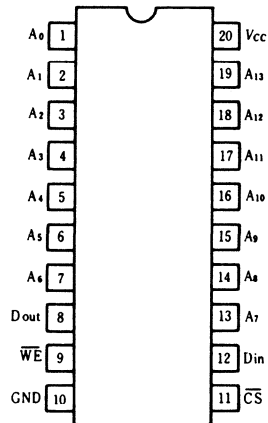
FEATURES

- Single +5V Supply and High Density 20 Pin Package
- Fast Access Time 85ns/100ns
- Low Power Stand-by and Low Power Operation
Stand-by 5μW (typ) and Operating 150mW (typ.)
- Completely Static Memory. No Clock or Refresh Required
- Fully TTL Compatible. All Inputs and Output
- Separate Data Input and Output Three State Output
- Capable of Battery Back up Operation

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to GND	V_T	-0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature**	$T_{stg(bias)}$	-10 to +85	°C

* Pulse width 20ns - 3.5V ** under bias

RECOMMENDED DC OPERATING CONDITIONS (0 °C ≤ T_a ≤ 70 °C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-3.0*	—	0.8	V

* Pulse width 20ns, DC; V_{IL} min = -0.3V

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	Output Pin	Reference Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	
L	H	Read	I_{CC}	Dout	Read Cycle 1, 2
L	L	Write	I_{CC}	High Z	Write Cycle 1, 2

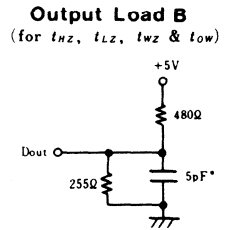
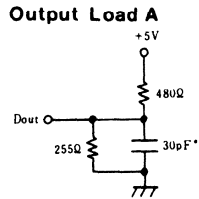
■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0 \sim +70^\circ C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V$ $V_{IN}=0V \sim V_{CC}$	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$, $V_{OI}=0V \sim V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{LL}$, Output Open	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	5	20	mA
	I_{SB1}	$\overline{CS}=V_{CC}-0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	1	50	μA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $T_a=25^\circ C$ and specified loading.

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
 Input rise and fall times: 5 ns
 Input timing reference levels: 1.5V
 Output reference levels: 1.5V
 Output load: See Figure



* Including scope and jig.

■ CAPACITANCE ($T_a=25^\circ C$, $f=1.0MHz$)

Item	Symbol	max	Unit	Conditions
Input Capacitance	C_{IN}	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	6	pF	$V_{OUT}=0V$

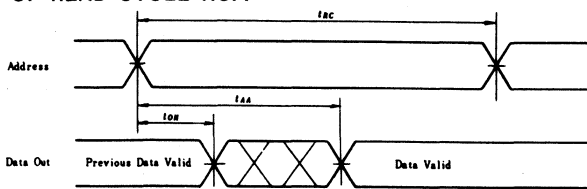
Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($T_a=0^\circ C$ to $+70^\circ C$, $V_{CC}=5V \pm 10\%$, unless otherwise noted.)

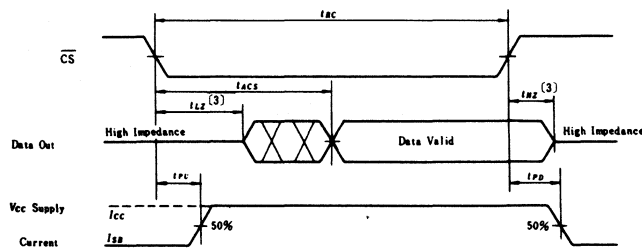
● READ CYCLE

Item	Symbol	HM6167LP-6		HM6167LP-8		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	85	—	100	—	ns
Address Access Time	t_{AA}	—	85	—	100	ns
Chip Select Access Time	t_{ACS}	—	85	—	100	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{HZ}	0	40	0	40	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	40	—	45	ns

● TIMING WAVEFORM OF READ CYCLE NO.1 ¹⁾



● TIMING WAVEFORM OF READ CYCLE NO.2 ^{1), 3)}



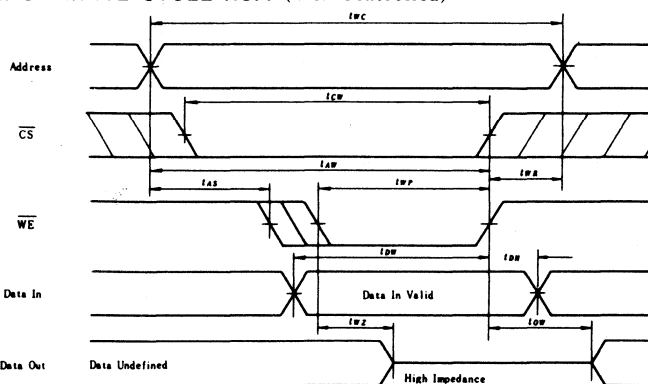
- NOTES: 1. \overline{WE} is high and \overline{CS} is low for READ Cycle.
 2. Addresses valid prior to or coincident with \overline{CS} transition low.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading B.

● WRITE CYCLE

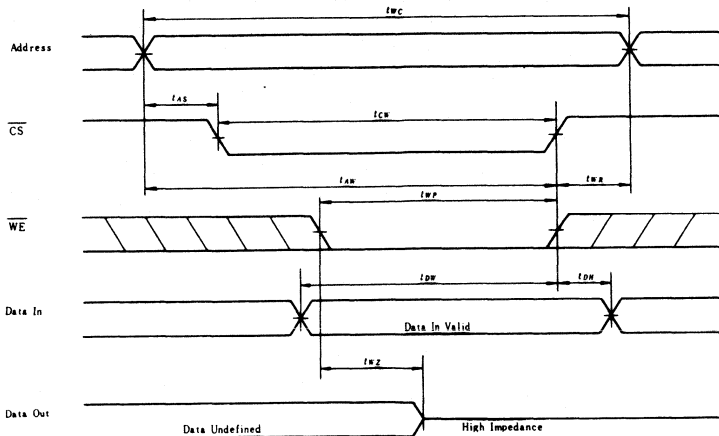
Item	Symbol	HM6167LP-6		HM6167LP-8		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	85	—	100	—	ns	2
Chip Selection to End of Write	t_{CW}	65	—	80	—	ns	
Address Valid to End of Write	t_{AW}	65	—	80	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	45	—	55	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	35	—	40	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enable to Output in High Z	t_{WZ}	0	40	0	40	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

- Notes) 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance state.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO.1 (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE No. 2 (\overline{CS} Controlled)



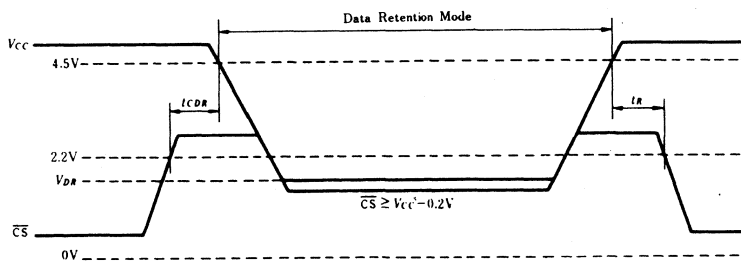
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a=0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{i.s} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{i.s} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*	μA
			—	—	30**	
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^Δ	—	—	ns

Δt_{RC} —Read Cycle Time

* $V_{CC}=2.0\text{V}$
** $V_{CC}=3.0\text{V}$

■ LOW V_{CC} DATA RETENTION WAVEFORM



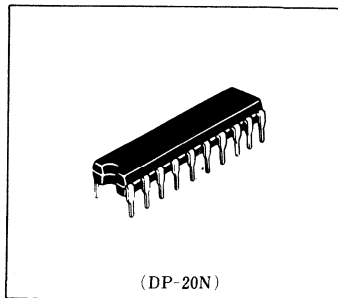
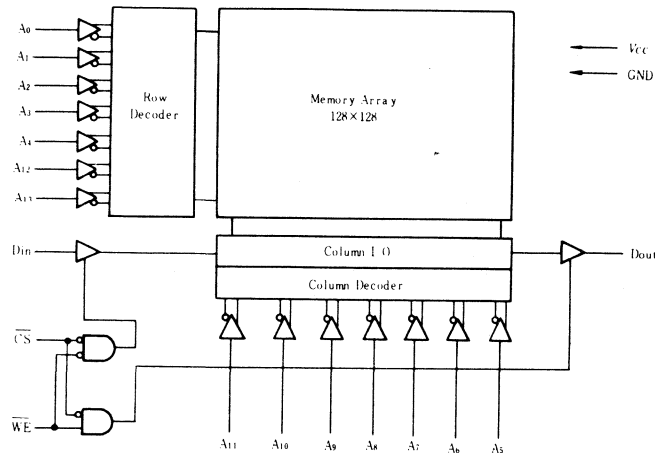
HM6167HP Series

16384-word x 1-bit High Speed Static CMOS RAM

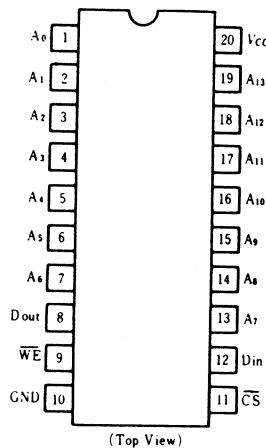
■ FEATURES

- Fast Access Time. HM6167HP-55 55ns (max)
HM6167HP-70 70ns (max)
- Low Power Standby and Low Power Operation
Standby 100 μ W (typ), Operating 200mW (typ)
- Single +5V Supply and High Density 20 Pin Package
- Completely Static Memory No Clock nor Refresh Required
- Fully TTL Compatible All Inputs and Output
- Separate Data Input and Output. Three State Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C
Storage Temperature (under bias)	T_{bias}	-10 to +85	$^{\circ}$ C

* Pulse Width 20ns, DC: -0.5V

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70 $^{\circ}$ C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width: 20ns, DC: V_{IL} (min) = -0.5V

TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0^\circ C$ to $+70^\circ C$)

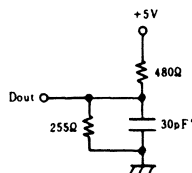
Item	Symbol	Test Conditions	HM6167HP-55			HM6167HP-70			Unit
			min	typ	max	min	typ	max	
Input Leakage Current	$ I_{LI} $	$V_{CC}=5.5V, V_{IN}=0V \sim V_{CC}$	—	—	2	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}, V_{OUT}=0V \sim V_{CC}$	—	—	2	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, Output Open	—	40	80	—	30	60	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	10	20	—	5	20	mA
	I_{SB1}	$\overline{CS} \geq V_{CC}-0.2V$ $V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC}-0.2V$	—	0.02	2	—	0.02	2	mA
Output Low Voltage	V_{OL}	$I_{OL}=8mA$	—	—	0.4	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4mA$	2.4	—	—	2.4	—	—	V

Note) Typical limits are at $V_{CC}=5.0V$, $T_a=25^\circ C$ and specified loading.

AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
 Input rise and fall times: 5 ns
 Input timing reference levels: 1.5V
 Output reference levels: 1.5V
 Output load: See Figure

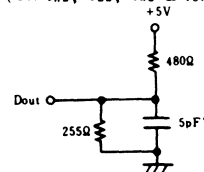
Output Load A



* Including scope and jig.

Output Load B

(for t_{wz} , t_{LZ} , t_{wz} & t_{ow})



* Including scope and jig.

CAPACITANCE ($T_a=25^\circ C$, $f=1.0MHz$)

Item	Symbol	typ	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	$V_{IN}=0V$
Output Capacitance	C_{OUT}	—	7	pF	$V_{OUT}=0V$

Note) This parameter is sampled and not 100% tested.

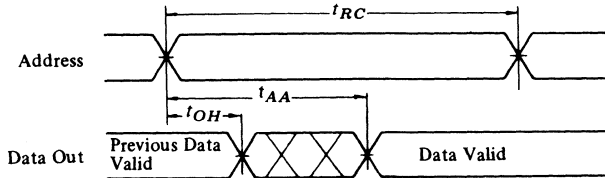
■ AC CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0^\circ\text{C}$ to 70°C , unless otherwise noted.)

● READ CYCLE

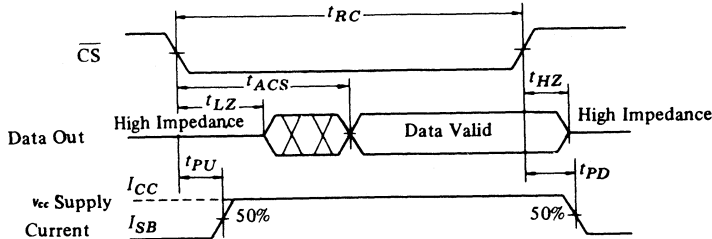
Item	Symbol	HM6167HP-55		HM6167HP-70		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	55	—	70	—	ns	(1)
Address Access Time	t_{AA}	—	55	—	70	ns	
Chip Select Access Time	t_{ACS}	—	55	—	70	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	(2) (3) (7)
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	35	ns	(2) (3) (7)
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	30	—	35	ns	

- NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is High for READ cycle.
 5. Device is continuously selected, $\overline{CS} = V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO.1 (4), 5)



● TIMING WAVEFORM OF READ CYCLE NO.2 (4), 6)

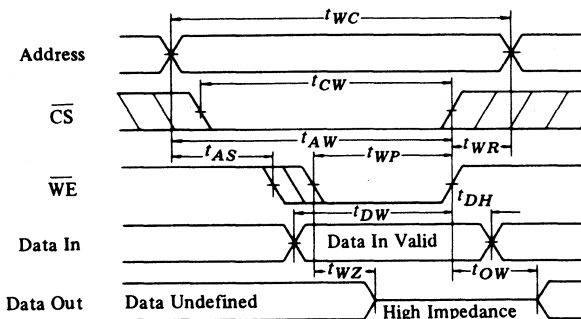


• WRITE CYCLE

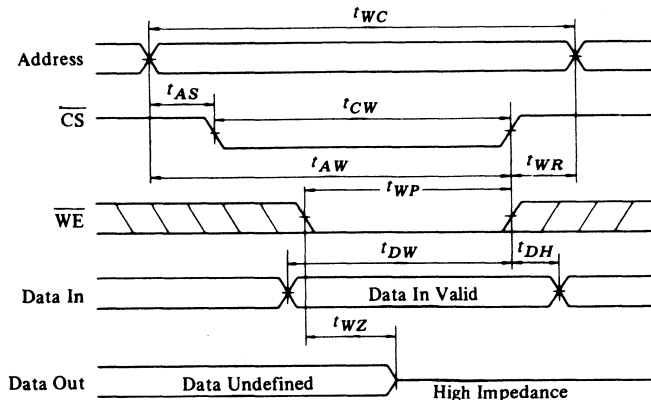
Item	Symbol	HM6167HP-55		HM6167HP-70		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	55	-	70	-	ns	(2)
Chip Selection to End of Write	t_{CW}	50	-	55	-	ns	
Address Valid to End of Write	t_{AW}	50	-	55	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	ns	
Write Pulse Width	t_{WP}	35	-	40	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	ns	
Data Valid to End of Write	t_{DW}	25	-	30	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	30	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	-	0	-	ns	(3) (4)

- NOTES: 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All write cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

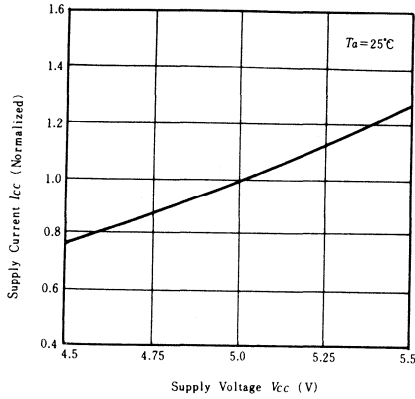
• TIMING WAVEFORM OF WRITE CYCLE (\overline{WE} Controlled)



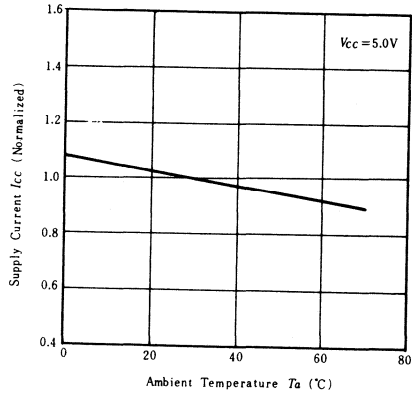
• TIMING WAVEFORM OF WRITE CYCLE (\overline{CS} Controlled)



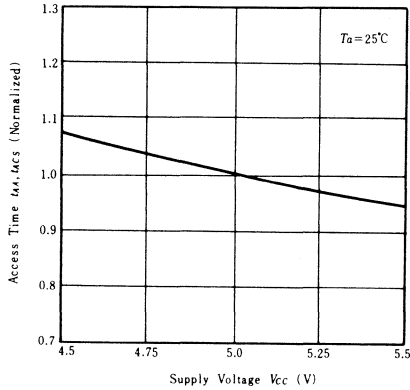
**SUPPLY CURRENT vs.
SUPPLY VOLTAGE**



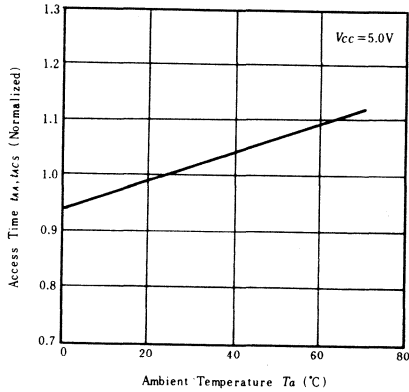
**SUPPLY CURRENT vs.
AMBIENT TEMPERATURE**



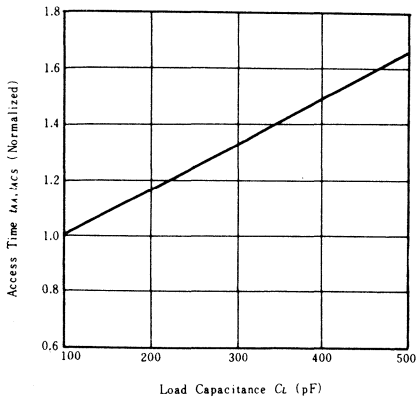
**ACCESS TIME vs.
SUPPLY VOLTAGE**



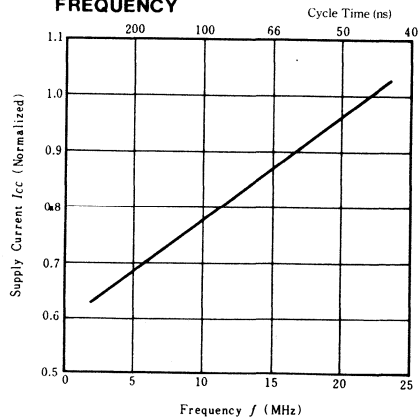
**ACCESS TIME vs.
AMBIENT TEMPERATURE**



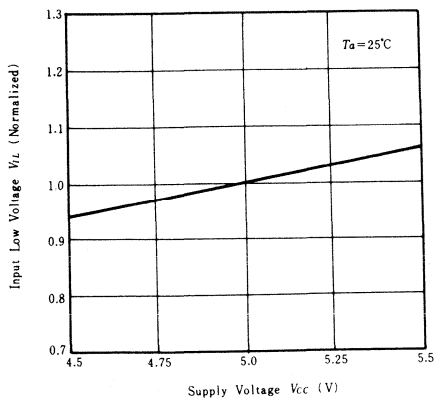
**ACCESS TIME vs.
LOAD CAPACITANCE**



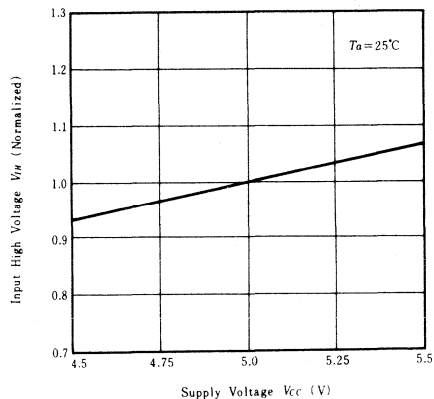
**SUPPLY CURRENT vs.
FREQUENCY**



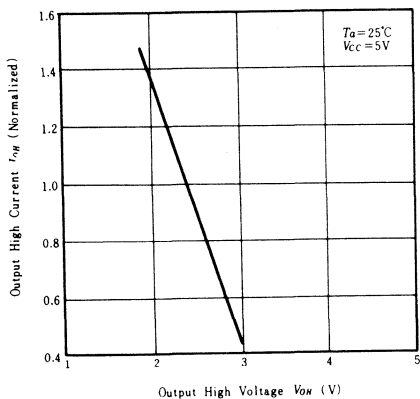
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



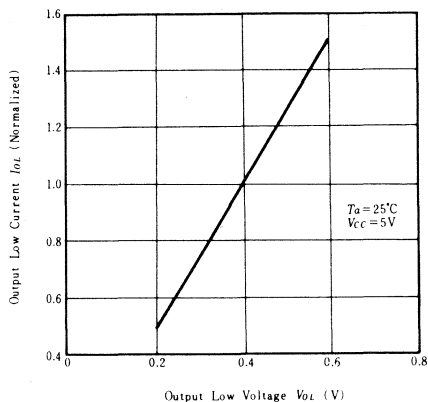
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



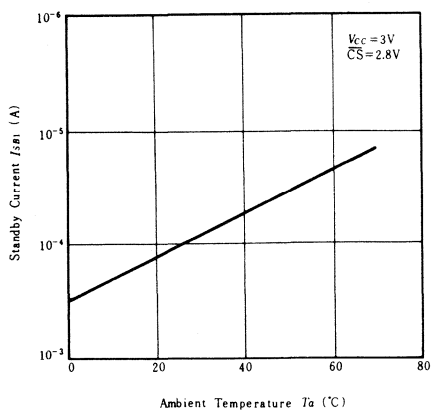
OUTPUT CURRENT vs. OUTPUT VOLTAGE



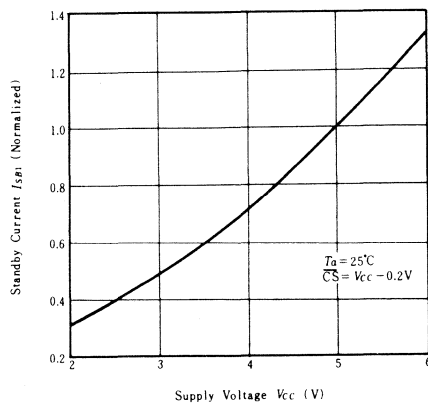
OUTPUT CURRENT vs. OUTPUT VOLTAGE



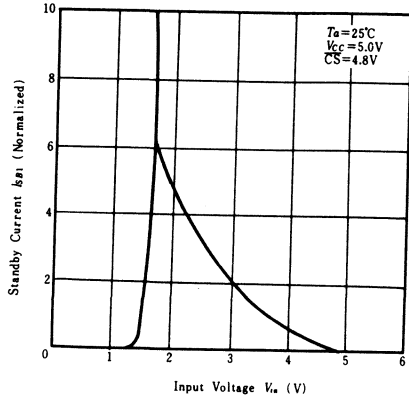
STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE



**STANDBY CURRENT vs.
INPUT VOLTAGE**



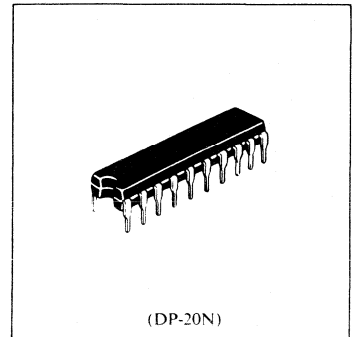
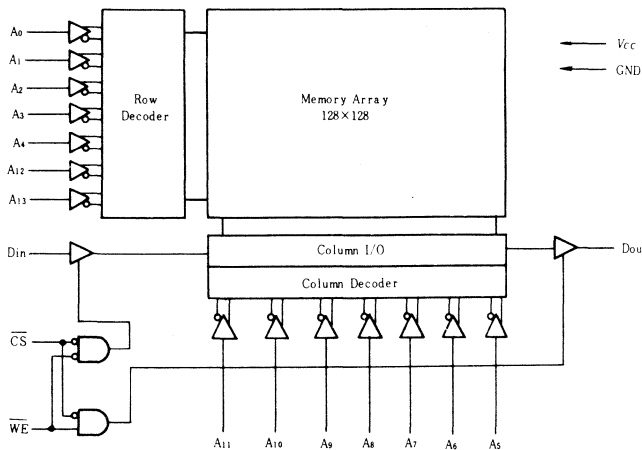
HM6167HLP Series

16384-word x 1-bit High Speed Static CMOS RAM

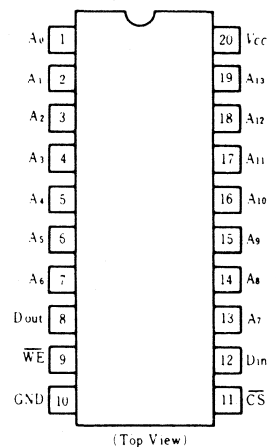
■ FEATURES

- Fast Access Time. HM6167HLP-55 55ns (max)
HM6167HLP-70 70ns (max)
- Low Power Standby and Low Power Operation
Standby $5\mu\text{W}$ (typ) and Operating 200mW (typ)
- Capable of Battery Back-up Operation
- Single +5V Supply and High Density 20 Pin Package
- Completely static Memory
No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible All Inputs and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with respect to GND	V_T	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

* Pulse Width 20ns, DC: -0.5V

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = -0.5V

■ TRUTH TABLE

CS	WE	Mode	V _{CC} Current	Dout Pin	Ref. Cycle
H	X	Not selected	I _{SB} , I _{SB1}	High-Z	
L	H	Read	I _{CC}	Dout	Read Cycle
L	L	Write	I _{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS (V_{CC} = 5V ± 10%, T_a = 0 ~ +70°C)

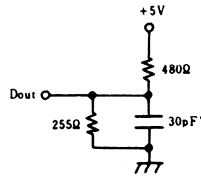
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5V V _{IN} = 0V ~ V _{CC}	—	—	2	μA
Output Leakage Current	I _{LO}	CS = V _{IN} , V _{o1} = 0V ~ V _{CC}	—	—	2	μA
Operating Power Supply Current	I _{CC}	CS = V _{IL} , Output Open	—	40	80	mA
Standby Power Supply Current	I _{SB}	CS = V _{IN}	—	10	20	mA
	I _{SB1}	CS = V _{CC} - 0.2V V _{IN} ≧ 0.2V or V _{IN} ≧ V _{CC} - 0.2V	—	1	50	μA
Output Low Voltage	V _{OL}	I _{OL} = 8mA	—	—	0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4mA	2.4	—	—	V

Note) Typical limits are at V_{CC} = 5.0V, T_a = 25°C and specified loading.

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
 Input rise and fall times: 5 ns
 Input timing reference levels: 1.5V
 Output reference levels: 1.5V
 Output load: See Figure

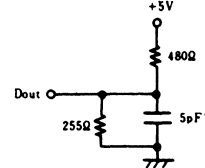
Output Load A



* Including scope and jig.

Output Load B

(for t_{HZ}, t_{LZ}, t_{wz} & t_{ow})



* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C _{IN}	—	5	pF	V _{IN} = 0V
Output Capacitance	C _{OUT}	—	7	pF	V _{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

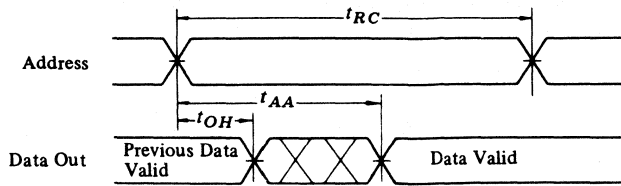
■ AC CHARACTERISTICS (T_a = 0°C to +70°C, V_{CC} = 5V ± 10%, unless otherwise noted.)

● READ CYCLE

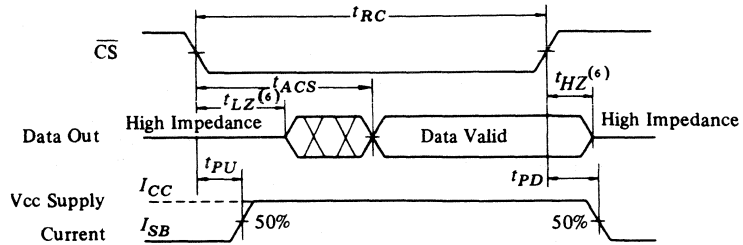
Item	Symbol	HM6167HLP-55		HM6167HLP-70		Unit	Notes
		min	max	min	max		
Read Cycle Time	t _{RC}	55	—	70	—	ns	(1)
Address Access Time	t _{AA}	—	55	—	70	ns	
Chip Select Access Time	t _{ACS}	—	55	—	70	ns	
Output Hold from Address Change	t _{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t _{LZ}	5	—	5	—	ns	(2) (3) (7)
Chip Selection to Output in High Z	t _{HZ}	0	30	0	30	ns	(2) (3) (7)
Chip Selection to Power Up Time	t _{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t _{PD}	—	30	—	35	ns	

- NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured ±500mV from steady state voltage with specified loading in Load B.
 4. WE is High for READ cycle.
 5. Device is continuously selected, CS = V_{IL}.
 6. Addresses valid prior to or coincident with CS transition low.
 7. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1 ^{4) 5)}



● TIMING WAVEFORM OF READ CYCLE NO. 2 ^{4) 6)}

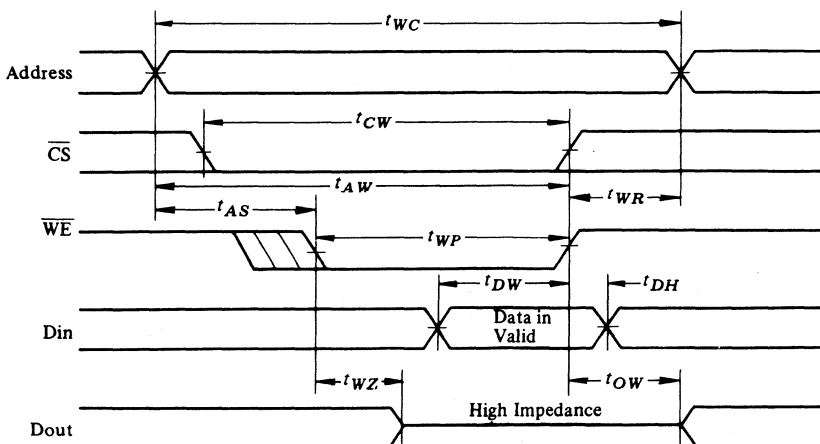


● WRITE CYCLE

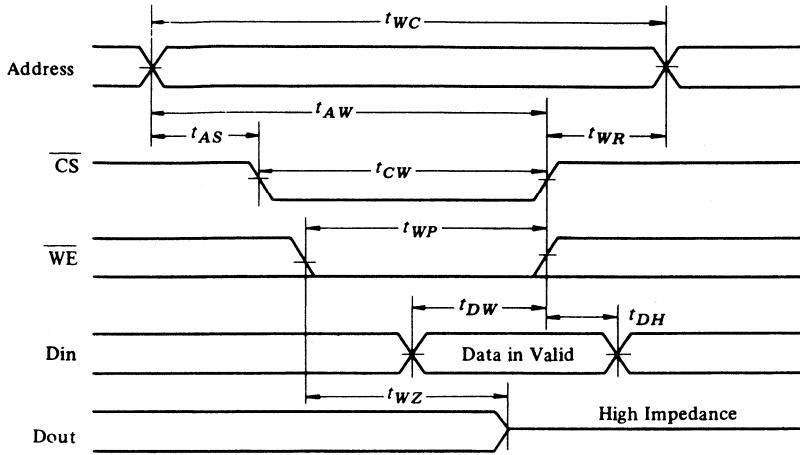
Item	Symbol	HM6167HLP-55		HM6167HLP-70		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	55	-	70	-	ns	(2)
Chip Selection to End of Write	t_{CW}	50	-	55	-	ns	
Address Valid to End of Write	t_{AW}	50	-	55	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	ns	
Write Pulse Width	t_{WP}	35	-	40	-	ns	
Write Recovery Time	t_{WR}	0	-	0	-	ns	
Data Valid to End of Write	t_{DW}	25	-	30	-	ns	
Data Hold Time	t_{DH}	0	-	0	-	ns	
Write Enable to Output in High Z	t_{WZ}	0	25	0	30	ns	(3) (4)
Output Active from End of Write	t_{OW}	0	-	0	-	ns	(3) (4)

- NOTES: 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
 3. Transition is measured $\pm 500mV$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} Controlled)



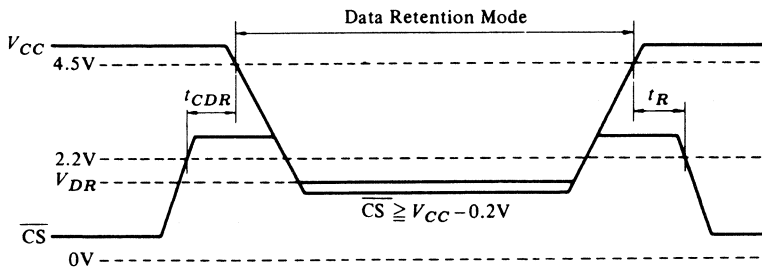
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a=0^\circ\text{C}$ to 70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{i*} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{i*} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	20*	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^Δ	—	—	ns

Δt_{RC} - Read Cycle Time

* $V_{CC} = 2.0\text{V}$
** $V_{CC} = 3.0\text{V}$

● LOW V_{CC} DATA RETENTION WAVEFORM



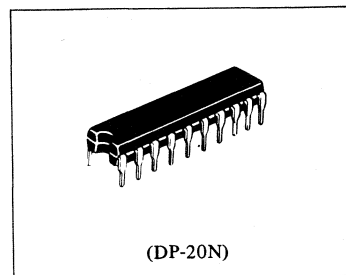
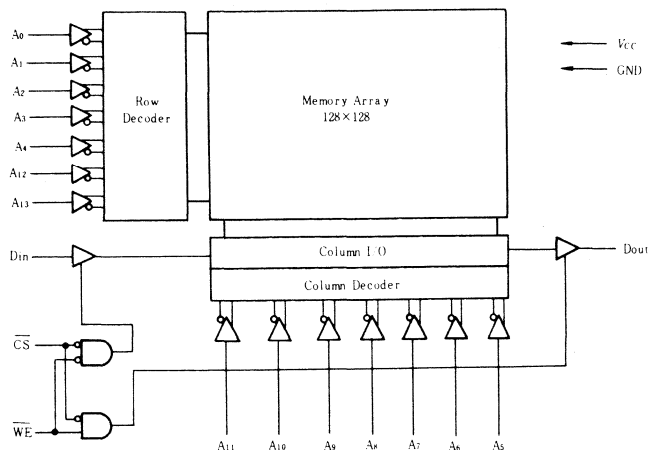
HM6267P Series

16384-word x 1-bit High Speed Static CMOS RAM

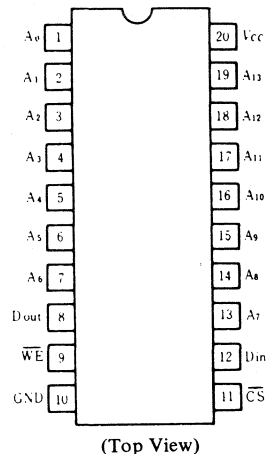
■ FEATURES

- High Speed: Fast Access Time 35/45ns (max.)
- Low Power Standby and Low Power Operation
Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

* with respect to GND. V_T min = -3.5V (Pulse width 20ns)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = -0.5V

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not selected	I_{SB}, I_{SB1}	High-Z	
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS⁽¹⁾ ($V_{CC} = 5V \pm 10\%$ ⁽²⁾, $GND = 0V$, $T_a = 0$ to $+70^\circ C$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5V, V_{in} = GND$ to V_{CC}	—	—	10	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS} = V_{IH}, V_{out} = GND$ to V_{CC}	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}$, Output Open	—	40	80 ⁽³⁾	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	—	10	20	mA
	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2V, V_{IN} \leq 0.2V$ or $V_{IN} \geq V_{CC} - 0.2V$	—	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL} = 8mA$	—	—	0.4	V
	V_{OH}	$I_{OH} = -4mA$	2.4	—	—	V

Notes) 1. Typical limits are at $V_{CC} = 5V, T_a = 25^\circ C$ and specified loading.
 2. $V_{CC} = 5V \pm 5\%$ for 35ns version.
 3. 100mA max. for 35ns version.

■ AC TEST CONDITIONS

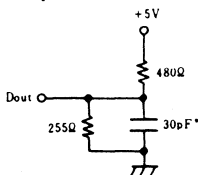
Input pulse levels: GND to 3.0V

Input rise and fall times: 5ns

Input and Output timing reference levels: 1.5V

Output load: See Figure

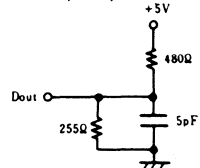
Output Load A



* Including scope and jig.

Output Load B

(for t_{HZ}, t_{LZ}, t_{WZ} & t_{OW})



* Including scope and jig.

■ CAPACITANCE ($T_a = 25^\circ C, f = 1MHz$)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C_{IN}	—	5	pF	$V_{IN} = 0V$
Output Capacitance	C_{OUT}	—	7	pF	$V_{OUT} = 0V$

Note) This parameter is sampled and not 100% tested.

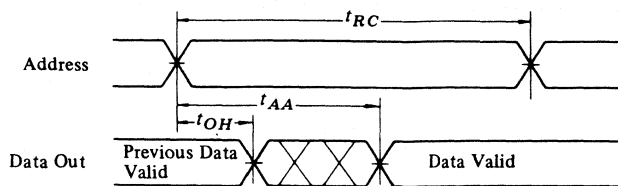
■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%*$, $T_a = 0$ to $70^\circ C$, unless otherwise noted.)

● READ CYCLE

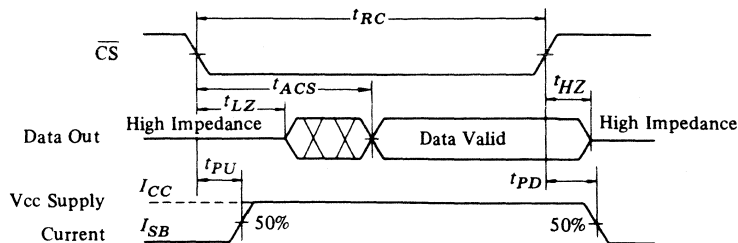
Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t_{RC}	35	—	45	—	ns	1
Address Access Time	t_{AA}	—	35	—	45	ns	
Chip Select Access Time	t_{ACS}	—	35	—	45	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	ns	
Chip Deselection to Power Down Time	t_{PD}	—	20	—	30	ns	

* $V_{CC} = 5V \pm 5\%$ for 35ns version.

● TIMING WAVEFORM OF READ CYCLE NO. 1 ^{4) 5)}



● TIMING WAVEFORM OF READ CYCLE NO. 2 ^{4) 6)}

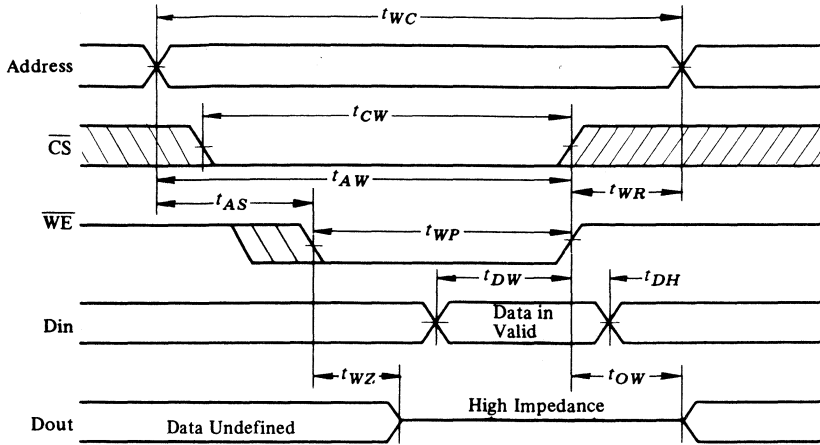


- NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is High for READ cycle.
 5. Device is continuously selected, $\overline{CS} = V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

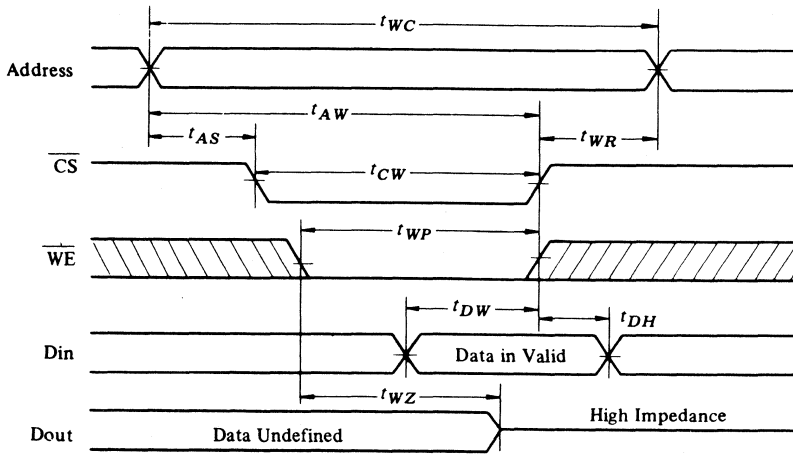
● WRITE CYCLE

Item	Symbol	HM6267P-35		HM6267P-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	2
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns	
Address Valid to End of Write	t_{AW}	30	—	40	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} Controlled)

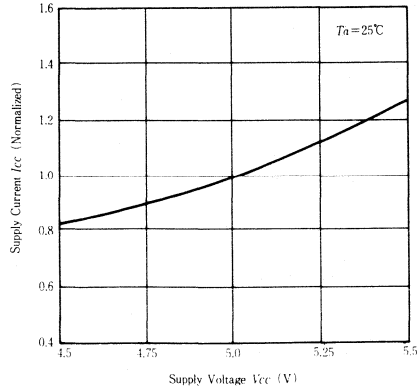


● TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} Controlled)

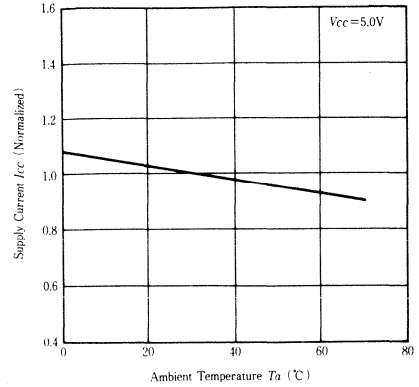


- NOTES: 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

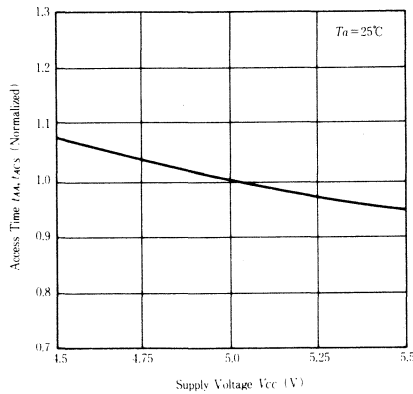
SUPPLY CURRENT VS. SUPPLY VOLTAGE



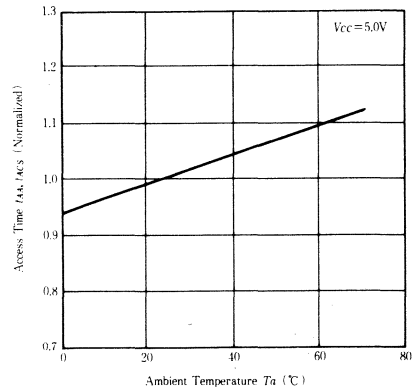
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



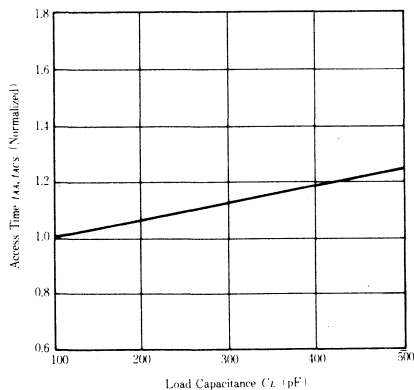
ACCESS TIME VS. SUPPLY VOLTAGE



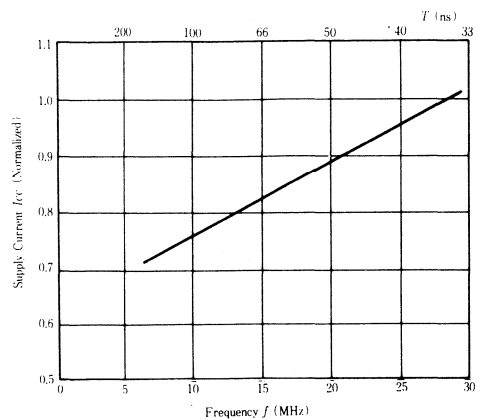
ACCESS TIME VS. AMBIENT TEMPERATURE



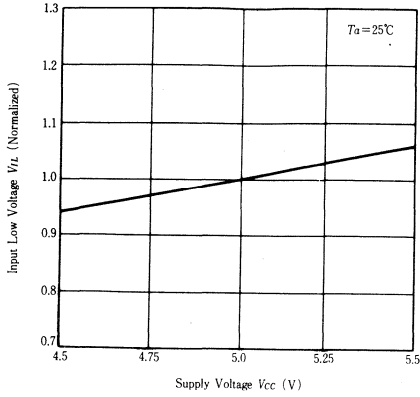
ACCESS TIME VS. LOAD CAPACITANCE



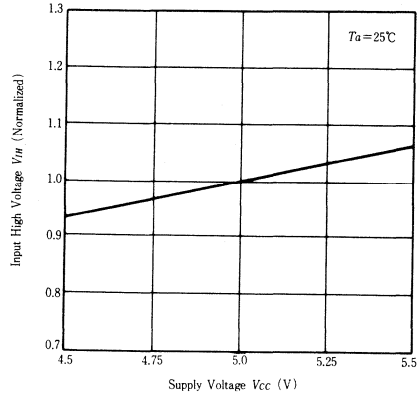
SUPPLY CURRENT VS. FREQUENCY



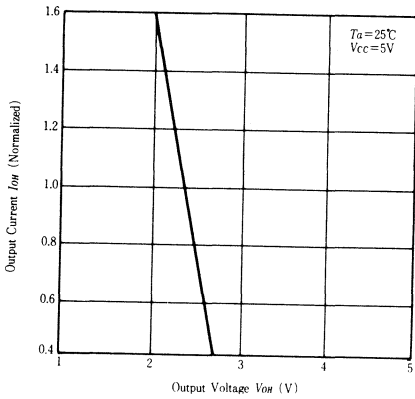
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



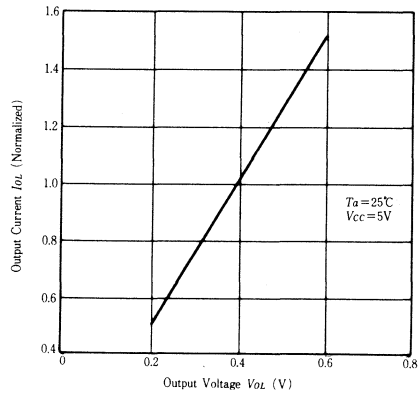
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



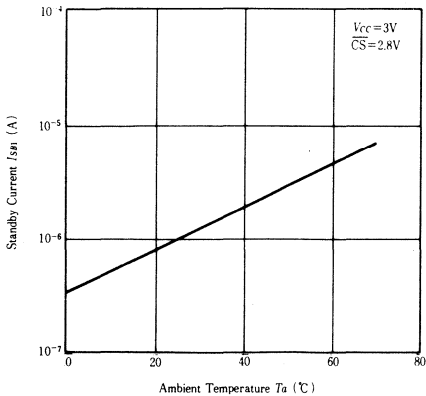
OUTPUT CURRENT VS. OUTPUT VOLTAGE



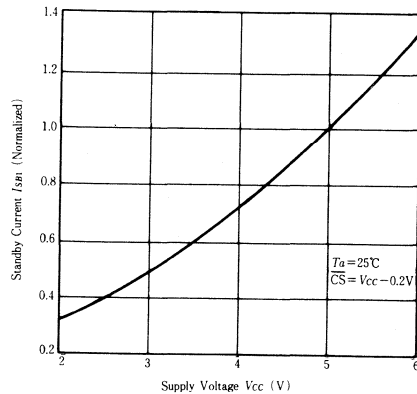
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



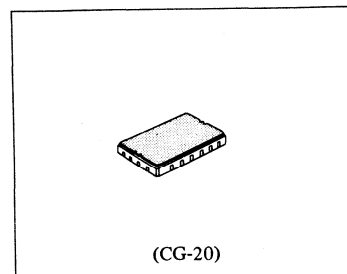
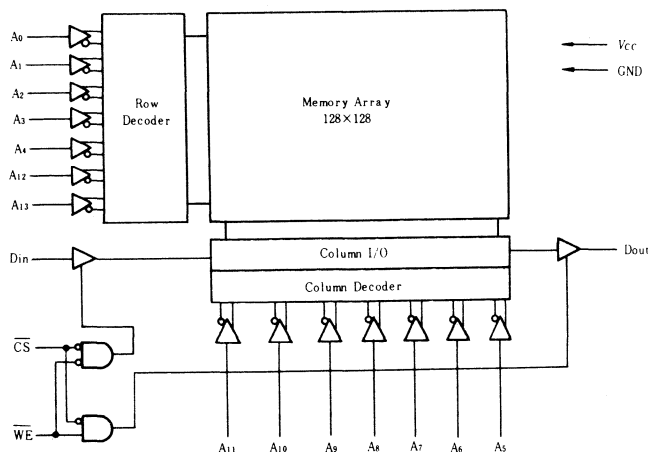
HM6267CG Series

16384-word x 1-bit High Speed Static CMOS RAM

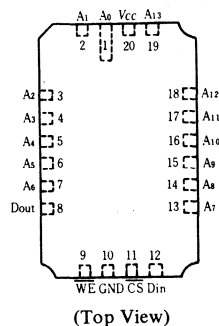
■ FEATURES

- High Speed: Fast Access Time 35/45ns (max.)
- Low Power Standby and Low Power Operation
Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Single 5V Supply
- Completely Static Memory No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-65 to +150	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

* with respect to GND. V_T min = -3.5V (Pulse width 20ns)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = -0.5V

■ TRUTH TABLE

CS	WE	Mode	V _{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I _{SB} , I _{SB1}	High-Z	
L	H	Read	I _{CC}	Dout	Read Cycle
L	L	Write	I _{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS⁽¹⁾ (V_{CC} = 5V ± 10%⁽²⁾, GND = 0V, T_a = 0 to +70°C)

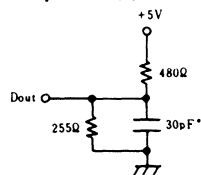
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5V, V _{in} = GND to V _{CC}	–	–	10	μA
Output Leakage Current	I _{LO}	CS = V _{IH} , V _{out} = GND to V _{CC}	–	–	10	μA
Operating Power Supply Current	I _{CC}	CS = V _{IL} , Output Open	–	40	80 ⁽³⁾	mA
Standby Power Supply Current	I _{SB}	CS = V _{IH}	–	10	20	mA
	I _{SB1}	CS ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} - 0.2V	–	0.02	2	mA
Output Voltage	V _{OL}	I _{OL} = 8mA	–	–	0.4	V
	V _{OH}	I _{OH} = -4mA	2.4	–	–	V

- Notes) 1. Typical limits are at V_{CC} = 5V, T_a = 25°C and specified loading.
 2. V_{CC} = 5V ± 5% for 35ns version.
 3. 100mA max. for 35ns version.

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
 Input rise and fall times: 5ns
 Input and Output timing reference levels: 1.5V
 Output load: See Figure

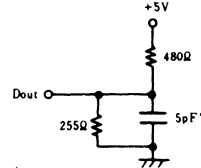
Output Load A



* Including scope and jig.

Output Load B

(for t_{HZ}, t_{LZ}, t_{wZ} & t_{ow})



* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C _{IN}	–	5	pF	V _{IN} = 0V
Output Capacitance	C _{OUT}	–	7	pF	V _{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

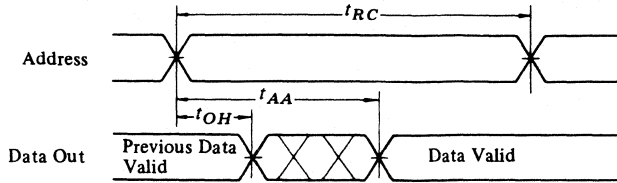
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%*, T_a = 0 to 70°C, unless otherwise noted.)

● READ CYCLE

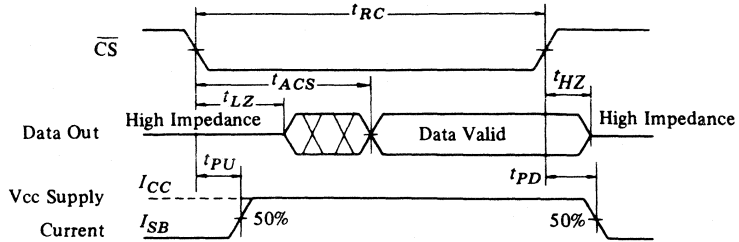
Item	Symbol	HM267CG-35		HM6267CG-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t _{RC}	35	–	45	–	ns	1
Address Access Time	t _{AA}	–	35	–	45	ns	
Chip Select Access Time	t _{ACS}	–	35	–	45	ns	
Output Hold from Address Change	t _{OH}	5	–	5	–	ns	
Chip Selection to Output in Low Z	t _{LZ}	5	–	5	–	ns	2, 3, 7
Chip Deselection to Output in High Z	t _{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t _{PU}	0	–	0	–	ns	
Chip Deselection to Power Down Time	t _{PD}	–	20	–	30	ns	

* V_{CC} = 5V ± 5% for 35ns version.

● TIMING WAVEFORM OF READ CYCLE NO. 1 ^{4) 5)}



● TIMING WAVEFORM OF READ CYCLE NO. 2 ^{4) 6)}

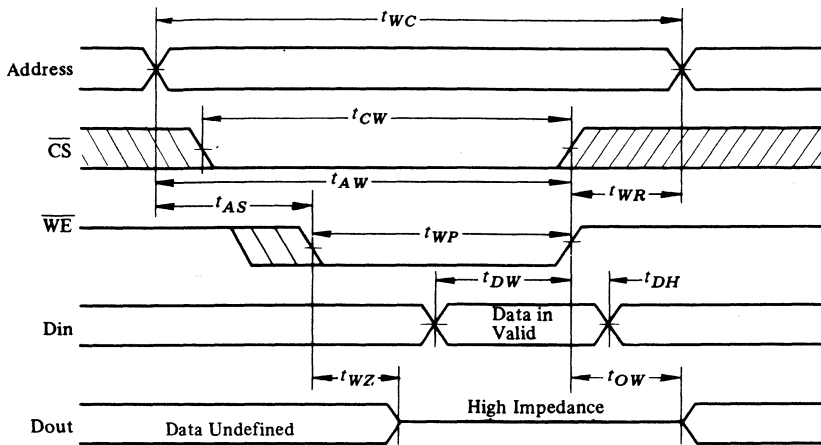


- NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is High for READ cycle.
 5. Device is continuously selected, $\overline{CS} = V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

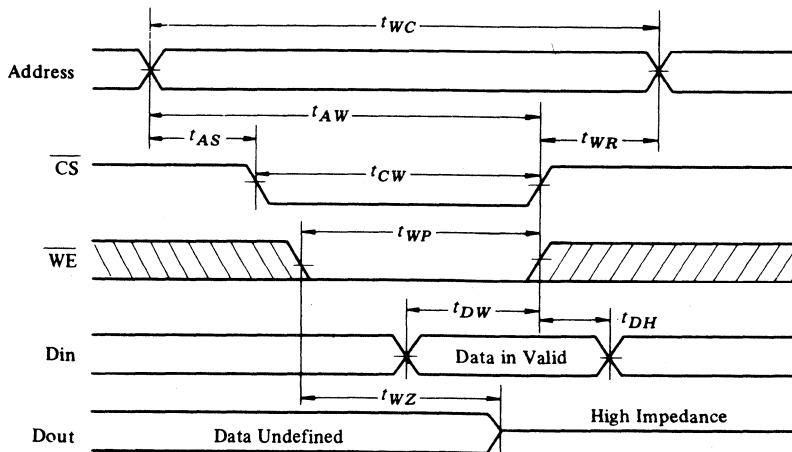
● WRITE CYCLE

Item	Symbol	HM6267CG-35		HM6267CG-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	2
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns	
Address Valid to End of Write	t_{AW}	30	—	40	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} Controlled)



- NOTES: 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

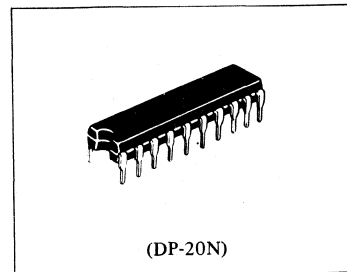
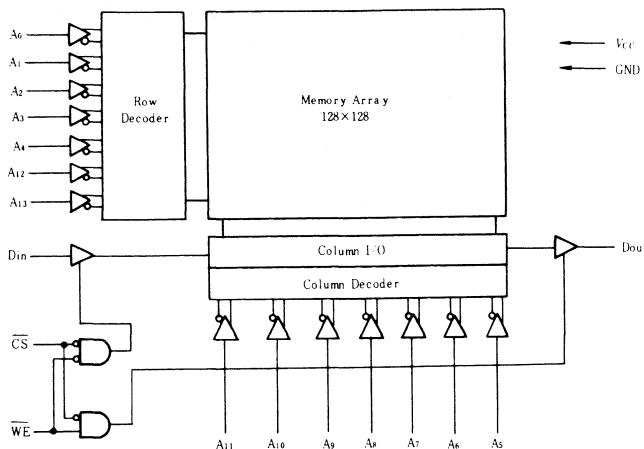
HM6267LP Series

16384-word x 1-bit High Speed Static CMOS RAM

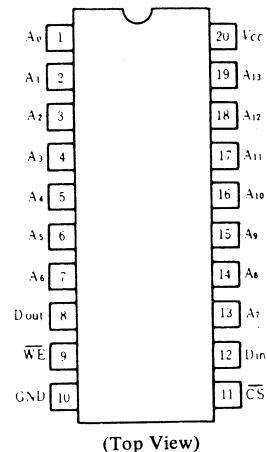
■ FEATURES

- High Speed: Fast Access Time 35/45ns (max.)
- Low Power Standby and Low Power Operation
Standby: 5 μ W (typ.), Operation: 220mW (typ.)
- Single 5V Supply and High Density 20 Pin Package
- Completely Static Memory No Clock or Timing Strobe Required
- Equal Access and Cycle Time
- Directly TTL Compatible: All Input and Output
- Capable of Battery Back Up Operation

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C
Temperature Under Bias	T_{bias}	-10 to +85	$^{\circ}$ C

* with respect to GND. V_T min = -3.5V (Pulse width 20ns)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70 $^{\circ}$ C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

* Pulse Width 20ns, DC: V_{IL} min = -0.5V

■ TRUTH TABLE

CS	WE	Mode	V _{CC} Current	Dout Pin	Ref. Cycle
H	×	Not selected	I _{SB} , I _{SB1}	High-Z	
L	H	Read	I _{CC}	Dout	Read Cycle
L	L	Write	I _{CC}	High-Z	Write Cycle

■ DC AND OPERATING CHARACTERISTICS⁽¹⁾ (V_{CC} = 5V ± 10%⁽²⁾, GND = 0V, T_a = 0 to +70°C)

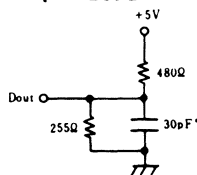
Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	V _{CC} = 5.5V, V _{in} = GND to V _{CC}	-	-	10	μA
Output Leakage Current	I _{LO}	CS = V _{IH} , V _{out} = GND to V _{CC}	-	-	10	μA
Operating Power Supply Current	I _{CC}	CS = V _{IL} , Output Open	-	40	80 ⁽³⁾	mA
Standby Power Supply Current	I _{SB}	CS = V _{IH}	-	10	20	mA
	I _{SB1}	CS ≥ V _{CC} - 0.2V, V _{IN} ≤ 0.2V or V _{IN} ≥ V _{CC} - 0.2V	-	10	50	μA
Output Voltage	V _{OL}	I _{OL} = 8mA	-	-	0.4	V
	V _{OH}	I _{OH} = -4mA	2.4	-	-	V

- Notes) 1. Typical limits are at V_{CC} = 5V, T_a = 25°C and specified loading.
 2. V_{CC} = 5V ± 5% for 35ns version.
 3. 100mA max. for 35ns version.

■ AC TEST CONDITIONS

Input pulse levels: GND to 3.0V
 Input rise and fall times: 5ns
 Input and Output timing reference levels: 1.5V
 Output load: See Figure

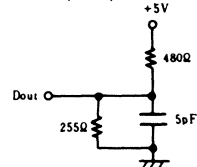
Output Load A



* Including scope and jig.

Output Load B

(for t_{wz}, t_{LZ}, t_{wz} & t_{ow})



* Including scope and jig.

■ CAPACITANCE (T_a = 25°C, f = 1MHz)

Item	Symbol	typ.	max	Unit	Conditions
Input Capacitance	C _{IN}	-	5	pF	V _{IN} = 0V
Output Capacitance	C _{OUT}	-	7	pF	V _{OUT} = 0V

Note) This parameter is sampled and not 100% tested.

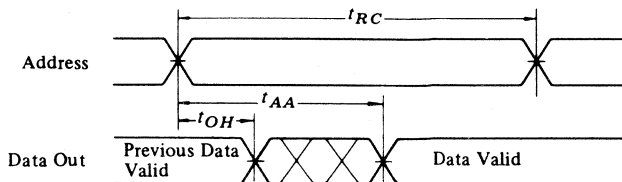
■ AC CHARACTERISTICS (V_{CC} = 5V ± 10%*, T_a = 0 to 70°C, unless otherwise noted.)

● READ CYCLE

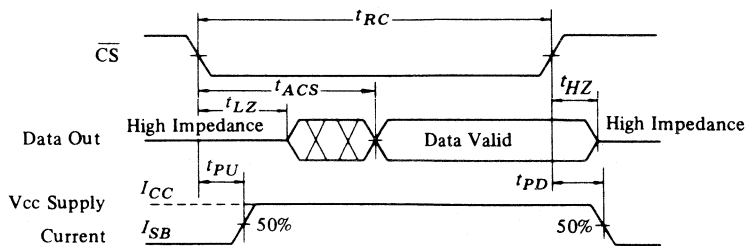
Item	Symbol	HM6267LP-35		HM6267LP-45		Unit	Notes
		min	max	min	max		
Read Cycle Time	t _{RC}	35	-	45	-	ns	1
Address Access Time	t _{AA}	-	35	-	45	ns	
Chip Select Access Time	t _{ACS}	-	35	-	45	ns	
Output Hold from Address Change	t _{OH}	5	-	5	-	ns	
Chip Selection to Output in Low Z	t _{LZ}	5	-	5	-	ns	2, 3, 7
Chip Deselection to Output in High Z	t _{HZ}	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t _{PU}	0	-	0	-	ns	
Chip Deselection to Power Down Time	t _{PD}	-	20	-	30	ns	

* V_{CC} = 5V ± 5% for 35ns version.

● TIMING WAVEFORM OF READ CYCLE NO. 1 ^{4) 5)}



● TIMING WAVEFORM OF READ CYCLE NO. 2 ^{4) 6)}

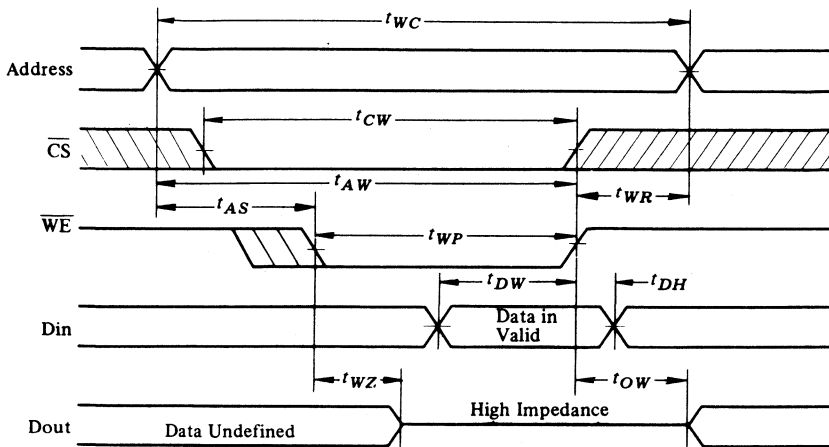


- NOTES: 1. All Read Cycle timing are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. \overline{WE} is High for READ cycle.
 5. Device is continuously selected, $\overline{CS} = V_{IL}$.
 6. Addresses valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

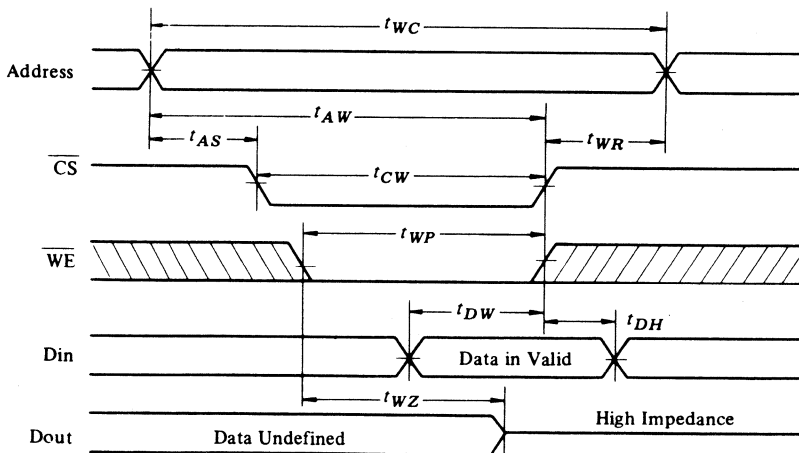
● WRITE CYCLE

Item	Symbol	HM6267LP-35		HM6267LP-45		Unit	Notes
		min	max	min	max		
Write Cycle Time	t_{WC}	35	—	45	—	ns	2
Chip Selection to End of Write	t_{CW}	30	—	40	—	ns	
Address Valid to End of Write	t_{AW}	30	—	40	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	ns	
Write Pulse Width	t_{WP}	20	—	25	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	20	—	25	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	20	0	25	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	ns	3, 4

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} Controlled)



● TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} Controlled)



- NOTES: 1. If \overline{CS} goes high simultaneously with \overline{WE} high, the output remains in a high impedance states.
 2. All Write Cycle timings are referenced from the last valid address to the first transitions address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

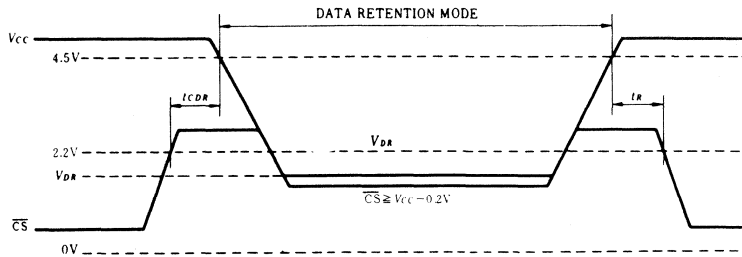
■ **LOW V_{CC} DATA RETENTION CHARACTERISTICS** ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$ $V_{i,s} \geq V_{CC} - 0.2\text{V}$ or $0\text{V} \leq V_{i,s} \leq 0.2\text{V}$	2.0	—	—	V
Data Retention Current	I_{CCDR}		—	—	30* 20**	μA
Chip Deselect to Data Retention Time	t_{CDR}		0	—	—	ns
Operation Recovery Time	t_R		$t_{RC(1)}$	—	—	ns

Note: 1. t_{RC} - Read Cycle Time.

* $V_{CC} = 3.0\text{V}$
 ** $V_{CC} = 2.0\text{V}$

● **LOW V_{CC} DATA RETENTION WAVEFORM**

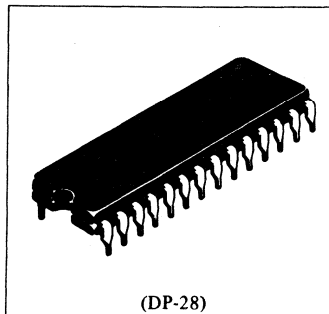


HM6264P Series

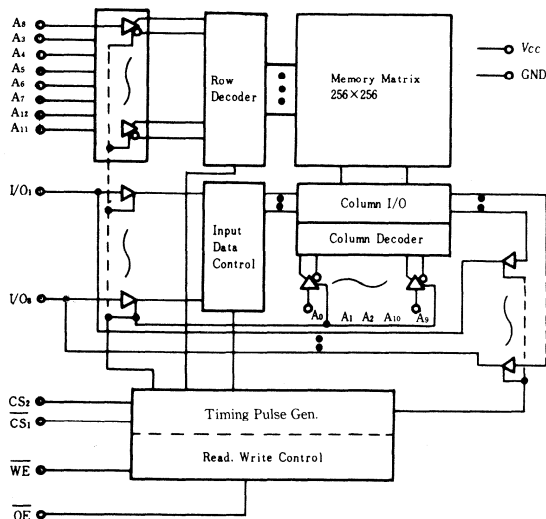
8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

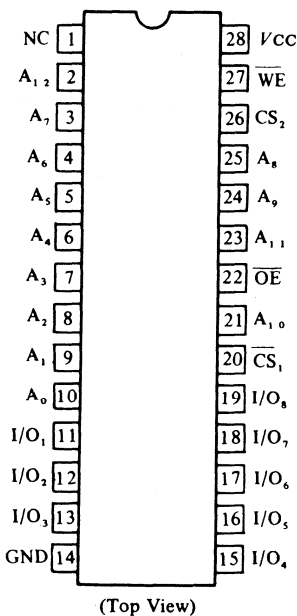
- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.1mW (typ.)
- Low Power Operation Operating: 200mW (typ.)
- Single +5V Supply
- Completely Static Memory. . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764



■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

* With respect to GND. ** Pulse width 50ns: -3.0V

■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V _{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	<i>I_{SB}</i> , <i>I_{SB1}</i>	
X	X	L	X		High Z	<i>I_{SB}</i> , <i>I_{SB2}</i>	
H	L	H	H	Output Disabled	High Z	<i>I_{CC}</i> , <i>I_{CC1}</i>	
H	L	H	L	Read	Dout	<i>I_{CC}</i> , <i>I_{CC1}</i>	
L	L	H	H	Write	Din	<i>I_{CC}</i> , <i>I_{CC1}</i>	Write Cycle (1)
L	L	H	L		Din	<i>I_{CC}</i> , <i>I_{CC1}</i>	Write Cycle (2)

X : H or L

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.3*	—	0.8	V

* Pulse Width 50ns: -3.0V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$, $V_{I/O} = \text{GND to } V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	—	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O} = 0\text{mA}$	—	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	—	1	3	mA
	I_{SB1}^{**}	$\overline{\text{CS}}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	—	0.02	2	mA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	—	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.

** V_{IL} min = -0.3V

CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	—	8	pF

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

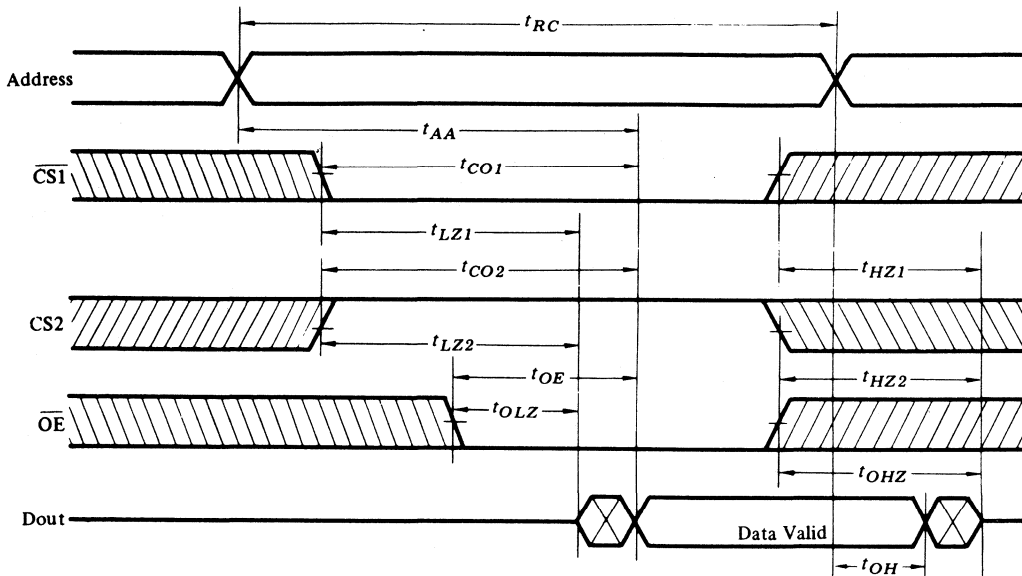
READ CYCLE

Item	Symbol	HM6264P-10		HM6264P-12		HM6264P-15		Unit	
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	100	—	120	—	150	—	ns	
Address Access Time	t_{AA}	—	100	—	120	—	150	ns	
Chip Selection to Output	$\overline{\text{CS}}1$	t_{CO1}	—	100	—	120	—	150	ns
	$\overline{\text{CS}}2$	t_{CO2}	—	100	—	120	—	150	ns
Output Enable to Output Valid	t_{OE}	—	50	—	60	—	70	ns	
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$	t_{LZ1}	10	—	10	—	15	—	ns
	$\overline{\text{CS}}2$	t_{LZ2}	10	—	10	—	15	—	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	ns	
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$	t_{HZ1}	0	35	0	40	0	50	ns
	$\overline{\text{CS}}2$	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Hold from Address Change	t_{OH}	10	—	10	—	15	—	ns	

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

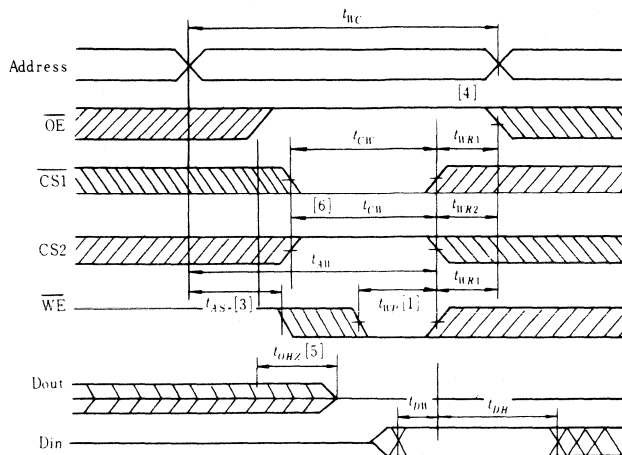


NOTE: 1) \overline{WE} is high for Read Cycle

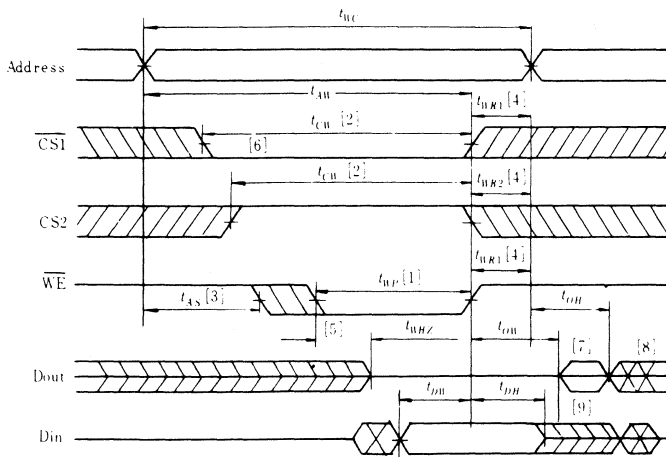
• WRITE CYCLE

Item	Symbol	HM6264P-10		HM6264P-12		HM6264P-15		Unit	
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns	
Chip Selection to End of Write	t_{CW}	80	-	85	-	100	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Address Valid to End of Write	t_{AW}	80	-	85	-	100	-	ns	
Write Pulse Width	t_{WP}	60	-	70	-	90	-	ns	
Write Recovery Time	$\overline{CS1}, \overline{WE}$	t_{WR1}	5	-	5	-	10	-	ns
	CS2	t_{WR2}	15	-	15	-	15	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns	
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
\overline{OE} to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	10	-	ns	

• WRITE CYCLE (1) ($\overline{\text{OE}}$ clock)

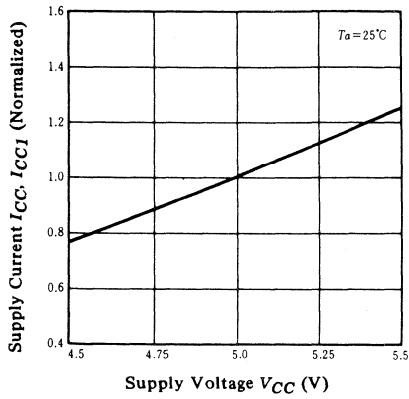


• WRITE CYCLE (2) ($\overline{\text{OE}}$ Low Fix)

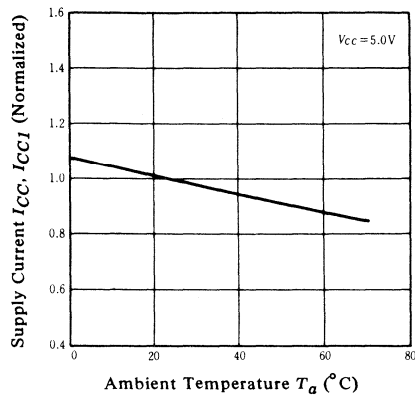


- NOTES: 1) A write occurs during the overlap of a low $\overline{\text{CS1}}$, a high $\overline{\text{CS2}}$ and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS1}}$ going low, $\overline{\text{CS2}}$ going high and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CS1}}$ going high, $\overline{\text{CS2}}$ going low and $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or $\overline{\text{CS2}}$ going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the end of write to the earliest change.
 t_{WR1} applies in case a write ends at $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high.
 t_{WR2} applies in case a write ends at $\overline{\text{CS2}}$ going low.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{\text{CS1}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
- 7) D_{out} is the same phase of the latest written data in this write cycle.
- 8) D_{out} is the read data of next address.
- 9) If $\overline{\text{CS1}}$ is low and $\overline{\text{CS2}}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

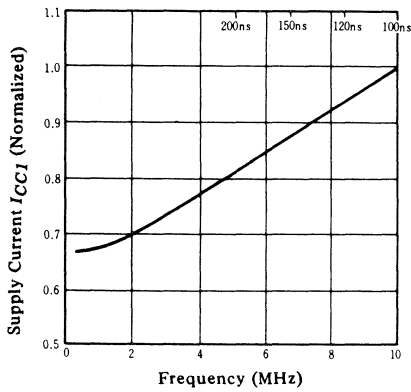
SUPPLY CURRENT vs. SUPPLY VOLTAGE



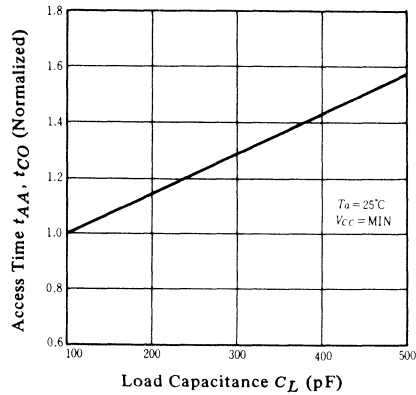
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



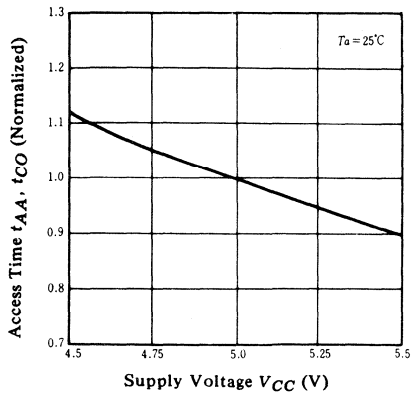
SUPPLY CURRENT vs. FREQUENCY



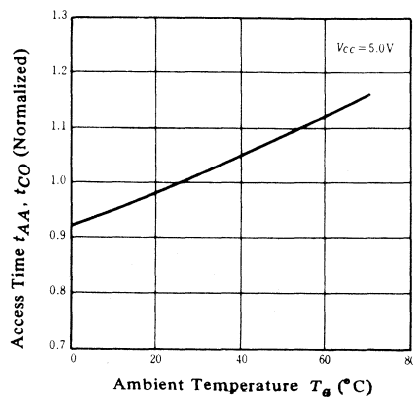
ACCESS TIME vs. LOAD CAPACITANCE



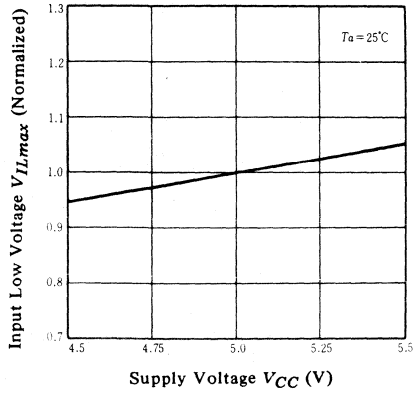
ACCESS TIME vs. SUPPLY VOLTAGE



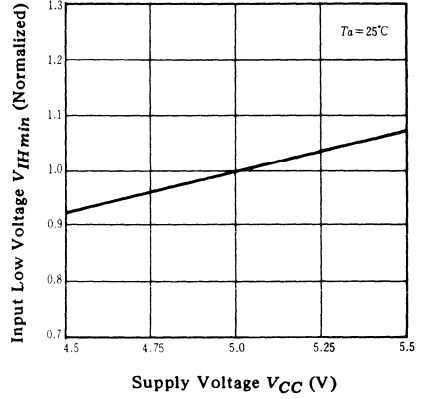
ACCESS TIME vs. AMBIENT TEMPERATURE



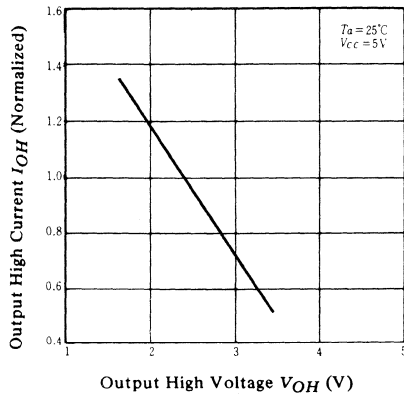
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



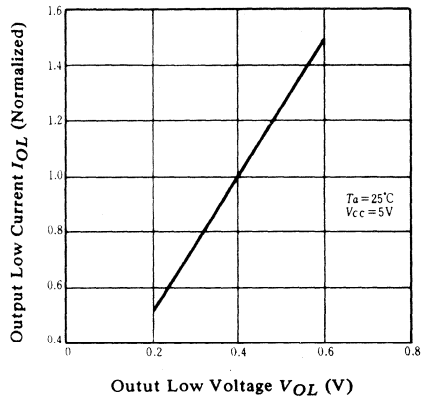
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE



OUTPUT CURRENT vs. OUTPUT VOLTAGE

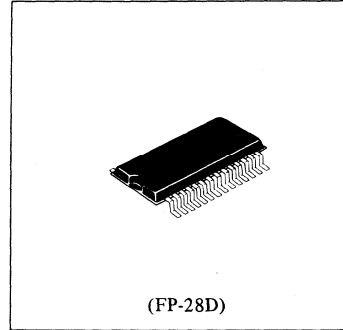


HM6264FP Series

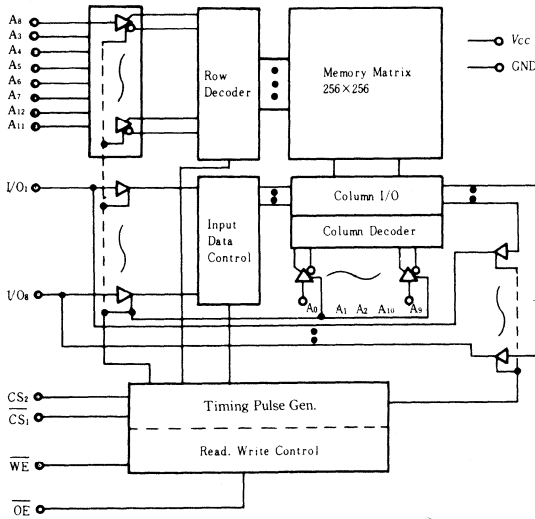
8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

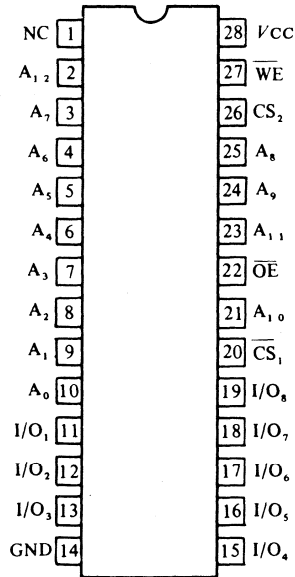
- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 100/120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
Standby: 0.1mW (typ.), Operation: 200mW (typ.)
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time



■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

* With respect to GND. ** Pulse width 50ns: -3.0V

■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-0.3*	—	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$. $V_{I/O} = \text{GND to } V_{CC}$	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\text{CS}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	—	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O} = 0\text{mA}$	—	60	110	mA
Standby Power Supply Current	I_{SB}	$\text{CS}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	—	1	3	mA
	I_{SB1}^{**}	$\text{CS}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	—	0.02	2	mA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	—	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.

** V_{IL} min = -0.3V

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	—	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

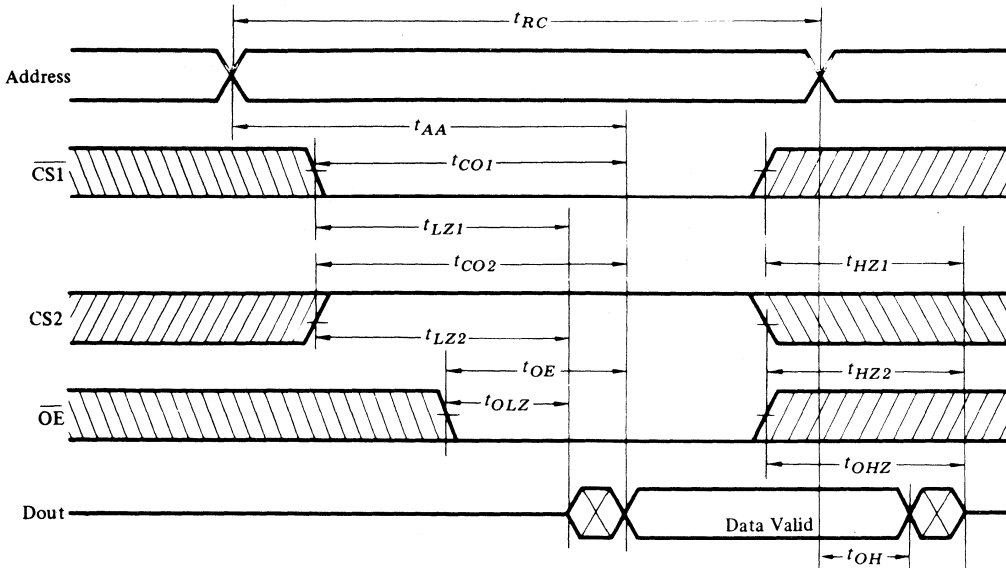
● READ CYCLE

Item	Symbol	HM6264FP-10		HM6264FP-12		HM6264FP-15		Unit	
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	100	—	120	—	150	—	ns	
Address Access Time	t_{AA}	—	100	—	120	—	150	ns	
Chip Selection to Output	$\overline{\text{CS}}1$	t_{CO1}	—	100	—	120	—	150	ns
	$\text{CS}2$	t_{CO2}	—	100	—	120	—	150	ns
Output Enable to Output Valid	t_{OE}	—	50	—	60	—	70	ns	
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$	t_{LZ1}	10	—	10	—	15	—	ns
	$\text{CS}2$	t_{LZ2}	10	—	10	—	15	—	ns
Output Enable to Output in Low Z	t_{QLZ}	5	—	5	—	5	—	ns	
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$	t_{HZ1}	0	35	0	40	0	50	ns
	$\text{CS}2$	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Hold from Address Change	t_{OH}	10	—	10	—	15	—	ns	

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

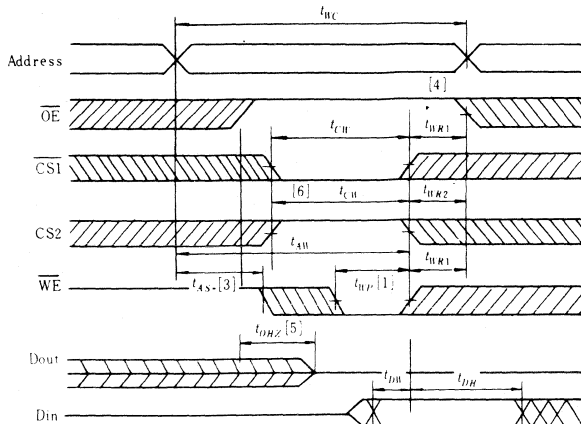


NOTE: 1) \overline{WE} is high for Read Cycle

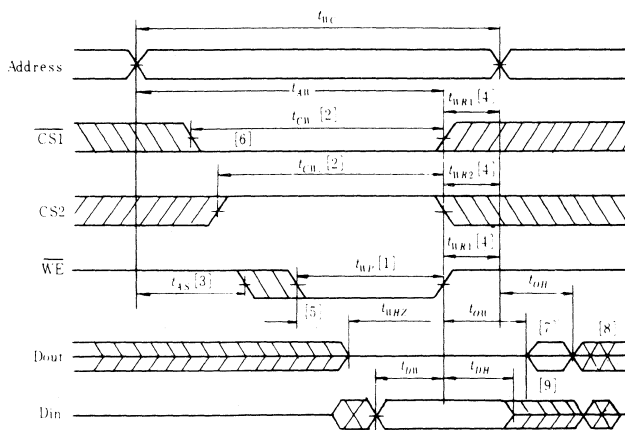
• WRITE CYCLE

Item	Symbol	HM6264FP-10		HM6264FP-12		HM6264FP-15		Unit	
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns	
Chip Selection to End of Write	t_{CW}	80	-	85	-	100	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Address Valid to End of Write	t_{AW}	80	-	85	-	100	-	ns	
Write Pulse Width	t_{WP}	60	-	70	-	90	-	ns	
Write Recovery Time	CS1, \overline{WE}	t_{WR1}	5	-	5	-	10	-	ns
	CS2	t_{WR2}	15	-	15	-	15	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns	
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
\overline{OE} to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	10	-	ns	

• WRITE CYCLE (1) (\overline{OE} clock)



• WRITE CYCLE (2) (\overline{OE} Low Fix)



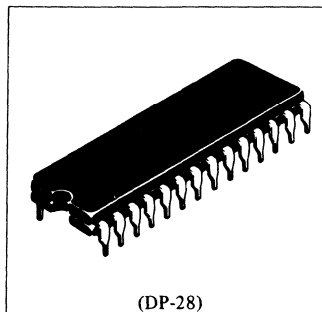
- NOTES: 1) A write occurs during the overlap of a low CS1, a high CS2 and a low WE. A write begins at the latest transition among CS1 going low, CS2 going high and WE going low. A write ends at the earliest transition among CS1 going high, CS2 going low and WE going high. t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of CS1 going low or CS2 going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the end of write to the address change.
 t_{WR1} applies in case a write ends at CS1 or WE going high.
 t_{WR2} applies in case a write ends at CS2 going low.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If CS1 goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.
- 7) Dout is the same phase of the latest written data in this write cycle.
- 8) Dout is the read data of next address.
- 9) If CS1 is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

HM6264LP Series

8192-word x 8-bit High Speed Static CMOS RAM

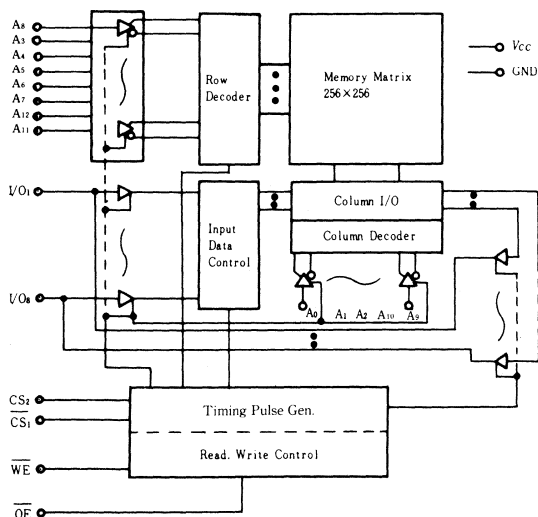
■ FEATURES

- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.01mW (typ.)
- Low Power Operation Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

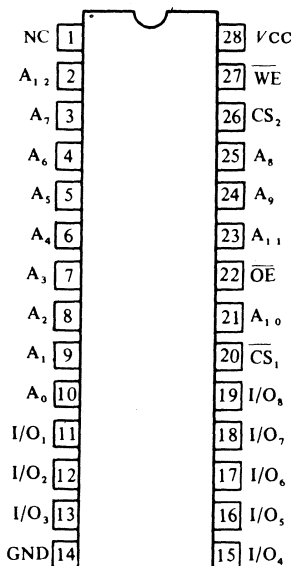


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

* With respect to GND ** Pulse width 50ns: -3.0V

■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V _{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	ISB, ISB1	
X	X	L	X		High Z	ISB, ISB2	
H	L	H	H	Output Disabled	High Z	ICC, ICC1	
H	L	H	L	Read	Dout	ICC, ICC1	
L	L	H	H	Write	Din	ICC, ICC1	Write Cycle (1)
L	L	H	L		Din	ICC, ICC1	Write Cycle (2)

X: H or L

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.3*	–	0.8	V

* Pulse Width 50ns: -3.0V

DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	–	–	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\text{OE} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$, $V_{I/O} = \text{GND to } V_{CC}$	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O} = 0\text{mA}$	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\text{CS}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	–	1	3	mA
	I_{SB1}^{**}	$\overline{\text{CS}}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	–	2	100	μA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	–	2	100	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	–	–	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.** V_{IL} min = -0.3V
CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	–	8	pF

Note) This parameter is sampled and not 100% tested.

AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

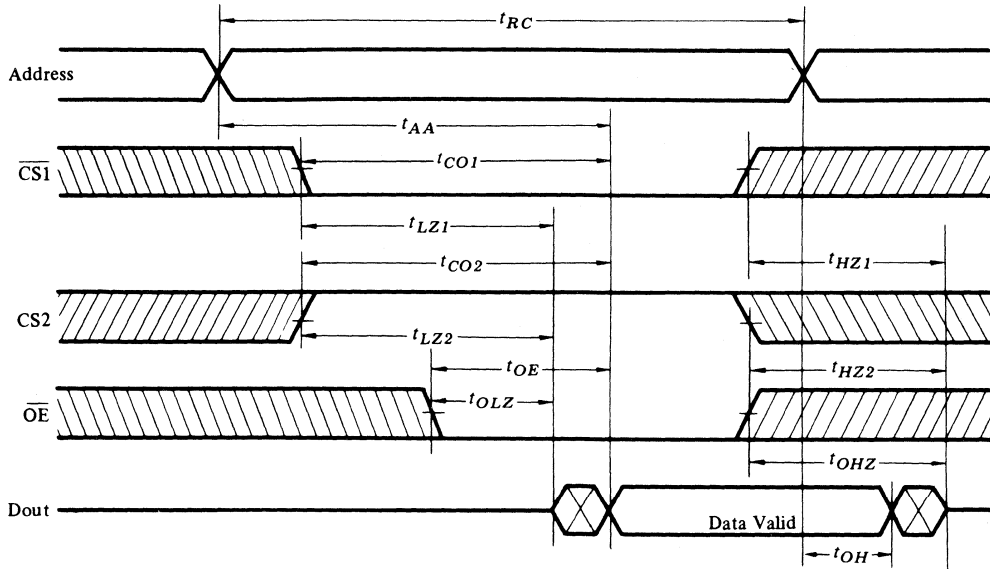
Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)
READ CYCLE

Item	Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit	
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns	
Address Access Time	t_{AA}	–	100	–	120	–	150	ns	
Chip Selection to Output	$\overline{\text{CS}}1$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns	
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns	
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Hold from Address Change	t_{OH}	10	–	10	–	15	–	ns	

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

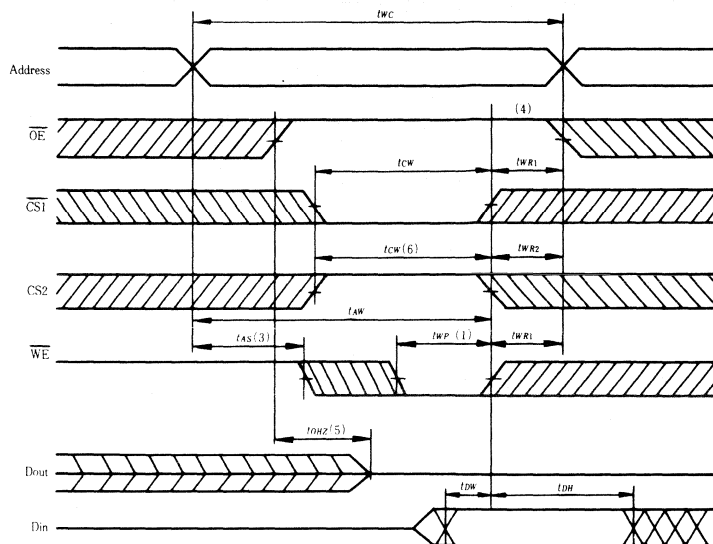


NOTE : 1) \overline{WE} is high for Read Cycle

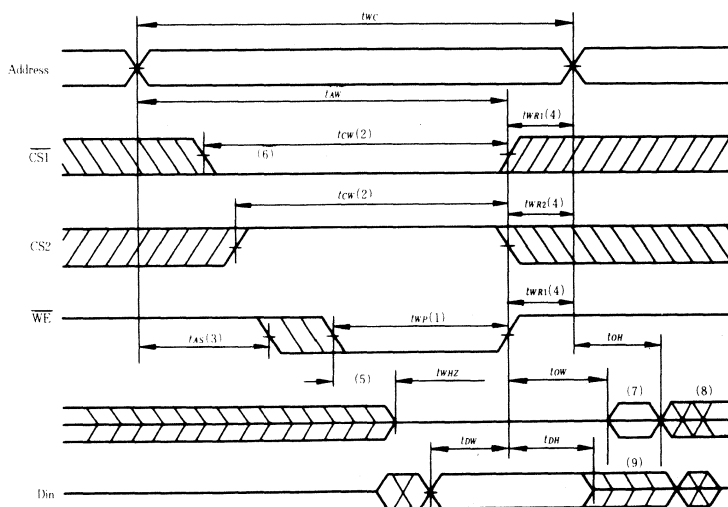
• WRITE CYCLE

Item	Symbol	HM6264LP-10		HM6264LP-12		HM6264LP-15		Unit	
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	100	—	120	—	150	—	ns	
Chip Selection to End of Write	t_{CW}	80	—	85	—	100	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AW}	80	—	85	—	100	—	ns	
Write Pulse Width	t_{WP}	60	—	70	—	90	—	ns	
Write Recovery Time	CS1, WE	t_{WR1}	5	—	5	—	10	—	ns
	CS2	t_{WR2}	15	—	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns	
Data to Write Time Overlap	t_{DW}	40	—	50	—	60	—	ns	
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns	
\overline{OE} to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Active from End of Write	t_{OW}	5	—	5	—	10	—	ns	

● WRITE CYCLE (1) ($\overline{\text{OE}}$ clock)



● WRITE CYCLE (2) ($\overline{\text{OE}}$ Low Fix)



- NOTES: 1) A write occurs during the overlap of a low $\overline{\text{CS1}}$, a high $\overline{\text{CS2}}$ and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS1}}$ going low, $\overline{\text{CS2}}$ going high and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CS1}}$ going high, $\overline{\text{CS2}}$ going low and $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or $\overline{\text{CS2}}$ going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the end of write to the address change.
 t_{WR1} applies in case a write ends at $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high.
 t_{WR2} applies in case a write ends at $\overline{\text{CS2}}$ going low.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{\text{CS1}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
- 7) Dout is the same phase of the latest written data in this write cycle.
- 8) Dout is the read data of next address.
- 9) If $\overline{\text{CS1}}$ is low and $\overline{\text{CS2}}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

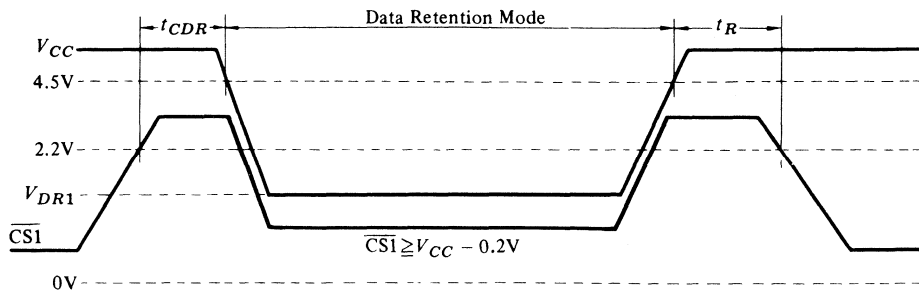
■ **LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70$ °C)**

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	-	-	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V, \overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	-	1	50*	μA
	I_{CCDR2}	$V_{CC} = 3.0V, CS2 \leq 0.2V$	-	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R					t_{RC}^{**}
						ns

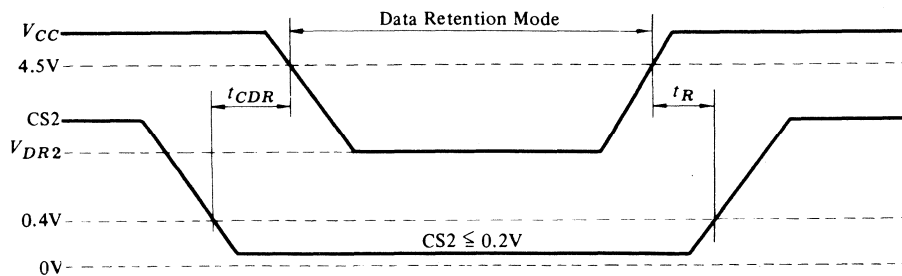
* V_{IL} min = -0.3V, 20 μA max at $T_a = 0 \sim 40^\circ C$

** t_{RC} = Read Cycle Time

● **LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)**

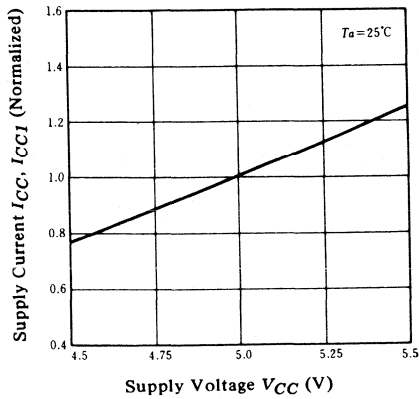


● **LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CS2$ Controlled)**

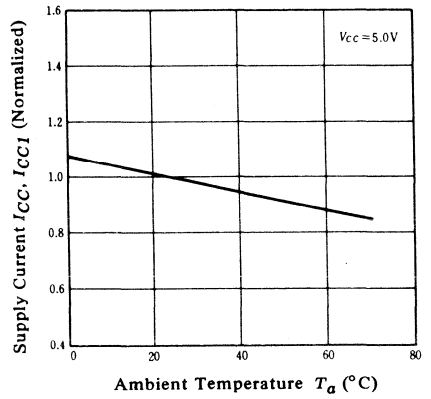


NOTE: In Data Retention Mode, $\overline{CS2}$ controls the Address, \overline{WE} , $\overline{CS1}$, \overline{OE} and Din buffer. If $\overline{CS2}$ controls data retention mode, Vin for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, $\overline{CS2}$ must satisfy either $CS2 > V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

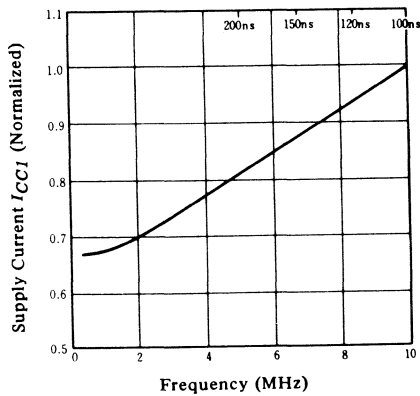
SUPPLY CURRENT vs. SUPPLY VOLTAGE



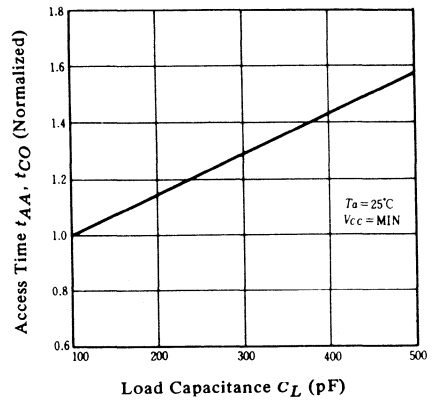
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



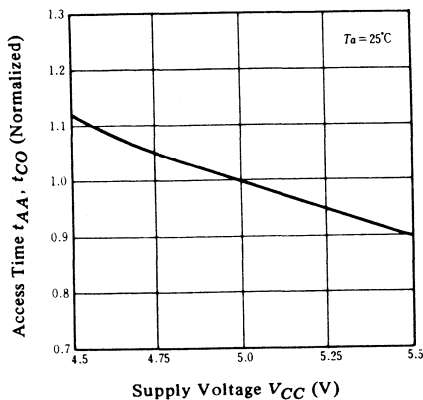
SUPPLY CURRENT vs. FREQUENCY



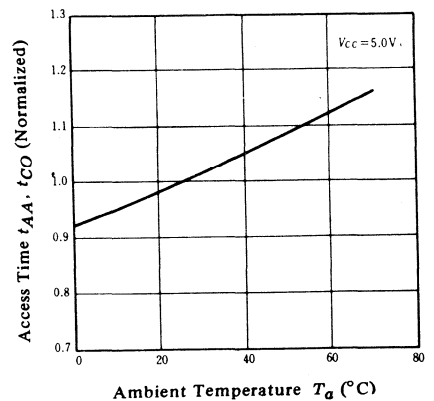
ACCESS TIME vs. LOAD CAPACITANCE



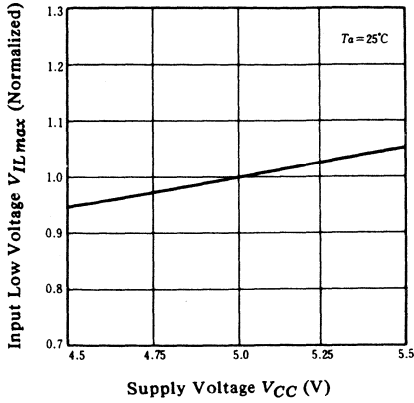
ACCESS TIME vs. SUPPLY VOLTAGE



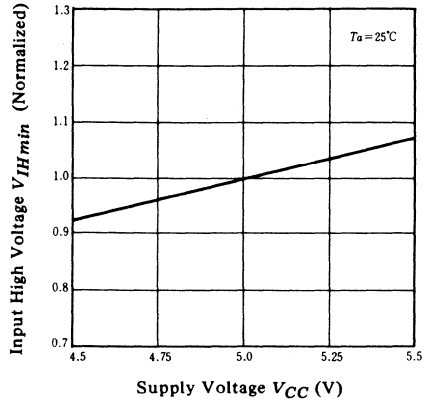
ACCESS TIME vs. AMBIENT TEMPERATURE



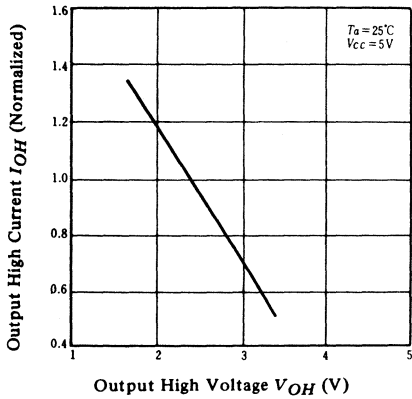
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



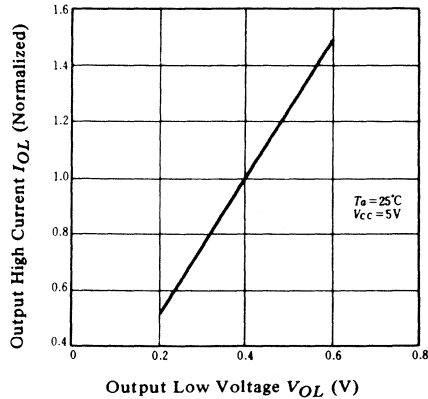
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



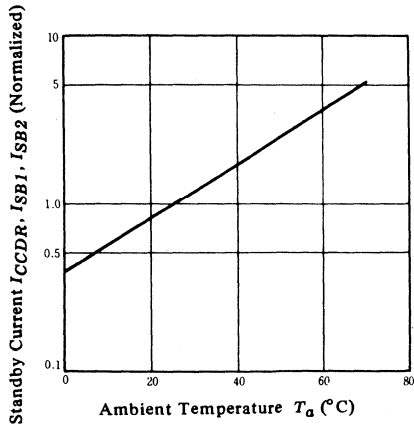
OUTPUT CURRENT vs. OUTPUT VOLTAGE



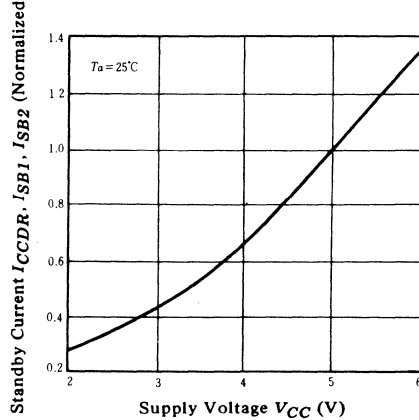
OUTPUT CURRENT vs. OUTPUT VOLTAGE



STANDBY CURRENT vs. AMBIENT TEMPERATURE



STANDBY CURRENT vs. SUPPLY VOLTAGE

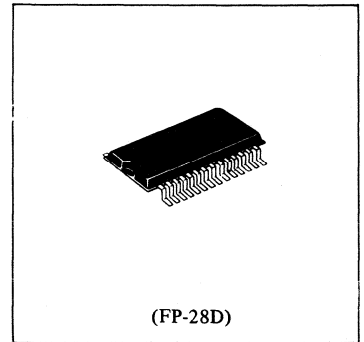


HM6264LFP Series

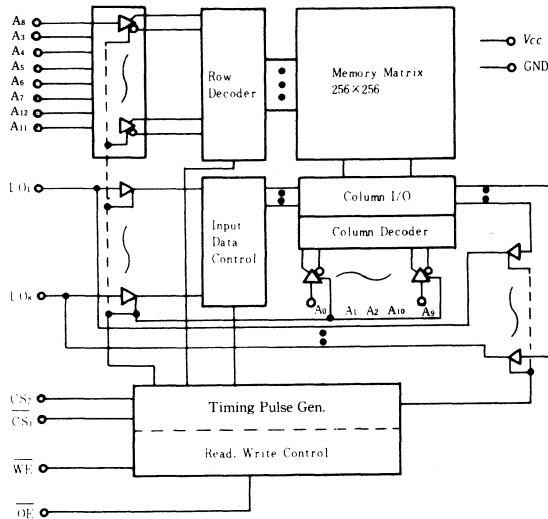
8192-word x 8-bit High Speed Static CMOS RAM

FEATURES

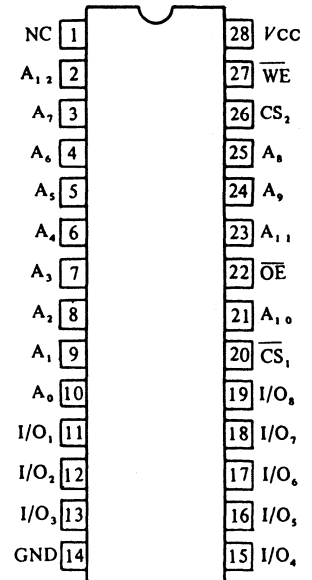
- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 100/120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
Standby: $10\mu\text{W}$ (typ.), Operation: 200mW (typ.)
- Capability of Battery Back-up Operation
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time



BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}\text{C}$
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}\text{C}$
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	$^{\circ}\text{C}$

* With respect to GND. ** Pulse width 50ns: -3.0V

TRUTH TABLE

$\overline{\text{WE}}$	$\overline{\text{CS}}_1$	$\overline{\text{CS}}_2$	$\overline{\text{OE}}$	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.3*	–	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	–	–	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\text{OE} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$, $V_{I/O} = \text{GND or } V_{CC}$	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O} = 0\text{mA}$	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	–	1	3	mA
	I_{SB1}^{**}	$\overline{\text{CS}}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	–	2	100	μA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	–	2	100	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	–	–	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.** V_{IL} min = -0.3V

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

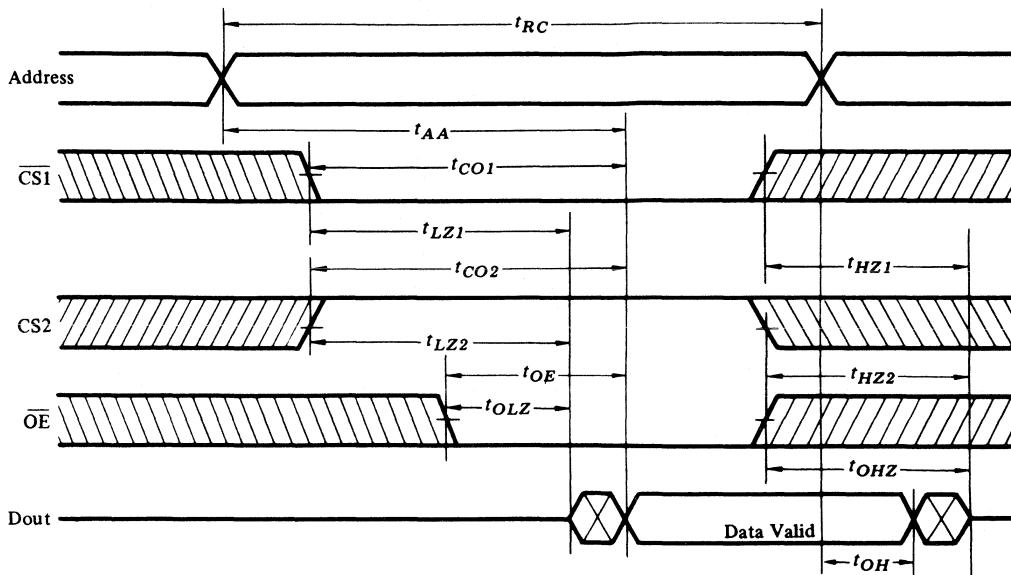
Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

● READ CYCLE

Item	Symbol	HM6264LFP-12		HM6264LFP-12		HM6264LFP-15		Unit	
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns	
Address Access Time	t_{AA}	–	100	–	120	–	150	ns	
Chip Selection to Output	$\overline{\text{CS}}1$	t_{CO1}	–	100	–	120	–	150	ns
	CS2	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid		t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$	t_{LZ1}	10	–	10	–	15	–	ns
	CS2	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z		t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$	t_{HZ1}	0	35	0	40	0	50	ns
	CS2	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z		t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change		t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

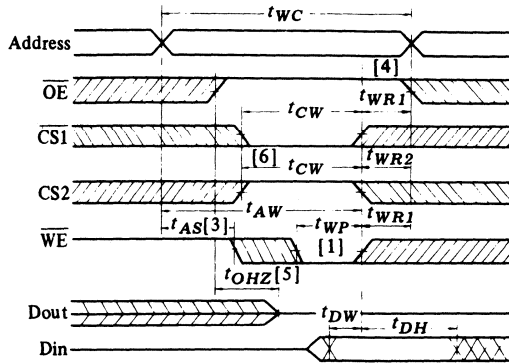


NOTE : 1) \overline{WE} is high for Read Cycle

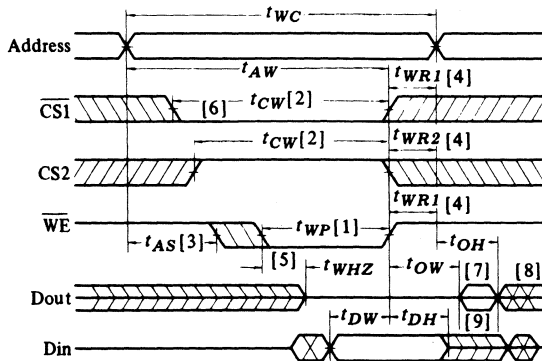
• WRITE CYCLE

Item	Symbol	HM6264LFP-10		HM6264LFP-12		HM6264LFP-15		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	80	—	85	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	80	—	85	—	100	—	ns
Write Pulse Width	t_{WP}	60	—	70	—	90	—	ns
Write Recovery Time	$\overline{CS1}, \overline{WE}$ t_{WR1}	5	—	5	—	10	—	ns
	CS2 t_{WR2}	15	—	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
\overline{OE} to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	—	5	—	10	—	ns

● WRITE CYCLE (1) ($\overline{\text{OE}}$ clock)



● WRITE CYCLE (2) ($\overline{\text{OE}}$ Low Fix)



- NOTES: 1) A write occurs during the overlap of a low $\overline{\text{CS1}}$, a high $\overline{\text{CS2}}$ and a low $\overline{\text{WE}}$. A write begins at the latest transition among $\overline{\text{CS1}}$ going low, $\overline{\text{CS2}}$ going high and $\overline{\text{WE}}$ going low. A write ends at the earliest transition among $\overline{\text{CS1}}$ going high, $\overline{\text{CS2}}$ going low and $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of $\overline{\text{CS1}}$ going low or $\overline{\text{CS2}}$ going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the end of write to the address change.
 t_{WR1} applies in case a write ends at $\overline{\text{CS1}}$ or $\overline{\text{WE}}$ going high.
 t_{WR2} applies in case a write ends at $\overline{\text{CS2}}$ going low.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{\text{CS1}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
- 7) t_{OH} is the same phase of the latest written data in this write cycle.
- 8) t_{DH} is the read data of next address.
- 9) If $\overline{\text{CS1}}$ is low and $\overline{\text{CS2}}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

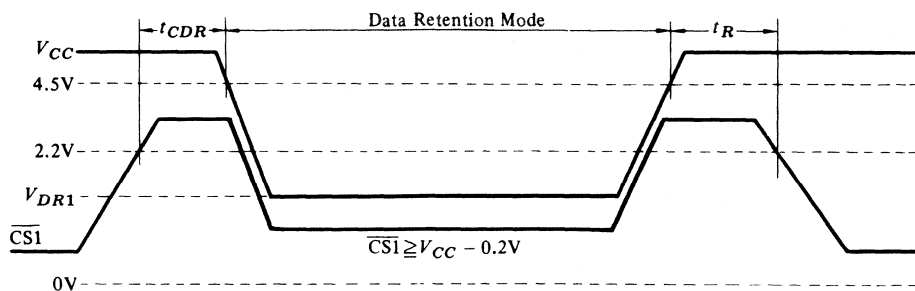
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70$ °C)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	-	-	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V, \overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	-	1	50*	μA
	I_{CCDR2}	$V_{CC} = 3.0V, CS2 \leq 0.2V$	-	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R		t_{RC}^{**}	-	-	ns

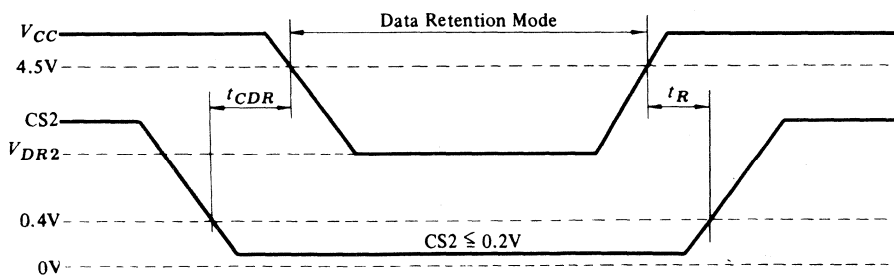
* V_{IL} min = -0.3V, 20 μA max at $T_a = 0 \sim +40$ °C.

** t_{RC} = Read Cycle Time

● LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



● LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CS2$ Controlled)



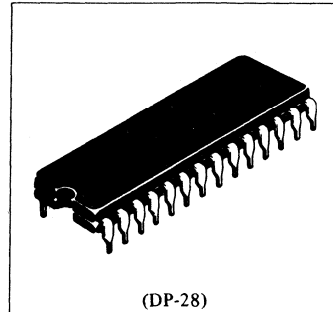
NOTE: In Data Retention Mode, $CS2$ controls the Address, \overline{WE} , $\overline{CS1}$, \overline{OE} and Din buffer. If $CS2$ controls data retention mode, V_{in} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, $CS2$ must satisfy either $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

HM6264LP-L Series

8192-word x 8-bit High Speed Static CMOS RAM

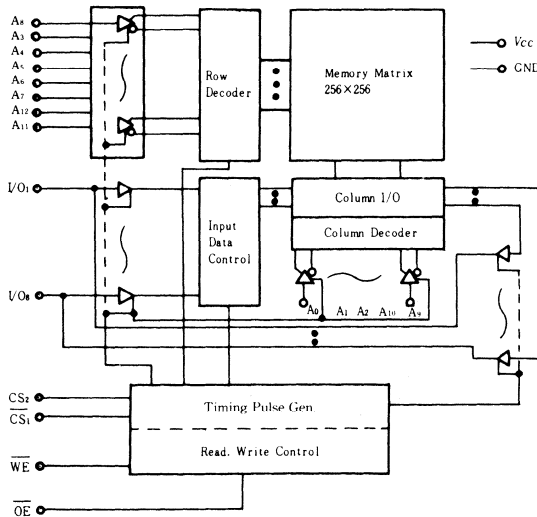
■ FEATURES

- Fast access Time 100ns/120ns/150ns (max.)
- Low Power Standby Standby: 0.01mW (typ.)
- Low Power Operation Operating: 200mW (typ.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output
- Standard 28pin Package Configuration
- Pin Out Compatible with 64K EPROM HN482764

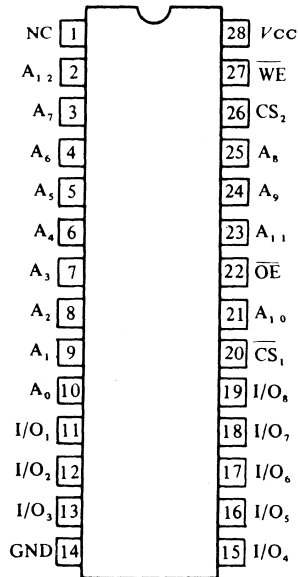


(DP-28)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

* With respect to GND. ** Pulse width 50ns: -3.0V

■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}, I_{SB1}	
X	X	L	X		High Z	I_{SB}, I_{SB2}	
H	L	H	H	Output Disabled	High Z	I_{CC}, I_{CC1}	
H	L	H	L	Read	Dout	I_{CC}, I_{CC1}	
L	L	H	H	Write	Din	I_{CC}, I_{CC1}	Write Cycle (1)
L	L	H	L		Din	I_{CC}, I_{CC1}	Write Cycle (2)

X: H or L

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.3*	–	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	I_{LI}	$V_{in} = \text{GND to } V_{CC}$	–	–	2	μA
Output Leakage Current	I_{LO}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\text{OE} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$, $V_{I/O} = \text{GND to } V_{CC}$	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\text{CS}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty = 100%, $I_{I/O} = 0\text{mA}$	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	–	1	3	mA
	I_{SB1}^{**}	$\text{CS}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	–	2	50	μA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	–	2	50	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	–	–	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.

** V_{IL} min = -0.3V

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	–	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

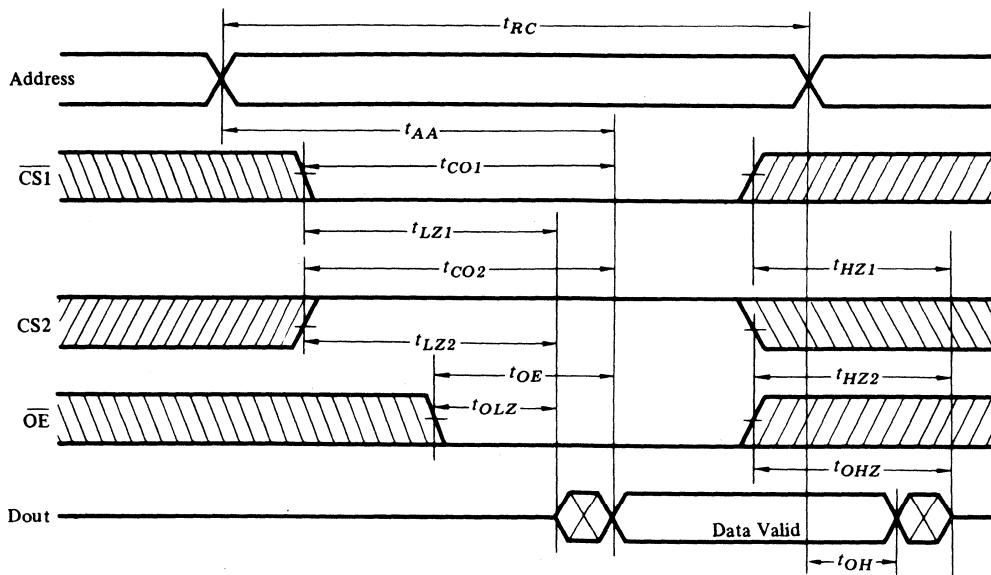
● READ CYCLE

Item	Symbol	HM6264LP-10L		HM6264LP-12L		HM6264LP-15L		Unit	
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns	
Address Access Time	t_{AA}	–	100	–	120	–	150	ns	
Chip Selection to Output	$\overline{\text{CS}}1$	t_{CO1}	–	100	–	120	–	150	ns
	$\text{CS}2$	t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns	
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$	t_{LZ1}	10	–	10	–	15	–	ns
	$\text{CS}2$	t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns	
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$	t_{HZ1}	0	35	0	40	0	50	ns
	$\text{CS}2$	t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Hold from Address Change	t_{OH}	10	–	10	–	15	–	ns	

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

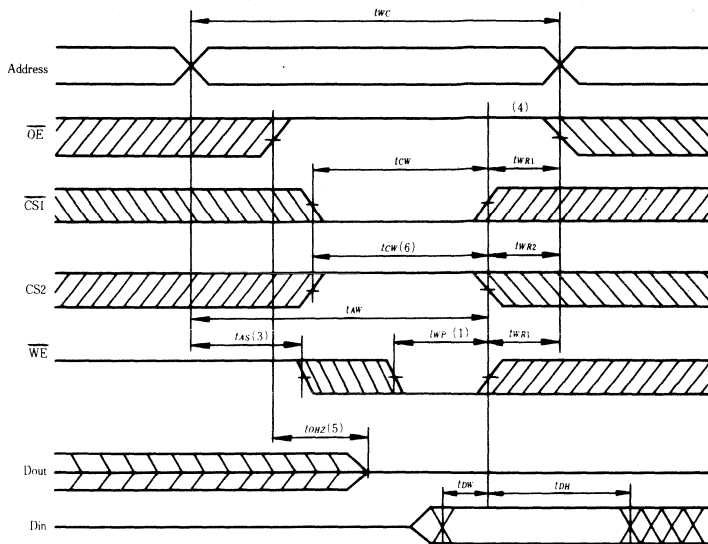


NOTE : 1) \overline{WE} is high for Read Cycle

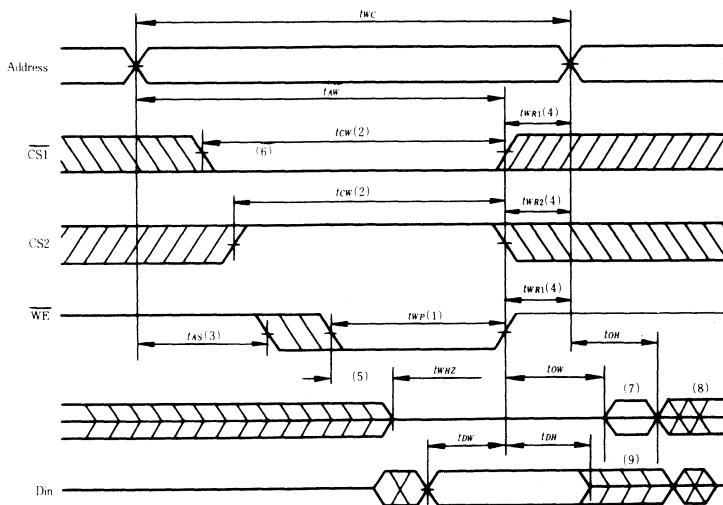
• WRITE CYCLE

Item	Symbol	HM6264LP-10L		HM6264LP-12L		HM6264LP-15L		Unit	
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	100	-	120	-	150	-	ns	
Chip Selection to End of Write	t_{CW}	80	-	85	-	100	-	ns	
Address Setup Time	t_{AS}	0	-	0	-	0	-	ns	
Address Valid to End of Write	t_{AW}	80	-	85	-	100	-	ns	
Write Pulse Width	t_{WP}	60	-	70	-	90	-	ns	
Write Recovery Time	CS1, WE	t_{WR1}	5	-	5	-	10	-	ns
	CS2	t_{WR2}	15	-	15	-	15	-	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns	
Data to Write Time Overlap	t_{DW}	40	-	50	-	60	-	ns	
Data Hold from Write Time	t_{DH}	0	-	0	-	0	-	ns	
\overline{OE} to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns	
Output Active from End of Write	t_{OW}	5	-	5	-	10	-	ns	

• WRITE CYCLE (1) (\overline{OE} clock)



• WRITE CYCLE (2) (\overline{OE} Low Fix)



- NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, $CS2$ going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low and \overline{WE} going high. tWP is measured from the beginning of write to the end of write.
- 2) tCW is measured from the later of $\overline{CS1}$ going low or $CS2$ going high to the end of write.
- 3) tAS is measured from the address valid to the beginning of write.
- 4) tWR is measured from the end of write to the address change.
 $tWR1$ applies in case a write ends at $\overline{CS1}$ or \overline{WE} going high.
 $tWR2$ applies in case a write ends at $CS2$ going low.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
- 7) $Dout$ is the same phase of the latest written data in this write cycle.
- 8) $Dout$ is the read data of next address.
- 9) If $\overline{CS1}$ is low and $CS2$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

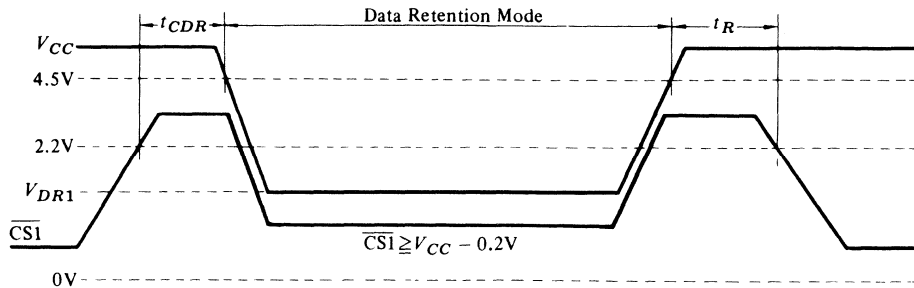
■ **LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)**

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2\text{V}, \overline{CS2} \geq V_{CC} - 0.2\text{V}$ or $\overline{CS2} \leq 0.2\text{V}$	2.0	-	-	V
	V_{DR2}	$\overline{CS2} \leq 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0\text{V}, \overline{CS1} \geq V_{CC} - 0.2\text{V}, \overline{CS2} \geq V_{CC} - 0.2\text{V}$ or $\overline{CS2} \leq 0.2\text{V}$	-	1	25*	μA
	I_{CCDR2}	$V_{CC} = 3.0\text{V}, \overline{CS2} \leq 0.2\text{V}$	-	1	25*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R					t_{RC}^{**}

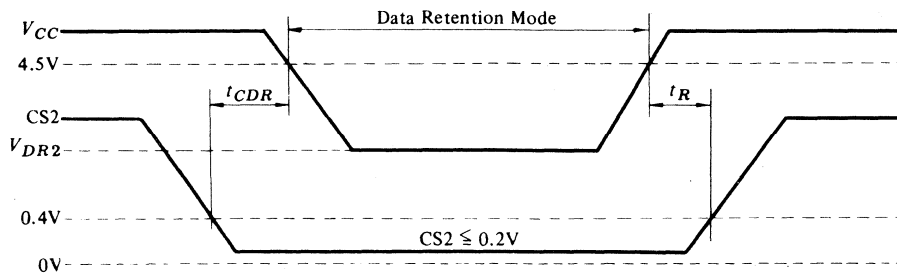
* V_{IL} min = -0.3V , $10\mu\text{A}$ max at $T_a = 0 \sim 40^\circ\text{C}$

** t_{RC} = Read Cycle Time

● **LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)**



● **LOW V_{CC} DATA RETENTION WAVEFORM (2) ($\overline{CS2}$ Controlled)**



NOTE: In Data Retention Mode, $\overline{CS2}$ controls the Address, \overline{WE} , $\overline{CS1}$, \overline{OE} and D_{in} buffer. If $\overline{CS2}$ controls data retention mode, V_{in} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, $\overline{CS2}$ must satisfy either $\overline{CS2} \geq V_{CC} - 0.2\text{V}$ or $\overline{CS2} \leq 0.2\text{V}$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

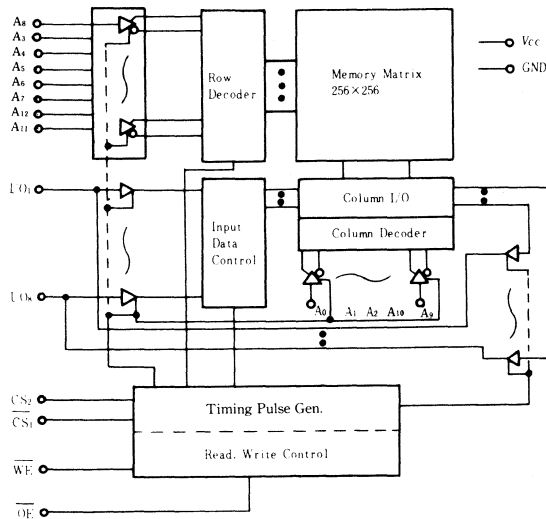
HM6264LFP-L Series

8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

- High Density Small-sized Packaged
- Projection Area Reduced to One-Thirds of Conventional DIP
- Thickness Reduced to a Half of Conventional DIP
- High Speed: Fast Access Time 120/150ns (max)
- Single 5V Supply
- Low Power Standby and Low Power Operation
Standby: 10 μ W (typ.), Operation: 200mW (typ.)
- Capability of Battery Back-up Operation
- Completely Static RAM: No clock nor Timing Strobe Required
- Directly TTL Compatible: All Input and Output
- Equal Access and Cycle Time

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

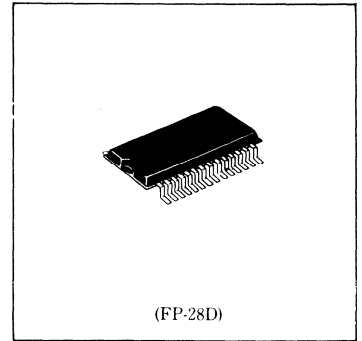
Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	$^{\circ}$ C

* With respect to GND. ** Pulse width 50ns: -3.0V

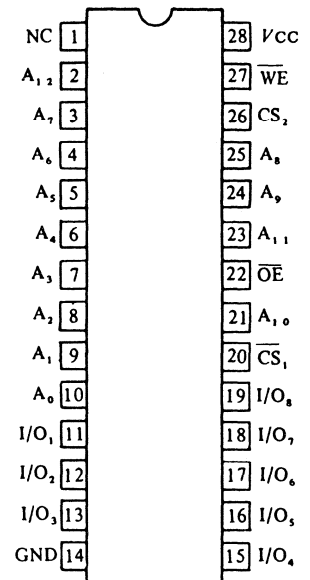
■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V_{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	/SB, /SB1	
X	X	L	X		High Z	/SB, /SB2	
H	L	H	H	Output Disabled	High Z	/CC, /CC1	
H	L	H	L	Read	Dout	/CC, /CC1	
L	L	H	H	Write	Din	/CC, /CC1	Write Cycle (1)
L	L	H	L		Din	/CC, /CC1	Write Cycle (2)

X: H or L



■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-0.3*	–	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	–	–	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$, $V_{I/O} = \text{GND or } V_{CC}$	–	–	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	–	40	80	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O} = 0\text{mA}$	–	60	110	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	–	1	3	mA
	I_{SB1}^{**}	$\overline{\text{CS}}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	–	2	50	μA
	I_{SB2}^{**}	$\text{CS}2 \leq 0.2\text{V}$	–	2	50	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	–	–	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.** V_{IL} min = -0.3V
■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	–	8	pF

(Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)
● AC TEST CONDITIONS

Input Pulse Levels: 0.8 to 2.4V

Input Rise and Fall Times: 10ns

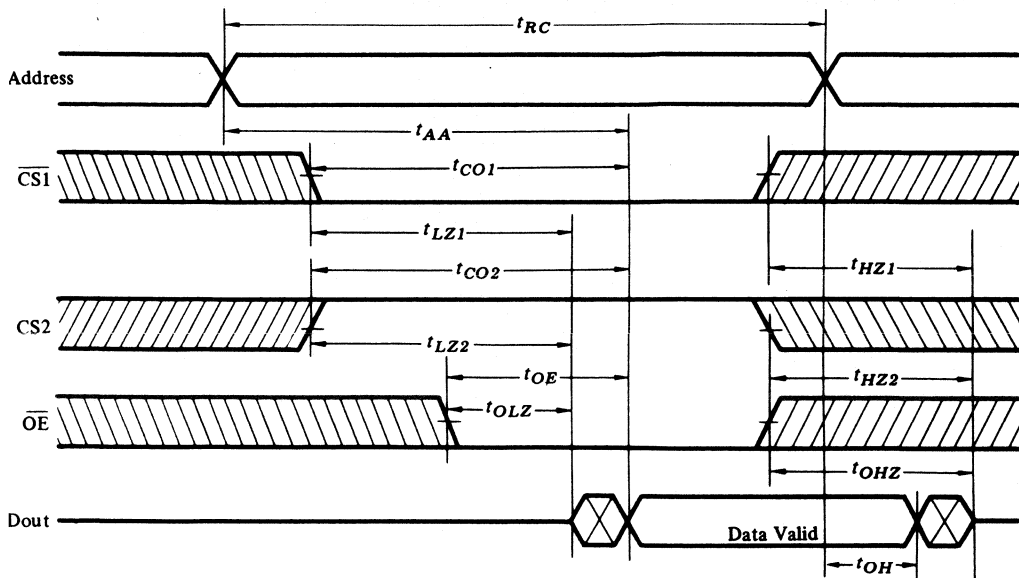
Input and Output Timing Reference Level: 1.5V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)
● READ CYCLE

Item	Symbol	HM6264LFP-10L		HM6264LFP-12L		HM6264LFP-15L		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	100	–	120	–	150	–	ns
Address Access Time	t_{AA}	–	100	–	120	–	150	ns
Chip Selection to Output	$\overline{\text{CS}}1$ t_{CO1}	–	100	–	120	–	150	ns
	$\text{CS}2$ t_{CO2}	–	100	–	120	–	150	ns
Output Enable to Output Valid	t_{OE}	–	50	–	60	–	70	ns
Chip Selection to Output in Low Z	$\overline{\text{CS}}1$ t_{LZ1}	10	–	10	–	15	–	ns
	$\text{CS}2$ t_{LZ2}	10	–	10	–	15	–	ns
Output Enable to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection to Output in High Z	$\overline{\text{CS}}1$ t_{HZ1}	0	35	0	40	0	50	ns
	$\text{CS}2$ t_{HZ2}	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Hold from Address Change	t_{OH}	10	–	10	–	15	–	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE

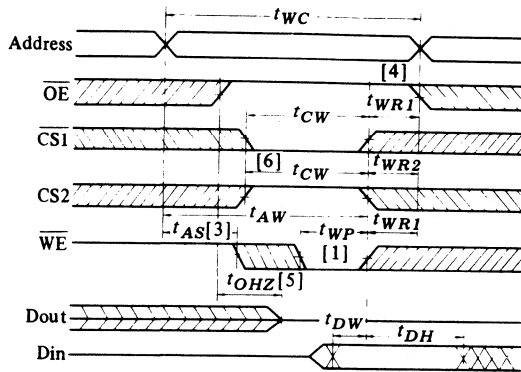


NOTE : 1) \overline{WE} is high for Read Cycle

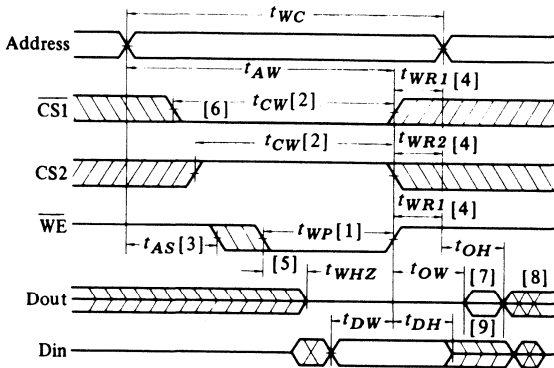
• WRITE CYCLE

Item	Symbol	HM6264LFP-10L		HM6264LFP-12L		HM6264LFP-15L		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	100	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	80	—	85	—	100	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	80	—	85	—	100	—	ns
Write Pulse Width	t_{WP}	60	—	70	—	90	—	ns
Write Recovery Time	CS1,WE t_{WR1}	5	—	5	—	10	—	ns
	CS2 t_{WR2}	15	—	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
OE to Output in High Z	t_{OHZ}	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	—	5	—	10	—	ns

• WRITE CYCLE (1) (\overline{OE} clock)



• WRITE CYCLE (2) (\overline{OE} Low Fix)



- NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high $\overline{CS2}$ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, $\overline{CS2}$ going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, $\overline{CS2}$ going low and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of $\overline{CS1}$ going low or $\overline{CS2}$ going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the end of write to the address change.
 t_{WR1} applies in case a write ends at $\overline{CS1}$ or \overline{WE} going high.
 t_{WR2} applies in case a write ends at $\overline{CS2}$ going low.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
- 7) D_{out} is the same phase of the latest written data in this write cycle.
- 8) D_{out} is the read data of next address.
- 9) If $\overline{CS1}$ is low and $\overline{CS2}$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

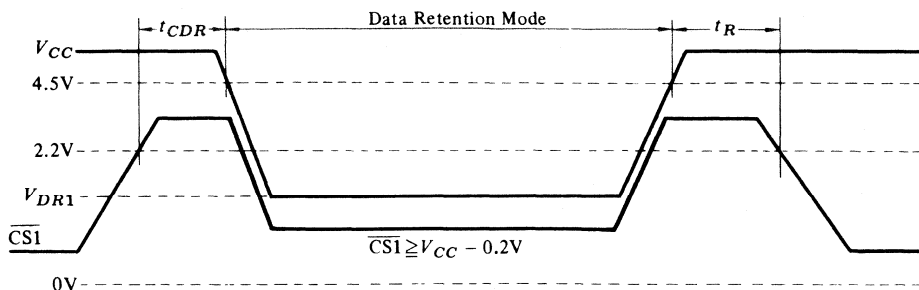
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70$ °C)

Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR1}	$\overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	2.0	-	-	V
	V_{DR2}	$CS2 \leq 0.2V$	2.0	-	-	V
Data Retention Current	I_{CCDR1}	$V_{CC} = 3.0V, \overline{CS1} \geq V_{CC} - 0.2V, CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$	-	1	25*	μA
	I_{CCDR2}	$V_{CC} = 3.0V, CS2 \leq 0.2V$	-	1	25*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R		t_{RC}^{**}	-	-	ns

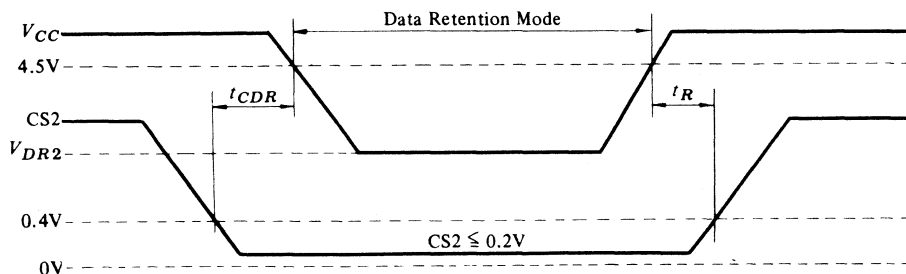
* V_{IL} min = $-0.3V$, $10\mu A$ max at $T_a = 0 \sim 40^\circ C$.

** t_{RC} = Read Cycle Time

● LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)



● LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CS2$ Controlled)



NOTE: In Data Retention Mode, $\overline{CS2}$ controls the Address, \overline{WE} , $\overline{CS1}$, \overline{OE} and Din buffer. If $CS2$ controls data retention mode, V_{in} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, $CS2$ must satisfy either $CS2 \geq V_{CC} - 0.2V$ or $CS2 \leq 0.2V$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

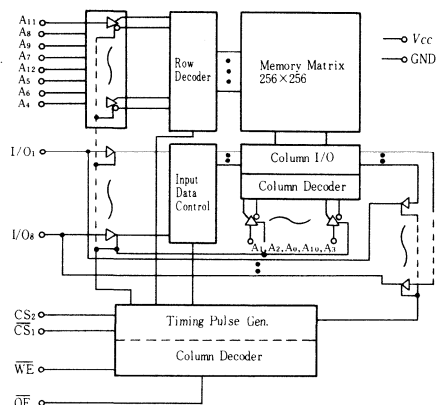
HM6264ASP Series, HM6264AFP Series

8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

- High Density 300 mil 28 pin Package
- Low Power Standby Standby: 0.1mW (typ.)
- Low Power Operation Operating: 15mW/MHz (typ.)
- Fast access Time 120ns/150ns (max.)
- Single +5V Supply
- Completely Static Memory. . . . No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

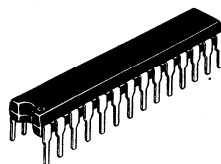
* With respect to GND. ** Pulse width 50ns: 3.0V

■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V _{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB}/I_{SB1}	
X	X	L	X		High Z	I_{SB}/I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

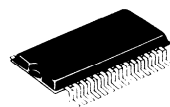
X: H or L

HM6264ASP Series



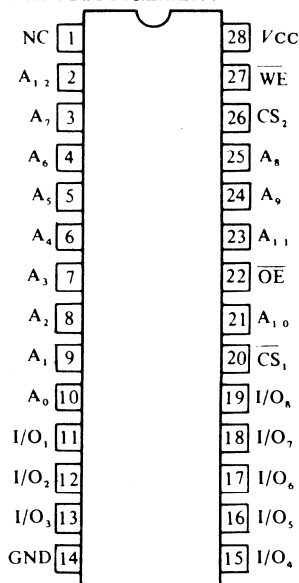
(DP-28N)

HM6264AFP Series



(FP-28D)

■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	--	6.0	V
	V_{IL}	-0.3*	--	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	--	--	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$ or $\overline{\text{OE}} = V_{IH}$ or $\overline{\text{WE}} = V_{IL}$, $V_{I/O} = \text{GND to } V_{CC}$	--	--	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	--	7	15	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{\text{CS}}1 = V_{IL}$, $\text{CS}2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	--	30	45	mA
	I_{CC2}	Cycle = $1\mu\text{s}$, duty = 100%, $I_{I/O} = 0\text{mA}$, $\overline{\text{CS}}1 \leq 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$, $V_{IH} \geq V_{CC} - 0.2\text{V}$, $V_{IL} \leq 0.2\text{V}$	--	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}}1 = V_{IH}$ or $\text{CS}2 = V_{IL}$	--	1	3	mA
	I_{SB1}^{**}	$\overline{\text{CS}}1 \geq V_{CC} - 0.2\text{V}$, $\text{CS}2 \geq V_{CC} - 0.2\text{V}$ or $\text{CS}2 \leq 0.2\text{V}$	--	0.02	2	mA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	--	--	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	--	--	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading. ** $V_{IL} \text{ min} = -0.3\text{V}$

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	--	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	--	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)

■ AC TEST CONDITIONS

Input Pulse Levels: 0.8V/2.4V

Input Rise and Fall Time: 10ns

Input Timing Reference Level: 1.5V

Output Timing Reference Level: 0.8V/2.0V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

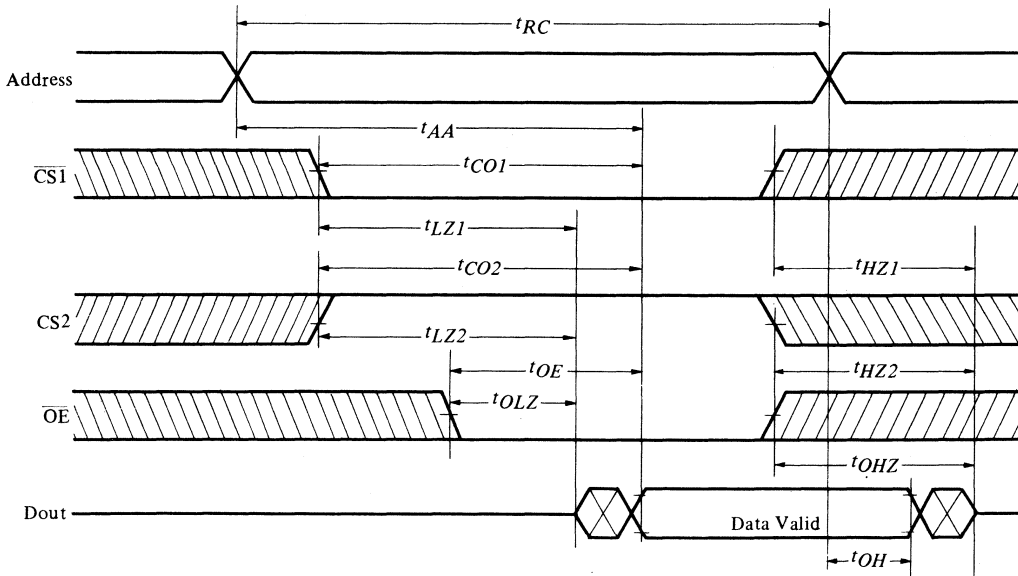
• READ CYCLE

Item	Symbol	HM6264ASP/FP-12		HM6264ASP/FP-15		Unit	
		min	max	min	max		
Read Cycle Time	t_{RC}	120	—	150	—	ns	
Address Access Time	t_{AA}	—	120	—	150	ns	
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	—	120	—	150	ns
	$CS2$	t_{CO2}	—	120	—	150	ns
Output Enable to Output Valid	t_{OE}	—	60	—	70	ns	
Chip Selection to Output in Low Z	$CS1$	t_{LZ1}	10	—	10	—	ns
	$CS2$	t_{LZ2}	10	—	10	—	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	ns	
Chip Deselection to Output in High Z	$CS1$	t_{HZ1}	0	40	0	50	ns
	$CS2$	t_{HZ2}	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	ns	
Output Hold from Address Change	t_{OH}	10	—	10	—	ns	

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

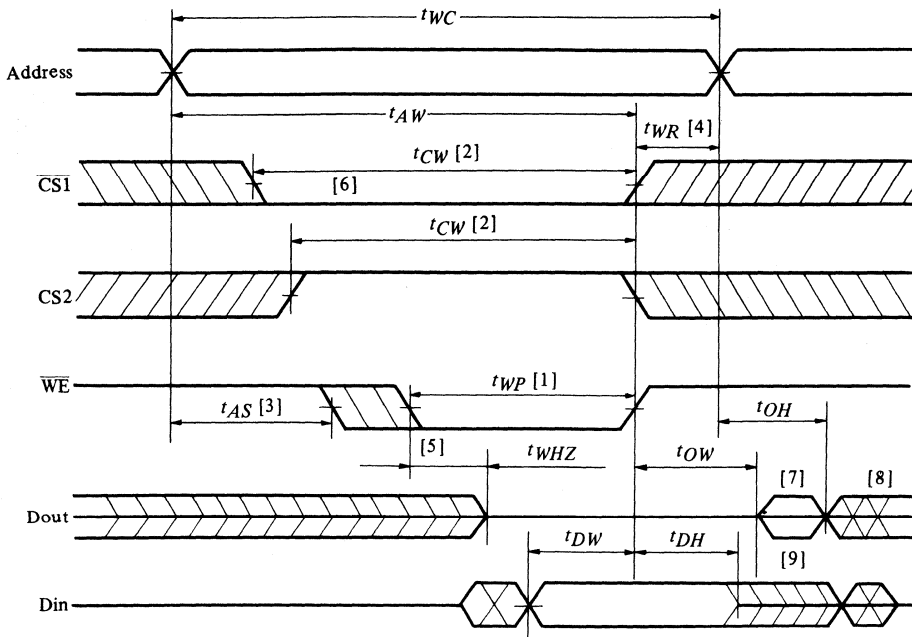
2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

• READ CYCLE



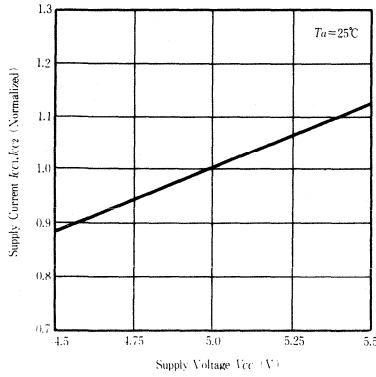
NOTE: 1) \overline{WE} is high for Read Cycle

• WRITE CYCLE (2) (\overline{OE} Low Fix)

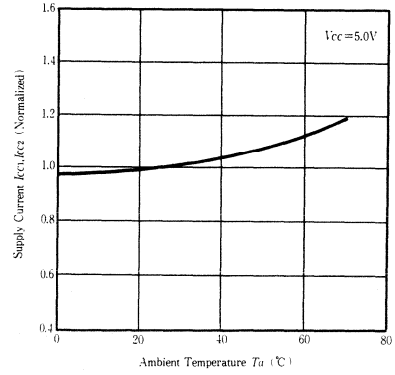


- NOTES: 1) A write occurs during the overlap of a low $\overline{CS1}$, a high $CS2$ and a low \overline{WE} . A write begins at the latest transition among $\overline{CS1}$ going low, $CS2$ going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, $CS2$ going low and \overline{WE} going high, t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of $\overline{CS1}$ going low or $CS2$ going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or $CS2$ going low to the end of write cycle.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
- 7) Dout is the same phase of the latest written data in this write cycle.
- 8) Dout is the read data of next address.
- 9) If $\overline{CS1}$ is low and $CS2$ is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

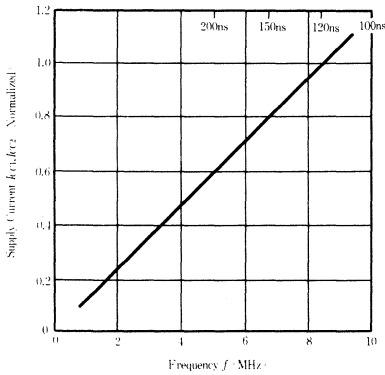
SUPPLY CURRENT VS. SUPPLY VOLTAGE



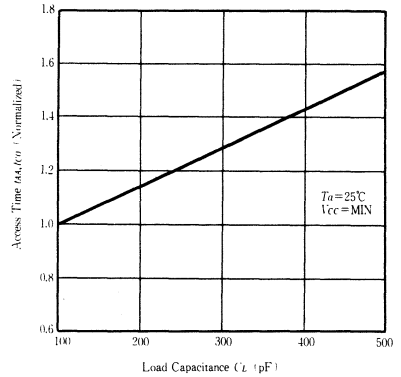
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



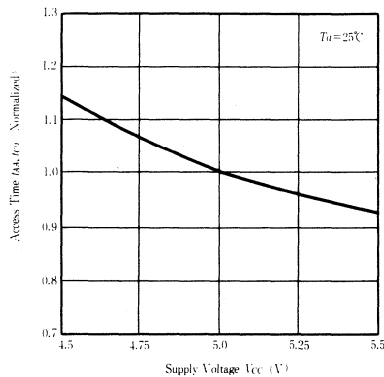
SUPPLY CURRENT VS. FREQUENCY



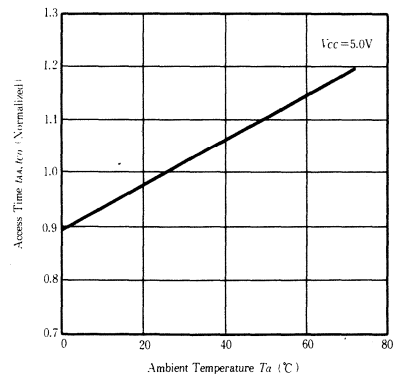
ACCESS TIME VS. LOAD CAPACITANCE



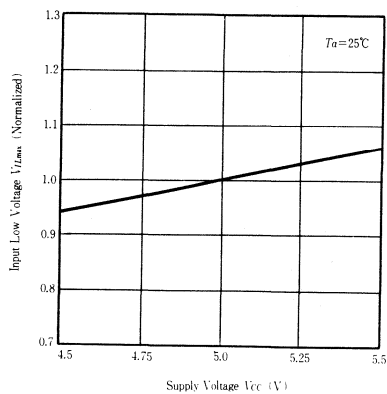
ACCESS TIME VS. SUPPLY VOLTAGE



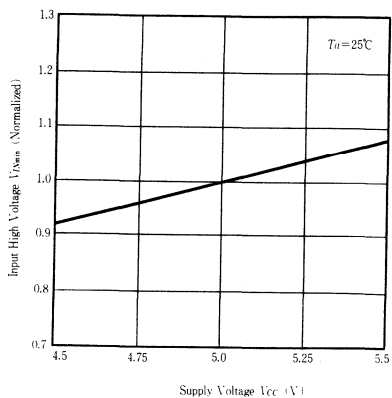
ACCESS TIME VS. AMBIENT TEMPERATURE



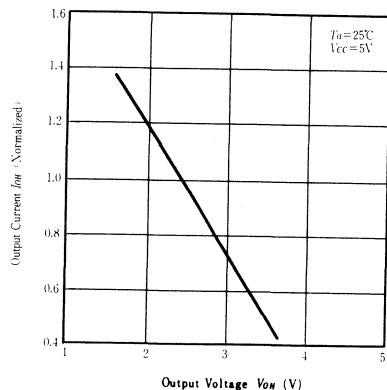
INPUT LOW VOLTAGE VS. SUPPLY VOLTAGE



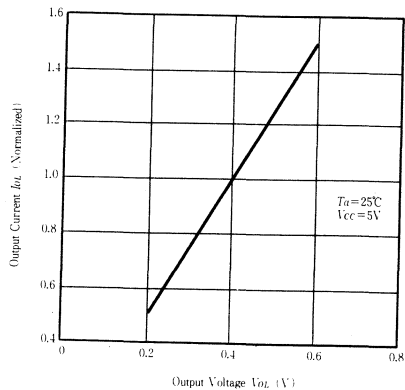
INPUT HIGH VOLTAGE VS. SUPPLY VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



OUTPUT CURRENT VS. OUTPUT VOLTAGE



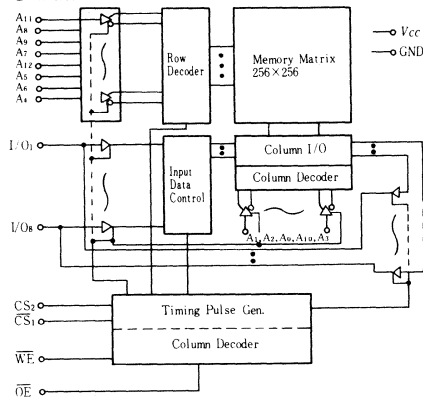
HM6264ALSP Series, HM6264ALFP Series

8192-word x 8-bit High Speed Static CMOS RAM

■ FEATURES

- High Density 300 mil 28pin Package
- Low Power Standby Standby: 0.01mW (typ.)
- Low Power Operation Operating: 15mW/MHz (typ.)
- Fast access Time 120ns/150ns (max.)
- Capability of Battery Back-up Operation
- Single +5V Supply
- Completely Static Memory. No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three State Output
- Directly TTL Compatible: All Input and Output

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage *	V_T	-0.5 ** to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (Under Bias)	T_{bias}	-10 to +85	°C

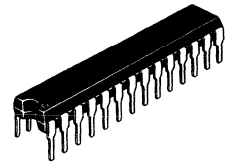
* With respect to GND. ** Pulse width 50ns: -3.0V

■ TRUTH TABLE

WE	CS ₁	CS ₂	OE	Mode	I/O Pin	V _{CC} Current	Note
X	H	X	X	Not Selected (Power Down)	High Z	I_{SB1}	
X	X	L	X		High Z	I_{SB1}	
H	L	H	H	Output Disabled	High Z	I_{CC}	
H	L	H	L	Read	Dout	I_{CC}	
L	L	H	H	Write	Din	I_{CC}	Write Cycle (1)
L	L	H	L		Din	I_{CC}	Write Cycle (2)

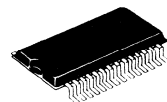
X: H or L

HM6264ALSP Series



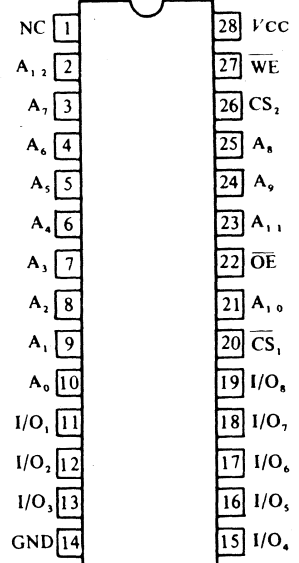
(DP-28N)

HM6264ALFP Series



(FP-28D)

■ PIN ARRANGEMENT



(Top View)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-0.3*	-	0.8	V

* Pulse Width 50ns: -3.0V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{in} = \text{GND to } V_{CC}$	-	-	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$ or $\text{OE} = V_{IH}$ or $\overline{WE} = V_{IL}$, $V_{I/O} = \text{GND to } V_{CC}$	-	-	2	μA
Operating Power Supply Current	I_{CCDC}	$\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	-	7	5	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $\overline{CS1} = V_{IL}$, $CS2 = V_{IH}$, $I_{I/O} = 0\text{mA}$	-	30	45	mA
	I_{CC2}	Cycle = $1\mu\text{s}$, duty = 100%, $I_{I/O} = 0\text{mA}$, $\overline{CS1} \leq 0.2\text{V}$, $CS2 \geq V_{CC} - 0.2\text{V}$, $V_{IH} \geq V_{CC} - 0.2\text{V}$, $V_{IL} \leq 0.2\text{V}$	-	3	5	mA
Standby Power Supply Current	I_{SB}	$\overline{CS1} = V_{IH}$ or $CS2 = V_{IL}$	-	1	3	mA
	I_{SB1}^{**}	$\overline{CS1} \geq V_{CC} - 0.2\text{V}$, $CS2 \geq V_{CC} - 0.2\text{V}$ or $CS2 \leq 0.2\text{V}$	-	2	1	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.4	V
	V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	-	-	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading. ** V_{IL} min = -0.3V

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Condition	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0\text{V}$	-	7	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$)
● AC TEST CONDITIONS

Input Pulse Levels: 0.8V/2.4V

Input Rise and Fall Time: 10ns

Input Timing Reference Level: 1.5V

Output Timing Reference Level: 0.8V/2.0V

Output Load: 1TTL Gate and $C_L = 100\text{pF}$ (including scope and jig)

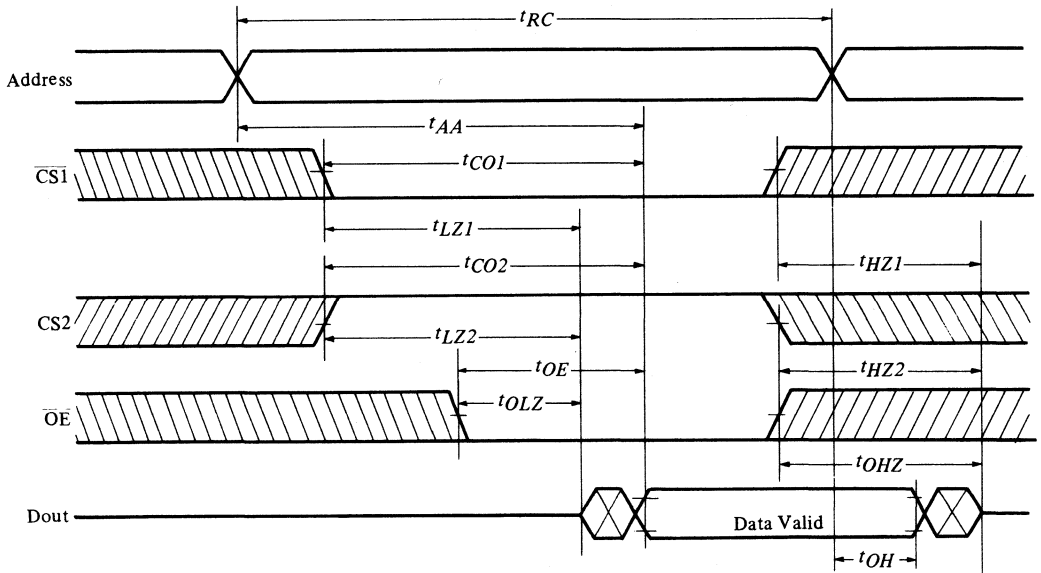
● READ CYCLE

Item	Symbol	HM6264ALSP/FP-12		HM6264ALSP/FP-15		Unit
		min	max	min	max	
Read Cycle Time	t_{RC}	120	—	150	—	ns
Address Access Time	t_{AA}	—	120	—	150	ns
Chip Selection to Output	$\overline{CS1}$	t_{CO1}	—	120	—	ns
	CS2	t_{CO2}	—	120	—	ns
Output Enable to Output Valid	t_{OE}	—	60	—	70	ns
Chip Selection to Output in Low Z	$\overline{CS1}$	t_{LZ1}	10	—	10	ns
	CS2	t_{LZ2}	10	—	10	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	ns
Chip Deselection to Output in High Z	$\overline{CS1}$	t_{HZ1}	0	40	0	50
	CS2	t_{HZ2}	0	40	0	50
Output Disable to Output in High Z	t_{OHZ}	0	40	0	50	ns
Output Hold from Address Change	t_{OH}	10	—	10	—	ns

NOTES: 1 t_{HZ} and t_{OHZ} are defined as the time at which the outputs achieve the open circuit condition and are not referred to output voltage levels.

2 At any given temperature and voltage condition, t_{HZ} max is less than t_{LZ} min both for a given device and from device to device.

● READ CYCLE

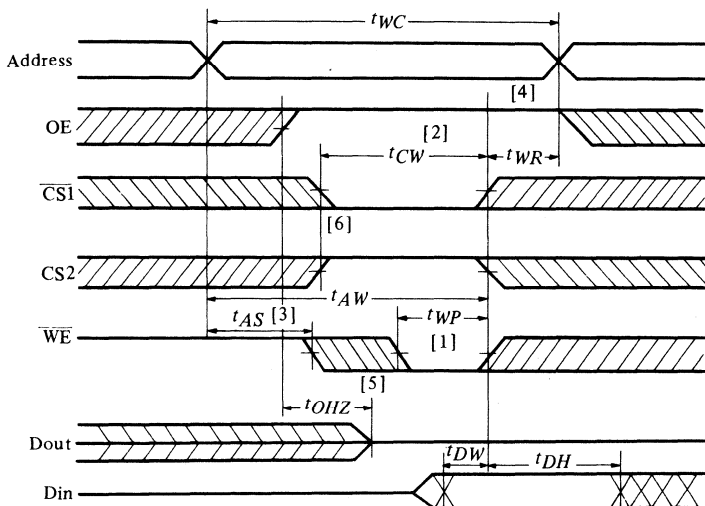


NOTE : 1) \overline{WE} is high for Read Cycle

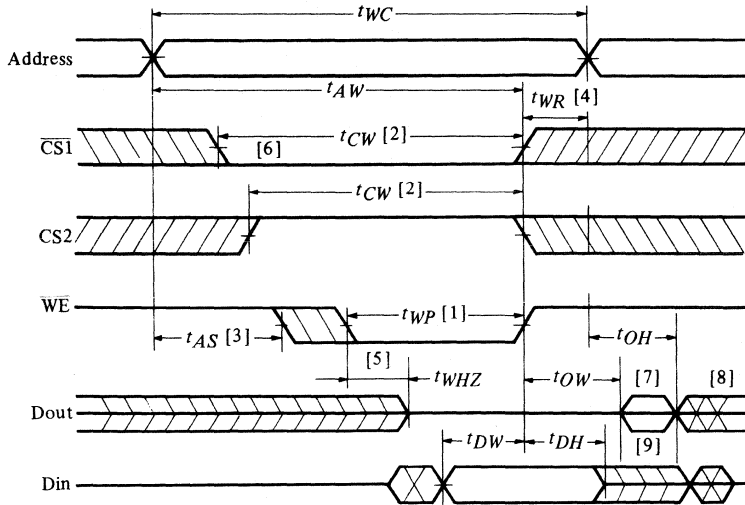
• WRITE CYCLE

Item	Symbol	HM6264ALSP/FP-12		HM6264ALSP/FP-15		Unit
		min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	100	—	120	—	ns
Address Setup Time	t_{AS}	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	100	—	120	—	ns
Write Pulse Width	t_{WP}	80	—	100	—	ns
Write Recovery Time	t_{WR}	0	—	0	—	ns
Write to Output in High Z	t_{WHZ}	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	50	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	ns
Output Enable to Output in High Z	t_{OHZ}	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	—	5	—	ns

• WRITE CYCLE (1) (\overline{OE} clock)



• WRITE CYCLE (2) (\overline{OE} Low Fix)



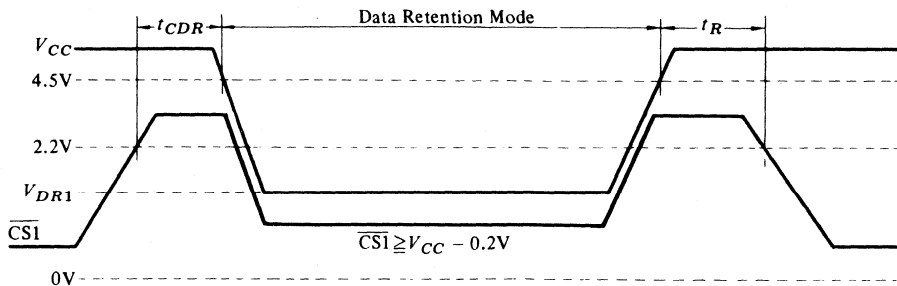
- NOTES: 1) A write occurs during the overlap of a low CS1, a high CS2 and a low WE. A write begins at the latest transition among $\overline{CS1}$ going low, CS2 going high and \overline{WE} going low. A write ends at the earliest transition among $\overline{CS1}$ going high, CS2 going low and \overline{WE} going high. t_{WP} is measured from the beginning of write to the end of write.
- 2) t_{CW} is measured from the later of $\overline{CS1}$ going low or CS2 going high to the end of write.
- 3) t_{AS} is measured from the address valid to the beginning of write.
- 4) t_{WR} is measured from the earliest of $\overline{CS1}$ or \overline{WE} going high or CS2 going low to the end of write cycle.
- 5) During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
- 6) If $\overline{CS1}$ goes low simultaneously with \overline{WE} going low or after \overline{WE} going low, the outputs remain in high impedance state.
- 7) Dout is the same phase of the latest written data in this write cycle.
- 8) Dout is the read data of next address.
- 9) If $\overline{CS1}$ is low and CS2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.

■ **LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)**

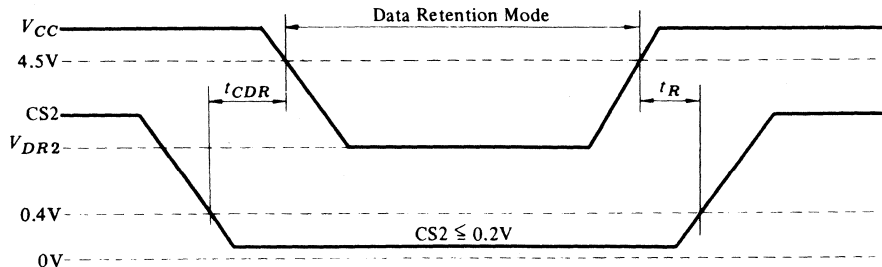
Item	Symbol	Test Condition	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$CS1 \geq V_{CC} - 0.2\text{V}$, $CS2 \geq V_{CC} - 0.2\text{V}$ or $CS2 \leq 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0\text{V}$ $CS1 \geq V_{CC} - 0.2\text{V}$, $CS2 \geq V_{CC} - 0.2\text{V}$ or $CS2 \leq 0.2\text{V}$	-	1	50*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R		t_{RC}^{**}	-	-	ns

* V_{IL} min = -0.3V , $20\mu\text{A}$ max at $T_a = 0 \sim 40^\circ\text{C}$
 ** t_{RC} = Read Cycle Time

● **LOW V_{CC} DATA RETENTION WAVEFORM (1) ($\overline{CS1}$ Controlled)**

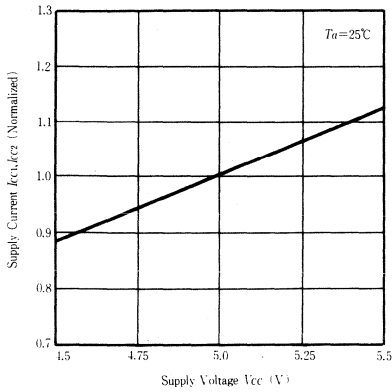


● **LOW V_{CC} DATA RETENTION WAVEFORM (2) ($CS2$ Controlled)**

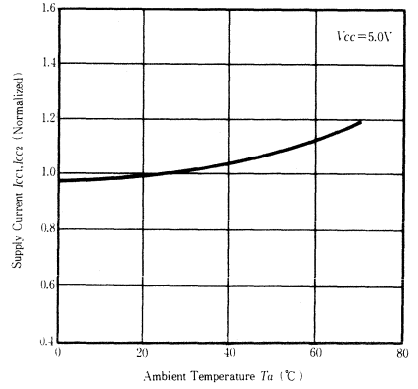


NOTE: In Data Retention Mode, $CS2$ controls the Address, \overline{WE} , $\overline{CS1}$, \overline{OE} and Din buffer. If $CS2$ controls data retention mode, V_{in} for these inputs can be in the high impedance state. If $\overline{CS1}$ controls the data retention mode, $CS2$ must satisfy either $CS2 \geq V_{CC} - 0.2\text{V}$ or $CS2 \leq 0.2\text{V}$. The other input levels (address, \overline{WE} , \overline{OE} , I/O) can be in the high impedance state.

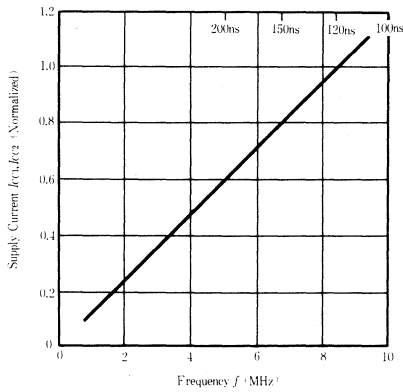
SUPPLY CURRENT VS. SUPPLY VOLTAGE



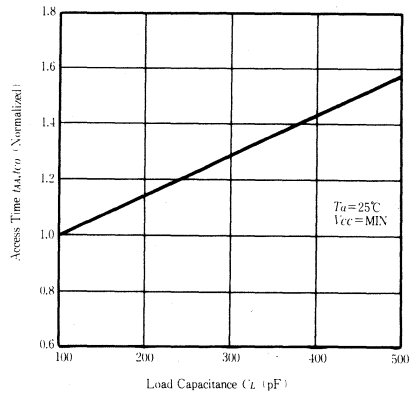
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



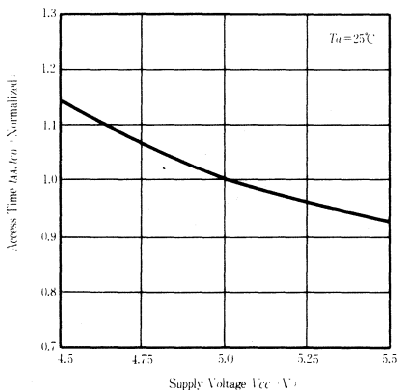
SUPPLY CURRENT VS. FREQUENCY



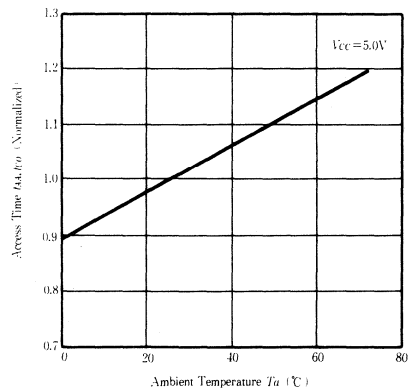
ACCESS TIME VS. LOAD CAPACITANCE



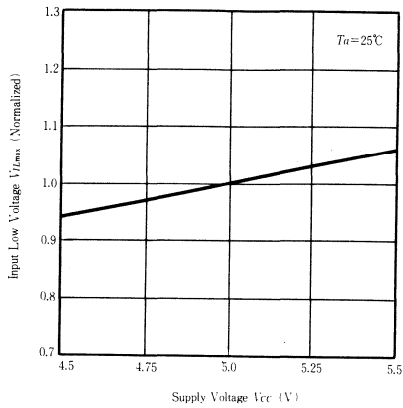
ACCESS TIME VS. SUPPLY VOLTAGE



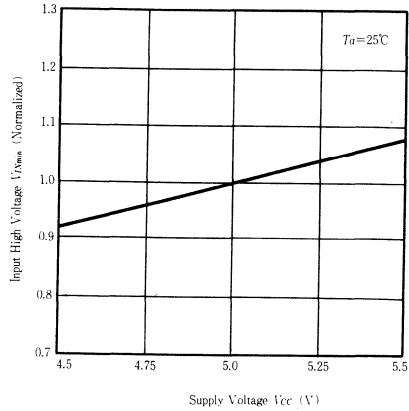
ACCESS TIME VS. AMBIENT TEMPERATURE



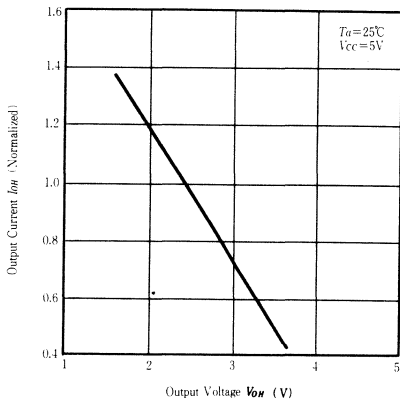
**INPUT LOW VOLTAGE
VS. SUPPLY VOLTAGE**



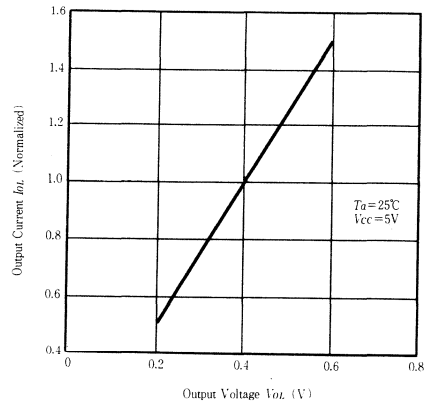
**INPUT HIGH VOLTAGE
VS. SUPPLY VOLTAGE**



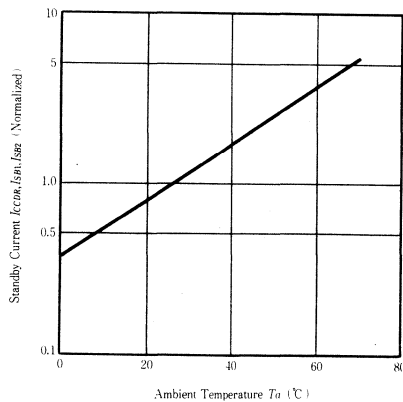
**OUTPUT CURRENT VS.
OUTPUT VOLTAGE**



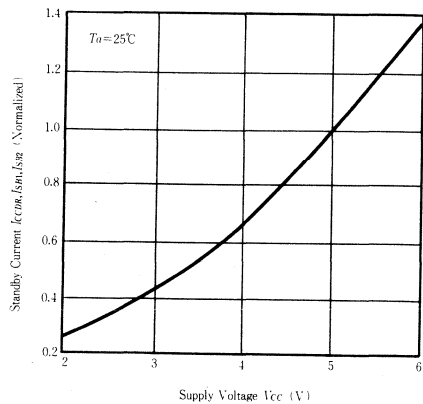
**OUTPUT CURRENT VS.
OUTPUT VOLTAGE**



**STANDBY CURRENT VS.
AMBIENT TEMPERATURE**



**STANDBY CURRENT VS.
SUPPLY VOLTAGE**

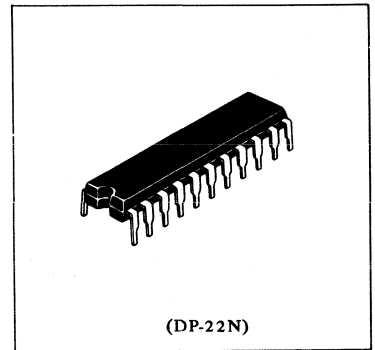
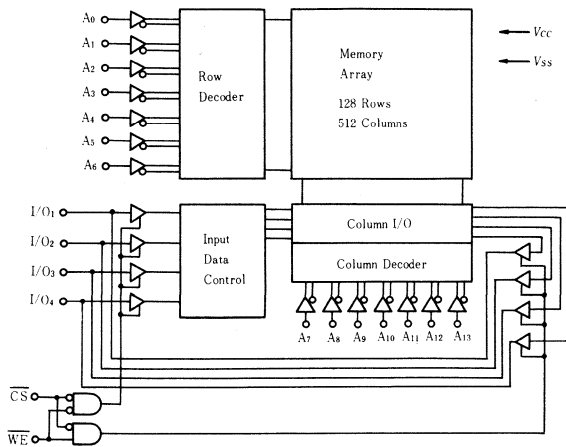


16384-word × 4-bit High Speed Static CMOS RAM

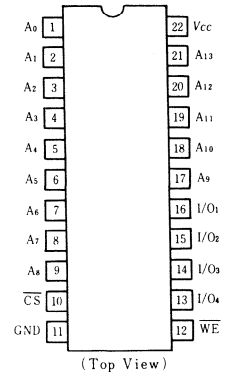
FEATURES

- Single 5V Supply and High Density 22 Pin Package.
- High Speed: Fast Access Time 35/45/55 ns (max).
- Low Power Standby and Low Power Operation 100μW typ. (Standby) 300mW typ. (Op.).
- Completely Static Memory
No Clock or Timing Strobe Required.
- Equal Access and Cycle Times.
- Directly TTL Compatible – All Inputs and Outputs.

BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{IN}	-3.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{op}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{vbb}	-10 to +85	°C

* Pulse Width 20ns, DC = -0.5V

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Ref. Cycle
H	×	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	Din	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	—	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-3.0*	—	0.8	V

* Pulse width 10ns DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 10\%$, $\text{GND}=0\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC}=\text{MAX. } V_{IN}=\text{GND to } V_{CC}$	—	—	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}, V_{I/O}=\text{GND to } V_{CC}$	—	—	10	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}, I_{I/O}=0\text{mA}$	—	60	TBD	mA
Standby Power Supply Current	I_{SB}	$\overline{CS}=V_{IH}$	—	15	TBD	mA
Standby Power Supply Current (1)	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\text{V}, V_{IN} \leq 0.2\text{V}$ or $V_{IX} \geq V_{CC} - 0.2\text{V}$	—	0.02	2.0	mA
Output Low Voltage	V_{OL}	$I_{OL}=8\text{mA}$	—	—	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-4.0\text{mA}$	2.4	—	—	V

Note:1. Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1.0\text{MHz}$)

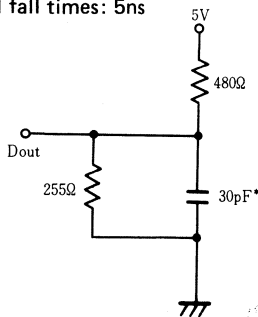
Parameter	Symbol	Test Conditions	min	max	Unit
Input Capacitance	C_{IN}	$V_{IN}=0\text{V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	—	10	pF

Note: This parameter is sampled and not 100% tested

■ AC CHARACTERISTICS

- AC Test Conditions
 Input pulse levels: GND to 3.0V
 Input rise and fall times: 5ns

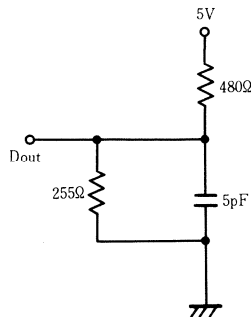
Input and Output timing reference levels: 1.5V
 Output load: See Figure



Output Load (A)

*Including scope & jig.

Output Load (A)



Output Load (B)

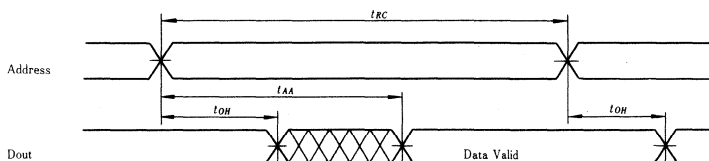
(for t_{HZ} , t_{LZ} , t_{WZ} & t_{OW})

■ **READ CYCLE** ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 10\%$, unless otherwise noted.)

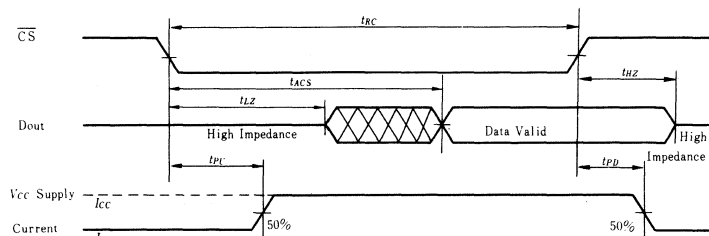
Parameter	Symbol	HM6288P-35		HM6288P-45		HM6288P-55		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	35	—	45	—	55	—	ns
Address Access Time	t_{AA}	—	35	—	45	—	55	ns
Chip Select Access Time	t_{ACS}	—	35	—	45	—	55	ns
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns
Chip Selection to Output in Low Z	t_{LZ}^*	10	—	10	—	10	—	ns
Chip Deselection to Output in High Z	t_{HZ}^*	0	20	0	20	0	20	ns
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns
Chip Deselection to Power Down Time	t_{PD}	—	30	—	30	—	30	ns

* Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● **Timing Waveform of Read Cycle No.1** [1] [2]



● **Timing Waveform of Read Cycle No.2** [1] [3]



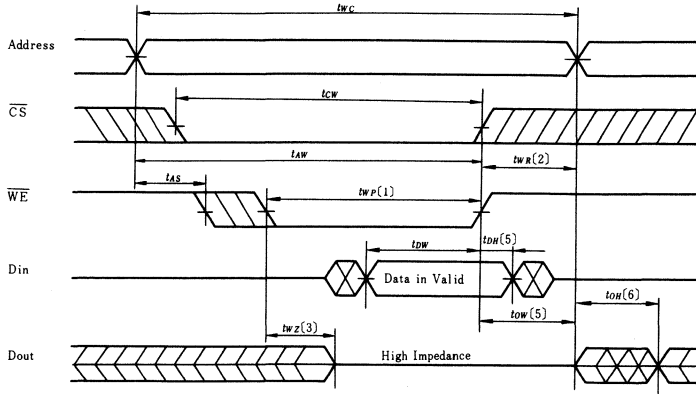
Notes: 1. $\overline{\text{WE}}$ is High for Read Cycle.
2. Device is continuously selected, $\overline{\text{CS}} = V_{IL}$.
3. Address Valid prior to or coincident with $\overline{\text{CS}}$ transition Low.

■ **WRITE CYCLE**

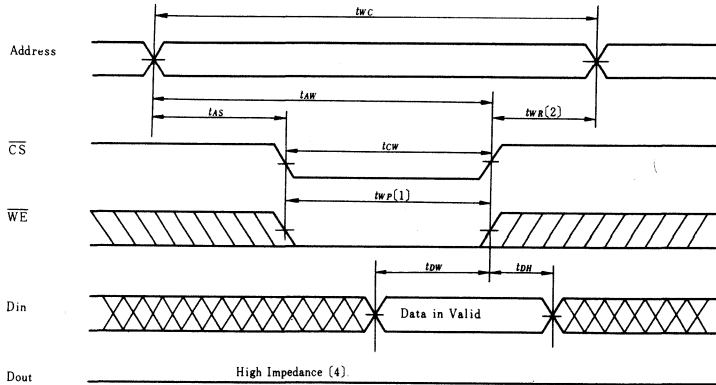
Parameter	Symbol	HM6288P-35		HM6288P-45		HM6288P-55		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	35	—	45	—	55	—	ns
Chip Selection to End of Write	t_{CW}	30	—	40	—	50	—	ns
Address Valid to End of Write	t_{AW}	30	—	40	—	50	—	ns
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	30	—	35	—	45	—	ns
Write Recovery Time	t_{WR}	TBD	—	TBD	—	TBD	—	ns
Data Valid to End of Write	t_{DW}	20	—	20	—	25	—	ns
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns
Write Enabled to Output in High Z	t_{WZ}^*	0	10	0	15	0	20	ns
Output Active from End of Write	t_{OW}^*	0	—	0	—	0	—	ns

* Transition is measured $\pm 200\text{mV}$ from steady state voltage with Load (B).
This parameter is sampled and not 100% tested.

● Timing Waveform of Write Cycle No.1 (WE Controlled)



● Timing Waveform of Write Cycle No.2 (CS Controlled)



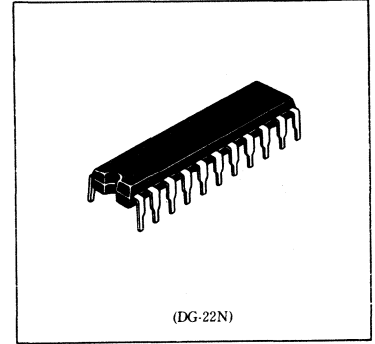
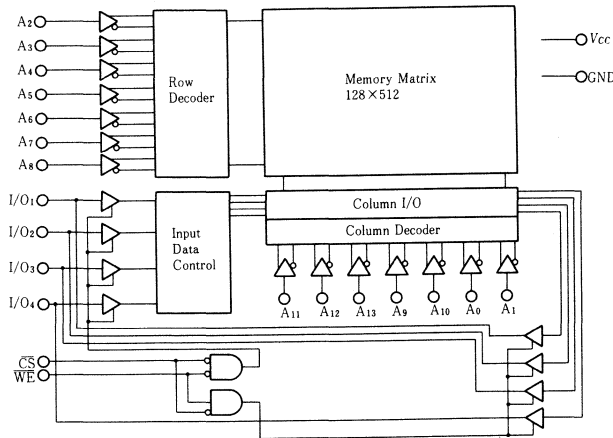
- Notes) 1. A write occurs during the overlap of a low CS and a low WE. (t_{WP})
 2. t_{WR} is measured from the earlier of CS or WE going high to the end of write cycle.
 3. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 4. If the CS low transition occurs simultaneously with the WE low transition or after the WE transition, the output buffers remain in a high impedance state.
 5. If CS is low during this period, I/O pins are in the output state. Then the data input signals of opposite phase to the outputs must not be applied to them.
 6. Dout is the same phase of write data of this write cycle.

16384-word x 4-bit High Speed Static RAM

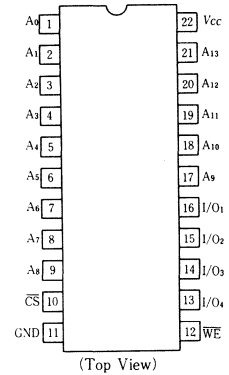
FEATURES

- Super Fast Access Time : 30ns (max.)
- Low power Operation
Operating: 230mW (typ), Standby: 10mW (typ)
- +5V Single Supply
- Completely Static Memory –
No Clock or Timing Strobe required
- Balanced Read and Write Cycle Time
- Fully TTL compatible Input and Output
- Skinny 22 Pin cerdip (300 mil)

BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage to GND pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature (with bias)	$T_{stg}(bias)$	-10 to +85	°C
Storage Temperature	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	6.0	V
Input High Voltage	V_{IH}	2.2	—	6.0	V
Input Low Voltage	V_{IL}	-0.3	—	0.8	V

■ TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	V_{CC} Current	Output Pin	Ref. Cycle
H	×	Not selected	I_{SB}, I_{SB1}	High Z	—
L	H	Output Disabled	I_{CC}, I_{CC1}	High Z	—
L	H	Read	I_{CC}, I_{CC1}	Dout	Read Cycle (1) (2)
L	L	Write	I_{CC}, I_{CC1}	Din	Write Cycle (1) (2)

×: H or L

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	$ I_{IL} $	$V_{CC} = 5.5\text{V}$, $V_{IN} = 0\text{V}$ to V_{CC}	—	—	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IH}$, $V_{I/O} = \text{GND}$ to V_{CC}	—	—	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}} = V_{IL}$, $I_{I/O} = 0\text{mA}$	—	46	80	mA
Average Operating Current	I_{CC1}	Min. Cycle, Duty: 100%	—	69	120	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}} = V_{IH}$, $I_{I/O} = 0\text{mA}$	—	11	30	mA
	I_{SB1}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$, $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	—	2	10	mA
Output Low Voltage	V_{OL}	$I_{OL} = 8\text{mA}$	—	—	0.5	V
Output High Voltage	V_{OH}	$I_{OH} = -4\text{mA}$	2.4	—	—	V

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^{\circ}\text{C}$, unless otherwise noted)

● AC Test Conditions

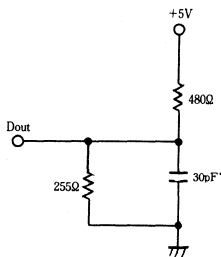
Input pulse levels: GND to 3.0V

Input rise and fall time: 4ns

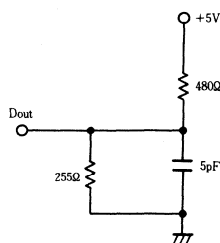
Input and Output reference levels: 1.5V

$\pm 500\text{mV}$ from steady level (Output Load B)

Output Load: See Figure



Output Load A



* Including scope and jig.

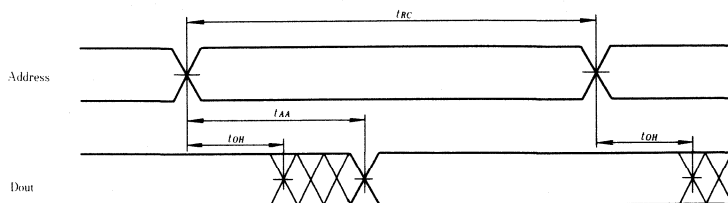
Output Load B
(t_{CHZ} , t_{WHZ} , t_{CLZ} , t_{OW})

● READ CYCLE

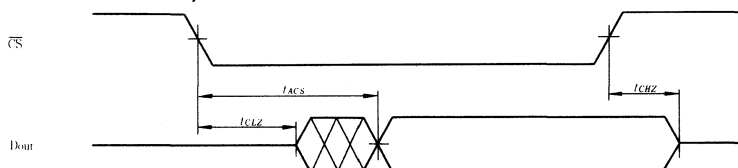
Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	30	—	ns
Address Access Time	t_{AA}	—	30	ns
Chip Select Access Time	t_{ACS}	—	30	ns
Chip Selection to Output in Low Z	t_{CLZ}	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	12	ns
Output Hold from Address Change	t_{OH}	5	—	ns
Chip Selection to Power Up Time	t_{PU}^*	0	—	ns
Chip Deselection to Power Down Time	t_{PD}^*	—	30	ns

* This parameter is sampled and not 100% tested.

● Timing waveform of Read Cycle No. 1^{1),2)}



● Timing waveform of Read Cycle No. 2^{1),3)}

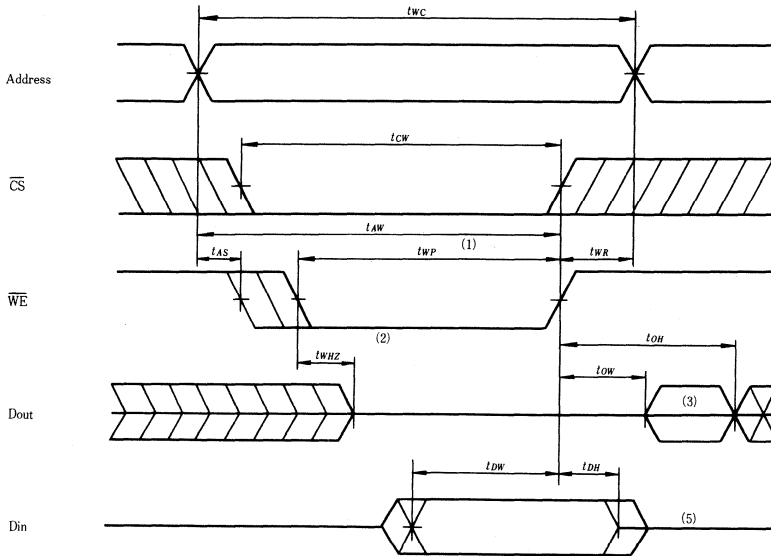


- Note) 1. $\overline{WE} = V_{IH}$
 2. $\overline{CS} = V_{IL}$
 3. Address valid prior to or coincident with \overline{CS} transition Low.

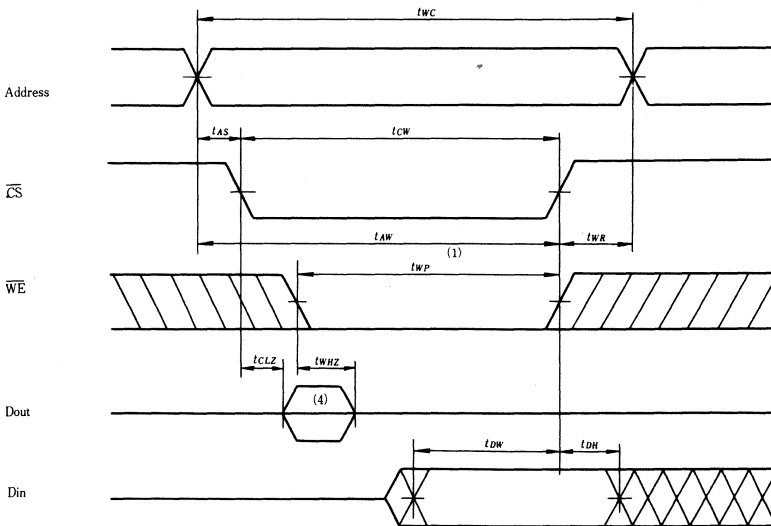
● WRITE CYCLE

Item	Symbol	min	max	Unit
Write Cycle Time	t_{WC}	30	—	ns
Chip Selection to End of Write	t_{CW}	25	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Valid to End of Write	t_{AW}	25	—	ns
Write Pulse Width	t_{WP}	25	—	ns
Write Recovery Time	t_{WR}	0	—	ns
Write to Output in High Z	t_{WHZ}	0	12	ns
Data Valid to End of Write	t_{DW}	15	—	ns
Data Hold Time	t_{DH}	5	—	ns
Output Active from End of Write	t_{OW}	0	—	ns

● Timing waveform of Write Cycle No. 1 (\overline{WE} Controlled)



● Timing waveform of Write Cycle No. 2 (\overline{CS} Controlled)



- Notes:
1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. During this period, I/O pins are in the output state so that the input signals of opposite phase to the outputs must not be applied.
 3. Dout is the same phase of write data of this write cycle.
 4. If the \overline{CS} low transition occurs after the \overline{WE} low transition, output remain in a high impedance state.
 5. If \overline{CS} is low during this period, I/O pins are in the output state. Then, the data input signals of opposite phase to the outputs must not be applied to them.

■ CAPACITANCE ($T_a=25^{\circ}\text{C}$, $f=1.0\text{MHz}$)

Item	Symbol	min	typ	max	Conditions
Input Capacitance	C_{IN}	—	—	6.0	$V_{IN}=0\text{V}$
Input/Output Capacitance	$C_{I/O}$	—	—	8.0	$V_{OUT}=0\text{V}$

Note) This parameter is sampled and not 100% tested.

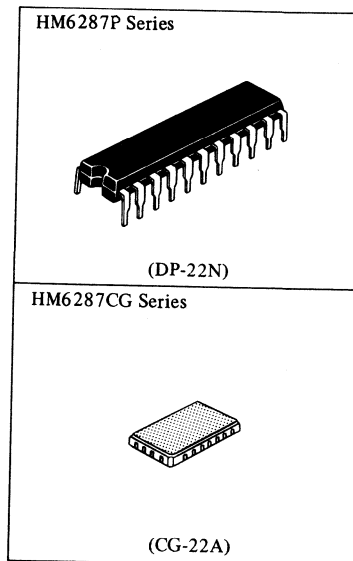
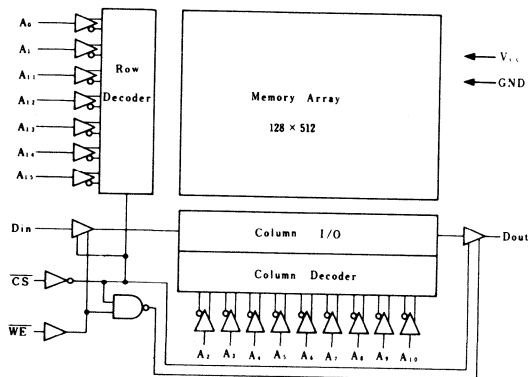
HM6287P Series, HM6287CG Series

65536-word × 1-bit High Speed Static CMOS RAM

■ FEATURES

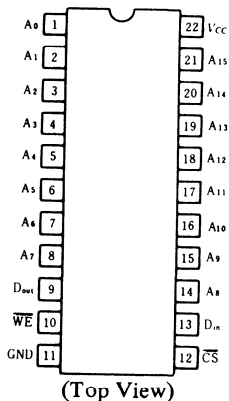
- High Speed: Fast Access Time 45/55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
Standby: 100μW (typ.), Operation: 300mW (typ.)
- Completely Static Memory
No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output

■ BLOCK DIAGRAM

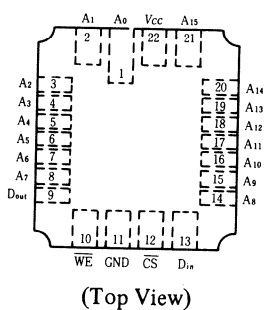


■ PIN ARRANGEMENT

● HM6287P Series



● HM6287CG Series



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	Plastic	-55 to +125	°C
	Ceramic	-65 to +150	
Temperature Under Bias	T_{bias}	-10 to +85	°C

* V_T min = -3.5V (Pulse width 20ns)

■ TRUTH TABLE

\overline{CS}	\overline{WE}	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	-
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

*Pulse width 20ns, DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, GND = 0V, $T_a = 0$ to +70°C)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = \text{Max.}, V_{in} = \text{GND to } V_{CC}$	-	-	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS} = V_{IH}, V_{out} = \text{GND to } V_{CC}$	-	-	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{CS} = V_{IL}, I_{out} = 0\text{mA}$	-	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{CS} = V_{IH}$	-	10	30	mA
	I_{SB1}	$\overline{CS} = V_{CC} - 0.2\text{V}, V_{IN} \leq 0.2\text{V or } \geq V_{CC} - 0.2\text{V}$	-	0.02	2.0	mA
Output Voltage	V_{OL}	$I_{OL} = 8\text{mA}$	-	-	0.4	V
	V_{OH}	$I_{OH} = -4.0\text{mA}$	2.4	-	-	V

* Typical limits are at $V_{CC} = 5.0\text{V}, T_a = 25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($f = 1\text{MHz}, T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	-	5	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	-	-	7.5	pF

Note) This parameter is sampled and not 100% tested.

■ **AC CHARACTERISTICS** ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$, unless otherwise noted)

● **AC TEST CONDITIONS**

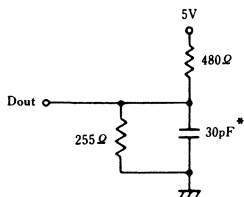
Input Pulse Levels: GND to 3.0V

Input Rise and Fall Times: 5ns

Input and Output Timing Reference Levels: 1.5V

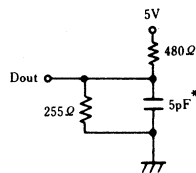
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

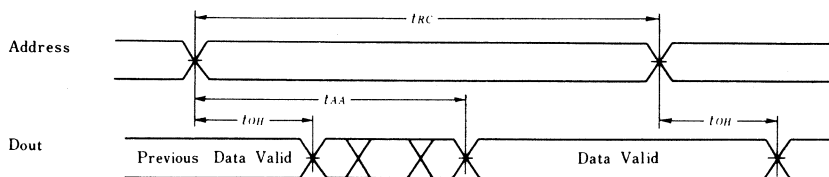


*Including scope & jig capacitance

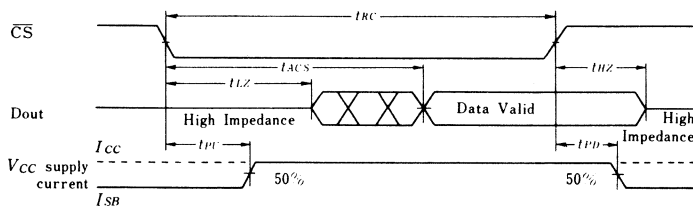
■ **READ CYCLE**

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	—	55	—	70	—	ns	1
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	
Chip Select Access Time	t_{ACS}	—	45	—	55	—	70	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	7
Chip Deselection to Power Down Time	t_{PD}	—	40	—	40	—	40	ns	7

● **Timing Waveform of Read Cycle No. 1** ⁽⁴⁾⁽⁵⁾



● **Timing Waveform of Read Cycle No. 2** ⁽⁴⁾⁽⁶⁾

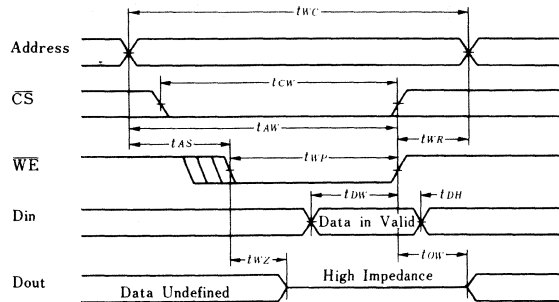


- Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured ± 500 mV from steady state voltage with specified loading in Load B.
 4. WE is high for READ Cycle.
 5. Device is continuously selected, while $\overline{CS} = V_{IL}$.
 6. Address valid prior to or coincident with \overline{CS} transition low.
 7. This parameter is sampled and not 100% tested.

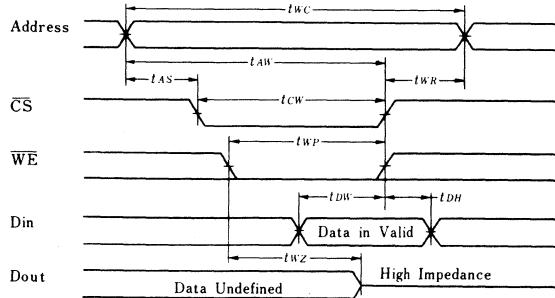
● WRITE CYCLE

Item	Symbol	HM6287-45		HM6287-55		HM6287-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	—	55	—	70	—	ns	
Chip Selection to End of Write	t_{CW}	40	—	50	—	55	—	ns	
Address Valid to End of Write	t_{AW}	40	—	50	—	55	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	25	—	35	—	40	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	25	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	3, 4

● Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled)

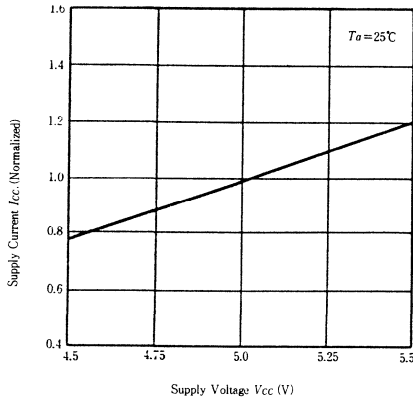


● Timing Waveform of Write Cycle No. 1 (\overline{CS} Controlled)

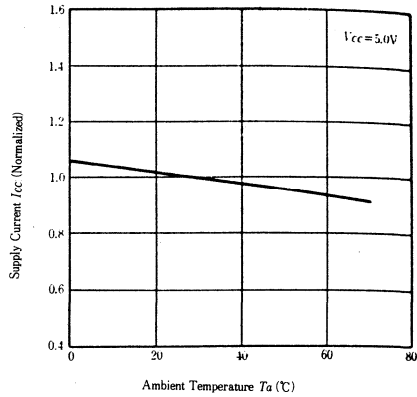


- Notes)
1. If \overline{CS} goes high Simultaneously with \overline{WE} high, the output remains in a high impedance state.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

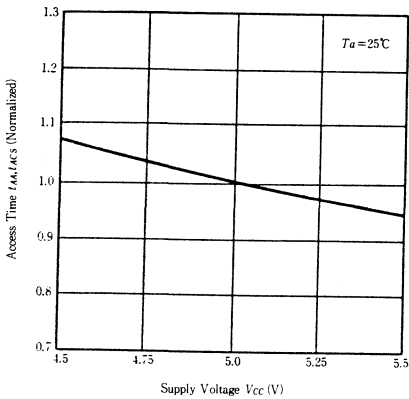
SUPPLY CURRENT vs. SUPPLY VOLTAGE



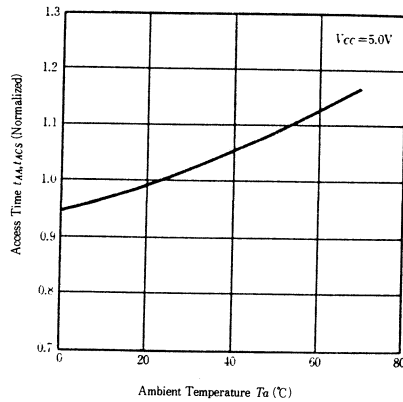
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



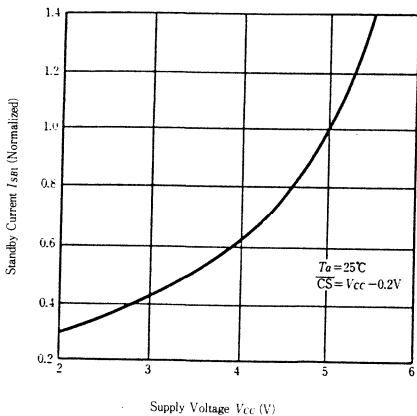
ACCESS TIME vs. SUPPLY VOLTAGE



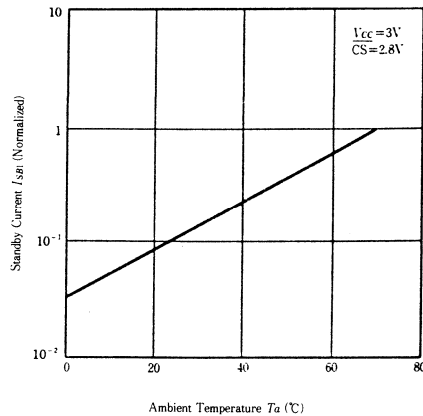
ACCESS TIME vs. AMBIENT TEMPERATURE



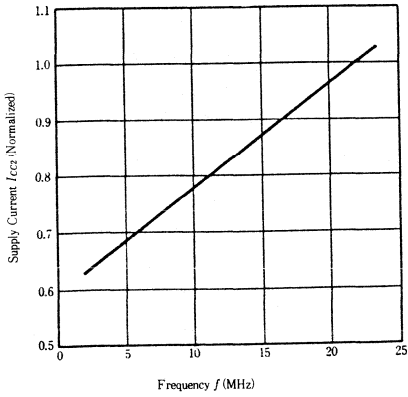
STANDBY CURRENT vs. SUPPLY VOLTAGE



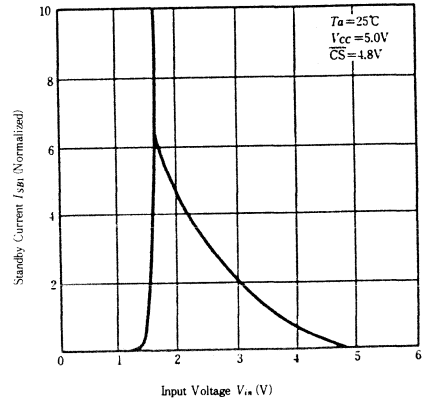
STANDBY CURRENT vs. AMBIENT TEMPERATURE



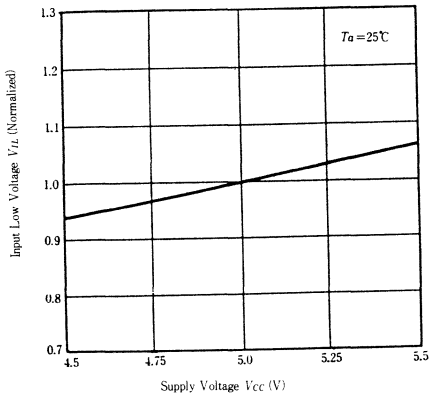
SUPPLY CURRENT vs. FREQUENCY



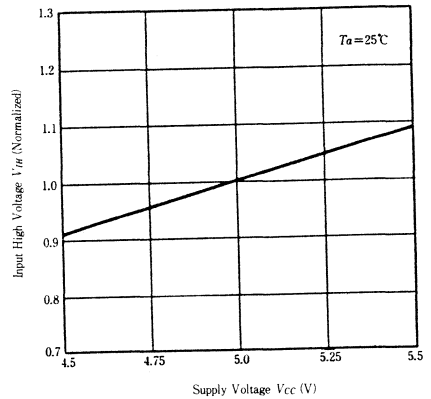
STANDBY CURRENT vs. INPUT VOLTAGE



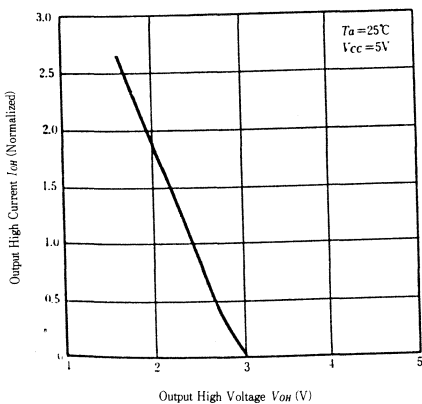
INPUT LOW VOLTAGE vs. SUPPLY VOLTAGE



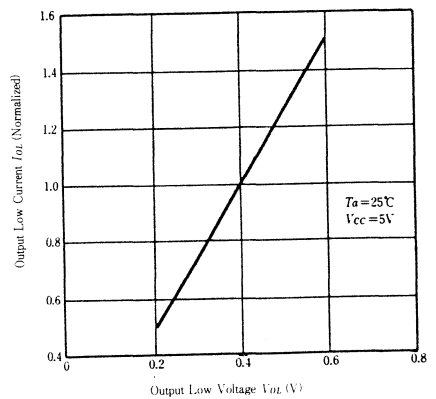
INPUT HIGH VOLTAGE vs. SUPPLY VOLTAGE



OUTPUT HIGH CURRENT vs. OUTPUT HIGH VOLTAGE



OUTPUT LOW CURRENT vs. OUTPUT LOW VOLTAGE



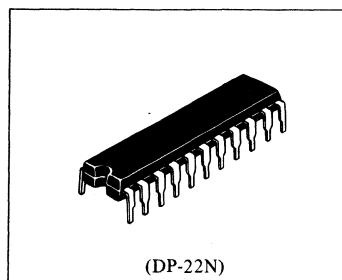
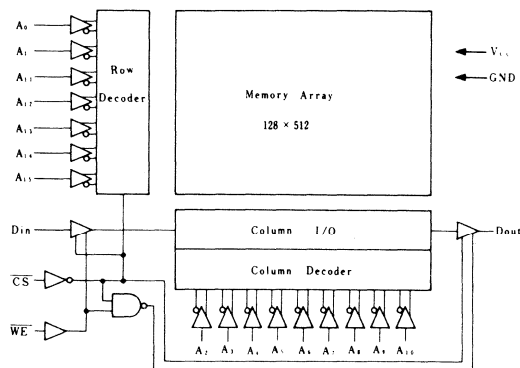
HM6287LP Series

65536-word × 1-bit High Speed Static CMOS RAM

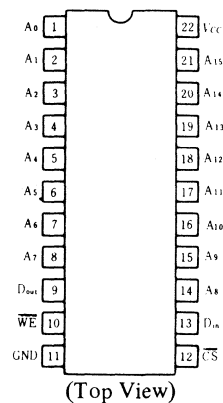
■ FEATURES

- High Speed: Fast Access Time 55/70ns (max.)
- Single 5V Supply and High Density 22 Pin Package
- Low Power Standby and Low Power Operation
Standby: 10 μ W (typ.), Operation: 300 mW (typ.)
- Completely Static Memory
No Clock or Timing Strobe Required
- Equal Access and Cycle Times
- Directly TTL Compatible: All Inputs and Output

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND*	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature	T_{stg}	-55 to +125	$^{\circ}$ C
Temperature Under Bias	T_{bias}	-10 to +85	$^{\circ}$ C

* V_T min = -3.5V (Pulse width 20ns)

■ TRUTH TABLE

CS	WE	Mode	V_{CC} Current	Dout Pin	Ref. Cycle
H	X	Not Selected	I_{SB}, I_{SB1}	High Z	–
L	H	Read	I_{CC}	Dout	Read Cycle
L	L	Write	I_{CC}	High Z	Write Cycle

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-3.0*	–	0.8	V

*Pulse width 20ns, DC: -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $\text{GND} = 0\text{V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = \text{Max.}, V_{in} = \text{GND to } V_{CC}$	–	–	2.0	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IH}, V_{out} = \text{GND to } V_{CC}$	–	–	2.0	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}} = V_{IL}, I_{out} = 0\text{mA}$	–	60	100	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}} = V_{IH}$	–	10	30	mA
	I_{SB1}	$\overline{\text{CS}} = V_{CC} - 0.2\text{V}, V_{IN} \leq 0.2\text{V or } \geq V_{CC} - 0.2\text{V}$	–	2	100	μA
Output Voltage	V_{OL}	$I_{OL} = 8\text{mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -4.0\text{mA}$	2.4	–	–	V

* Typical limits are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($f = 1\text{MHz}$, $T_a = 25^\circ\text{C}$)

Item	Symbol	Test Conditions	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	–	5	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	–	–	7.5	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0$ to $+70^\circ\text{C}$, unless otherwise noted)

● AC TEST CONDITIONS

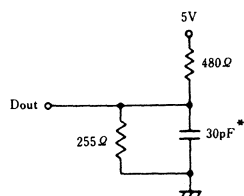
Input Pulse Levels: GND to 3.0V

Input Rise and Fall Times: 5ns

Input and Output Timing Reference Levels: 1.5V

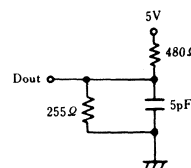
Output Load: See Figure

Output Load A



*Including scope & jig capacitance

Output Load B

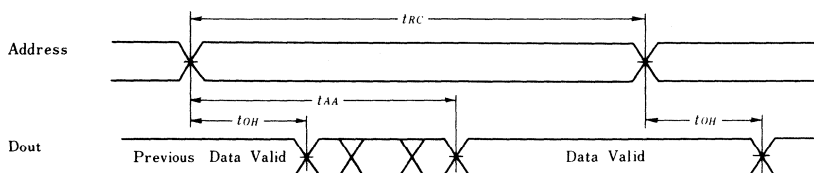


*Including scope & jig capacitance

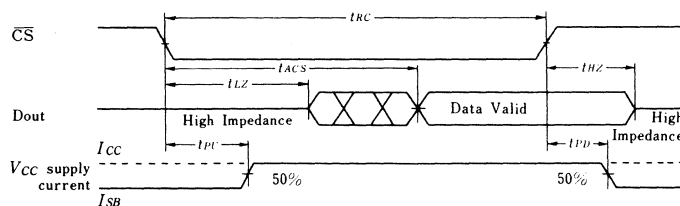
■ READ CYCLE

Item	Symbol	HM6287LP-45		HM6287LP-55		HM6287LP-70		Unit	Notes
		min	max	min	max	min	max		
Read Cycle Time	t_{RC}	45	—	55	—	70	—	ns	1
Address Access Time	t_{AA}	—	45	—	55	—	70	ns	
Chip Select Access Time	t_{ACS}	—	45	—	55	—	70	ns	
Output Hold from Address Change	t_{OH}	5	—	5	—	5	—	ns	
Chip Selection to Output in Low Z	t_{LZ}	5	—	5	—	5	—	ns	2, 3, 7
Chip Deselection to Output in High Z	t_{HZ}	0	30	0	30	0	30	ns	2, 3, 7
Chip Selection to Power Up Time	t_{PU}	0	—	0	—	0	—	ns	7
Chip Deselection to Power Down Time	t_{PD}	—	40	—	40	—	40	ns	7

● Timing Waveform of Read Cycle No. 1⁽⁴⁾⁽⁵⁾



● Timing Waveform of Read Cycle No. 2⁽⁴⁾⁽⁶⁾

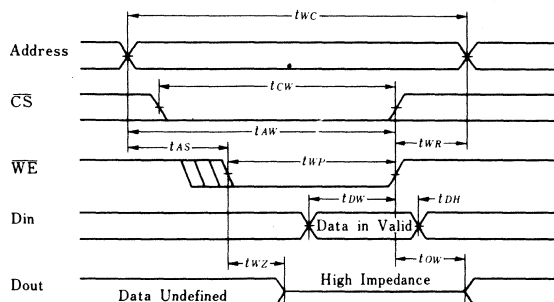


- Notes:
1. All Read Cycle timings are referenced from last valid address to the first transitioning address.
 2. At any given temperature and voltage condition, t_{HZ} max. is less than t_{LZ} min. both for a given device and from device to device.
 3. Transition is measured ± 50 mV from steady state voltage with specified loading in Load B.
 4. \overline{WE} is high for READ Cycle.
 5. Device is continuously selected, while $\overline{CS} = V_{IL}$.
 6. Address valid prior to or coincident with CS transition low.
 7. This parameter is sampled and not 100% tested.

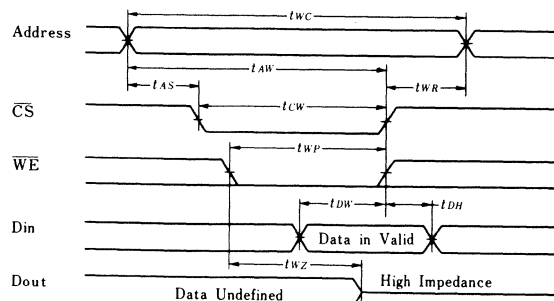
● WRITE CYCLE

Item	Symbol	HM6287LP-45		HM6287LP-55		HM6287LP-70		Unit	Notes
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	45	—	55	—	70	—	ns	2
Chip Selection to End of Write	t_{CW}	40	—	50	—	55	—	ns	
Address Valid to End of Write	t_{AW}	40	—	50	—	55	—	ns	
Address Setup Time	t_{AS}	0	—	0	—	0	—	ns	
Write Pulse Width	t_{WP}	25	—	35	—	40	—	ns	
Write Recovery Time	t_{WR}	0	—	0	—	0	—	ns	
Data Valid to End of Write	t_{DW}	25	—	25	—	30	—	ns	
Data Hold Time	t_{DH}	0	—	0	—	0	—	ns	
Write Enabled to Output in High Z	t_{WZ}	0	25	0	25	0	30	ns	3, 4
Output Active from End of Write	t_{OW}	0	—	0	—	0	—	ns	3, 4

● Timing Waveform of Write Cycle No. 1 (\overline{WE} Controlled)



● Timing Waveform of Write Cycle No. 1 (\overline{CS} Controlled)



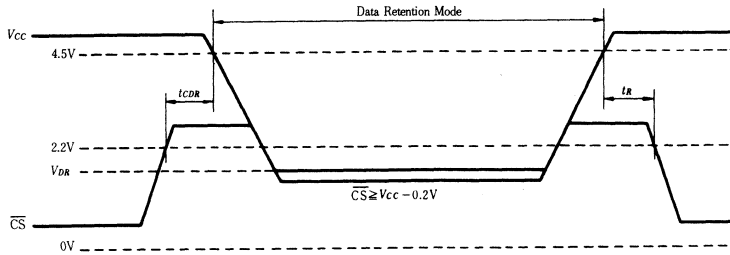
- Notes)
1. If \overline{CS} goes high Simultaneously with \overline{WE} high, the output remains in a high impedance state.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$,	2.0	—	—	V
Data Retention Current	I_{CCDR}	$V_{in} \geq V_{CC} - 0.2\text{V}$ or	—	1	50**	μA
Chip Deselect to Data Retention Time	t_{CDR}	$0\text{V} \leq V_{in} \leq 0.2\text{V}$	0	—	—	ns
Operation Recovery Time	t_R		t_{RC}^*	—	—	ns

* t_{RC} = Read Cycle Time ** $V_{CC} = 3.0\text{V}$

● LOW V_{CC} DATA RETENTION WAVEFORM



HM6787 Series, HM6787CG Series

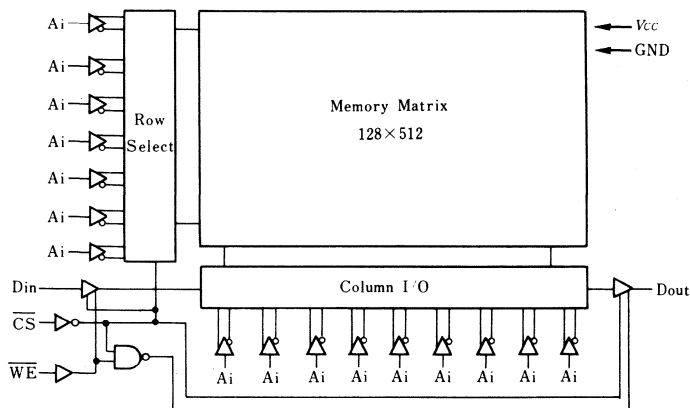
Preliminary

65536-word × 1-bit High Speed Static RAM

■ FEATURES

- Super Fast Access Time: 25ns/30ns (max.)
- Low Power Dissipation (DC):
Operating 180mW (typ)
- High Driving Capability: I_{OL} 16mA
- +5V Single Supply
- Completely Static Memory
No Clock or Timing Strobe Required
- Balanced Read and Write Cycle Time
- Fully TTL Compatible Input and Output
- Skinny 22-pin Cerdip (300 mil) and 22-pin Chip Carrier

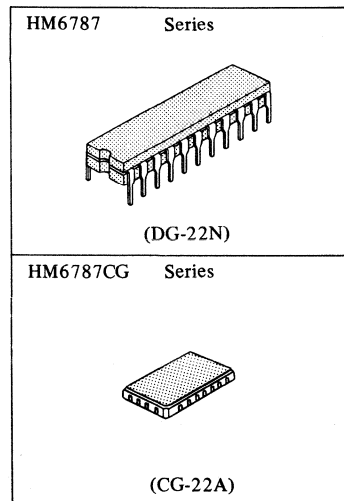
■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

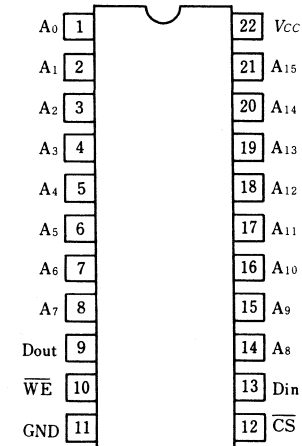
Item	Symbol	Rating	Unit
Terminal Voltage to GND Pin	V_T	-0.5 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sale Dept. regarding specifications.



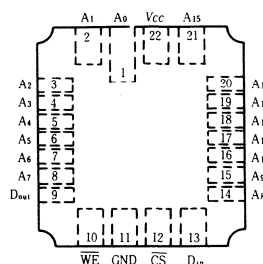
■ PIN ARRANGEMENT

● HM6787 Series



(Top View)

● HM6787CG Series



(Top View)

■ RECOMMENDED DC OPERATING CONDITIONS ($0^{\circ}\text{C} \leq T_a \leq 70^{\circ}\text{C}$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High Voltage	V_{IH}	2.2	-	6.0	V
Input Low Voltage	V_{IL}	-0.3	-	0.8	V

■ TRUTH TABLE

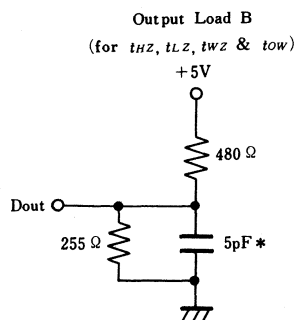
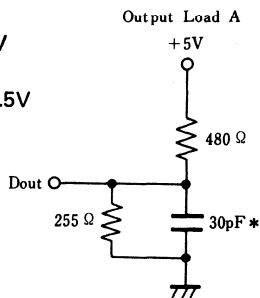
$\overline{\text{CS}}$	$\overline{\text{WE}}$	Mode	V_{CC} Current	Output Pin
H	X	Not Selected	I_{SB}, I_{SB1}	High Z
L	H	Read	I_{CC}	Dout
L	L	Write	I_{CC}	High Z

■ DC AND OPERATING CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	$ I_{LI} $	$V_{CC} = 5.5\text{V}, V_{IN} = 0\text{V}$ to V_{CC}	-	-	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{\text{CS}} = V_{IH}, V_{OUT} = 0\text{V}$ to V_{CC}	-	-	2	μA
Operating Power Supply Current	I_{CC}	$\overline{\text{CS}} = V_{IL}, I_{I/O} = 0\text{mA}$	-	-	100	mA
Standby Power Supply Current	I_{SB}	$\overline{\text{CS}} = V_{IH}, I_{I/O} = 0\text{mA}$	-	-	40	mA
	I_{SB1}	$\overline{\text{CS}} \geq V_{CC} - 0.2\text{V}$ $V_{IN} \leq 0.2\text{V}$ or $V_{IN} \geq V_{CC} - 0.2\text{V}$	-	-	20	mA
Output Low Voltage	V_{OL}	$I_{OL} = 16\text{mA}$	-	-	0.5	V
Output High Voltage	V_{OH}	$I_{OH} = -4\text{mA}$	2.4	-	-	V

■ AC TEST CONDITIONS

- Input pulse levels: GND to 3.0V
- Input rise and fall times: 4ns
- Input timing reference levels: 1.5V
- Output reference levels: 1.5V
- Output load: See Figure



* Including scope and jig.

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1.0\text{MHz}$)

Item	Symbol	typ.	Unit	Conditions
Input Capacitance	C_{IN}	2.0	pF	$V_{IN} = 0\text{V}$
Output Capacitance	C_{OUT}	3.0	pF	$V_{OUT} = 0\text{V}$

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 0^\circ\text{C}$ to 70°C , unless otherwise noted.)

● READ CYCLE

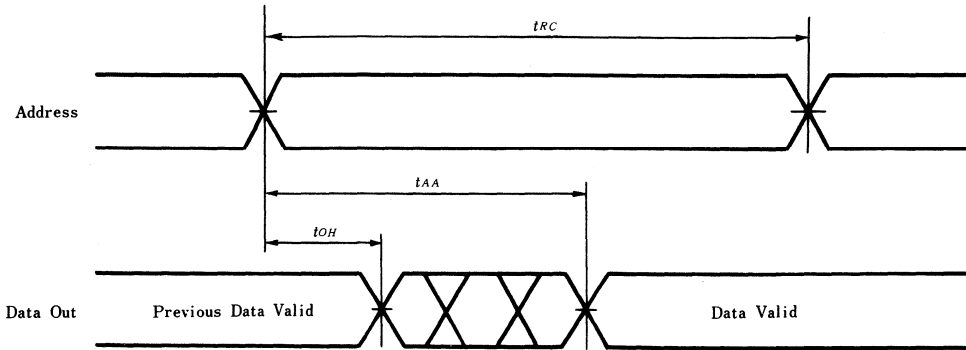
Item	Symbol	HM6787/CG		HM6787/CG-30		Unit
		min.	max.	min.	max.	
Read Cycle Time	t_{RC}	25	–	30	–	ns
Address Access Time	t_{AA}	–	25	–	30	ns
Chip Select Access Time	t_{ACS}	–	25	–	30	ns
Output Hold from Address Change	t_{OH}	5	–	5	–	ns
Chip Selection to Output in Low Z	t_{LZ}	5	–	5	–	ns
Chip Deselection to Output in High Z	t_{HZ}	0	15	0	15	ns
Chip Selection to Power Up Time	t_{PU}	0	–	0	–	ns
Chip Deselection to Power Down Time	t_{PD}	–	25	–	30	ns

● WRITE CYCLE

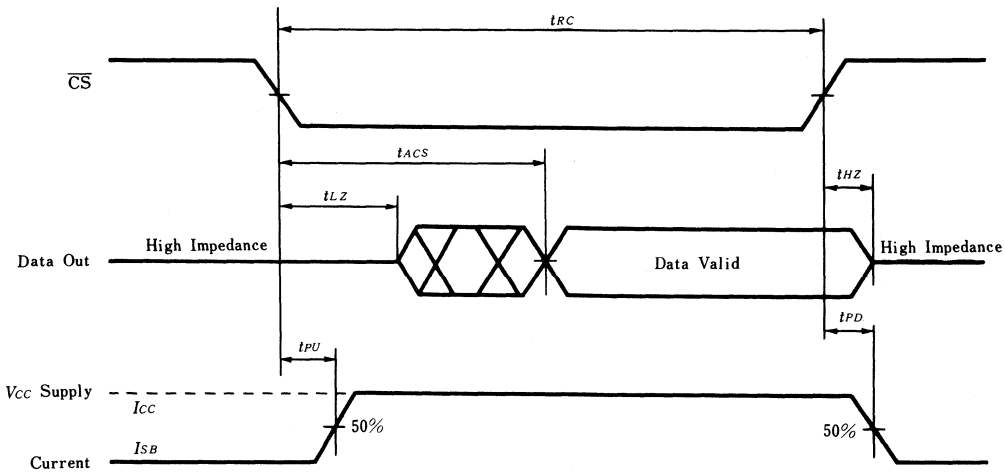
Item	Symbol	HM6787/CG		HM6787/CG-30		Unit	Notes
		min.	max.	min.	max.		
Write Cycle Time	t_{WC}	25	–	30	–	ns	2
Chip Selection to End of Write	t_{CW}	20	–	25	–	ns	
Address Valid to End of Write	t_{AW}	20	–	25	–	ns	
Address Setup Time	t_{AS}	0	–	0	–	ns	
Write Pulse Width	t_{WP}	20	–	25	–	ns	
Write Recovery Time	t_{WR}	5	–	5	–	ns	
Data Valid to End of Write	t_{DW}	20	–	25	–	ns	
Data Hold Time	t_{DH}	0	–	0	–	ns	
Write Enable to Output in High Z	t_{WZ}	0	15	0	15	ns	3, 4
Output Active from End of Write	t_{OW}	0	–	0	–	ns	3, 4

- Note: 1. If $\overline{\text{CS}}$ goes high simultaneously with $\overline{\text{WE}}$ high, the output remains in a high impedance state.
 2. All Write Cycle timings are referenced from the last valid address to the first transitioning address.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.
 4. This parameter is sampled and not 100% tested.

● TIMING WAVEFORM OF READ CYCLE NO. 1^{1), 2)}

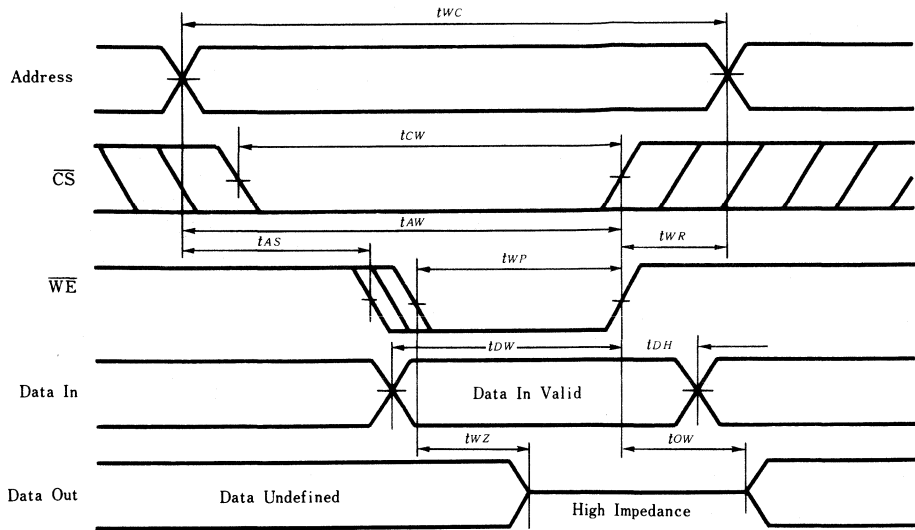


● TIMING WAVEFORM OF READ CYCLE NO. 2^{1), 3)}



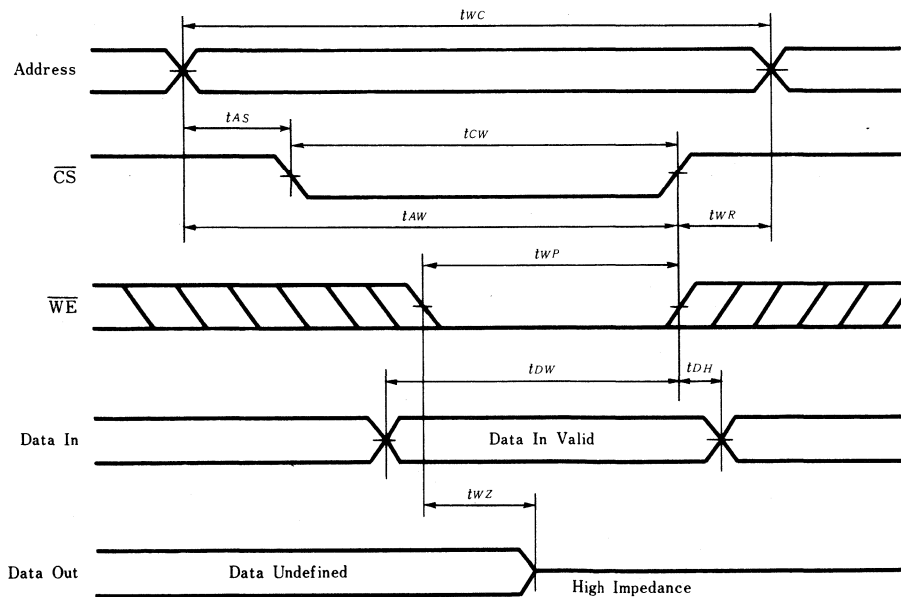
- Note: 1. \overline{WE} is high and \overline{CS} is low for READ cycle.
 2. Addresses valid prior to or coincident with \overline{CS} transition low.
 3. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO. 1 (\overline{WE} CONTROLLED)



Note: 1. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

● TIMING WAVEFORM OF WRITE CYCLE NO. 2 (\overline{CS} CONTROLLED)



Note: 1. Transition is measured $\pm 500\text{mV}$ from steady state voltage with specified loading in Load B.

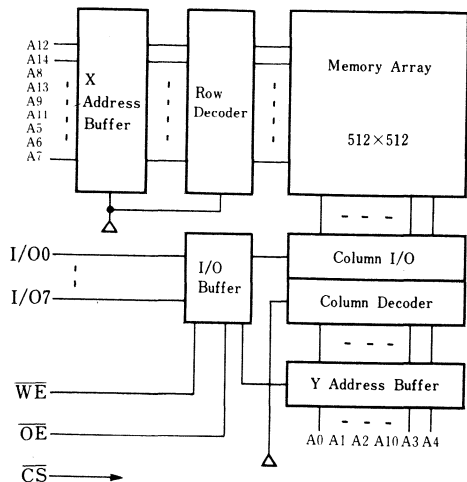
HM62256P Series, HM62256FP Series

32768-word × 8-bit High Speed Static CMOS RAM

■ FEATURES

- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation; Standby: 200 μ W (typ.), Operation: 40mW (typ.) ($f=1$ MHz)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Standard 28 pin Package Configuration

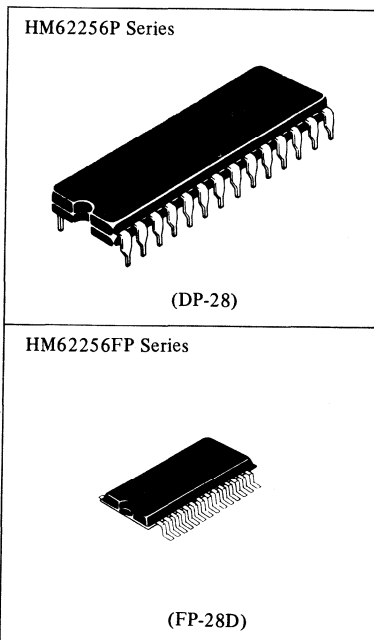
■ BLOCK DIAGRAM



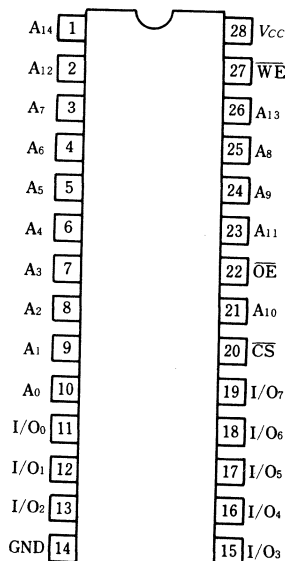
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to GND	V_T	-0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

*Pulse Width 50ns: -3.0V



■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	—
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	—	6.0	V
	V_{IL}	-3.0*	—	0.8	V

*Pulse Width: 50ns, DC: V_{IL} min = -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, GND=0V, $T_a=0$ to $+70^\circ\text{C}$)

Item	Item Symbol	Symbol	Test Condition	min.	typ.*	max.	Unit
Input Leakage Current		I_{LI}	$V_{IN}=\text{GND to } V_{CC}$	—	—	2	μA
Output Leakage Current		I_{LO}	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}=\text{GND to } V_{CC}$	—	—	2	μA
Operating Power Supply Current		I_{CC}	$\overline{CS}=V_{IL}, I_{I/O}=0\text{mA}$	—	8	15	mA
Average Operating Power Supply Current	HM62256P/FP-8	I_{CC1}	Min. Cycle, duty=100%, $I_{I/O}=0\text{mA}$	—	50	70	mA
	HM62256P/FP-10			—	40	70	
	HM62256P/FP-12			—	35	70	
	HM62256P/FP-15			—	33	70	
		I_{CC2}	$\overline{CS}=V_{IL}, V_{IH}=V_{CC}, V_{IL}=0\text{V}, I_{I/O}=0\text{mA}, f=1\text{MHz}$	—	8	15	mA
Standby Power Supply Current		I_{SB}	$\overline{CS}=V_{IH}$	—	0.5	3	mA
		I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	—	0.04	2	mA
Output Voltage		V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.4	V
		V_{OH}	$I_{OH} = -1.0\text{mA}$	2.4	—	—	V

Notes) *: Typical values are at $V_{CC} = 5.0\text{V}$, $T_a = 25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}, f=1\text{MHz}$)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	—	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	—	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC}=5V\pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$ unless otherwise noted)

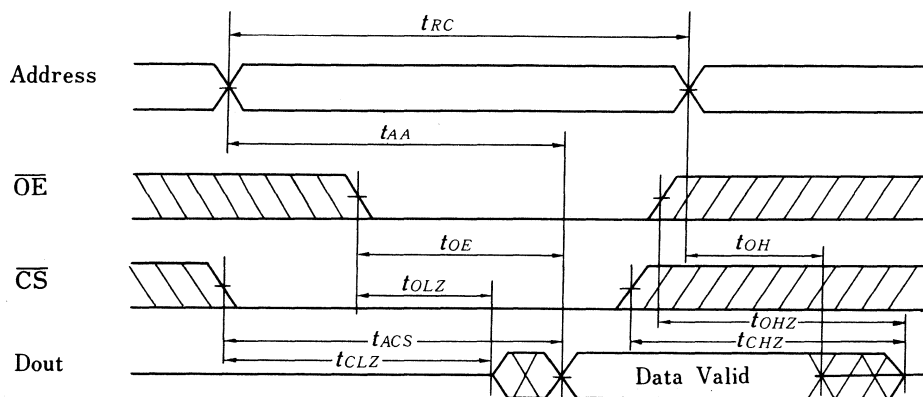
● AC Test Conditions

- Input pulse levels: 0.8V to 2.4V
- Input and Output timing reference levels: 1.5V
- Input rise and fall times: 5ns
- Output load: 1TTL Gate and $C_L = 100\text{pF}$
(Including scope and jig)

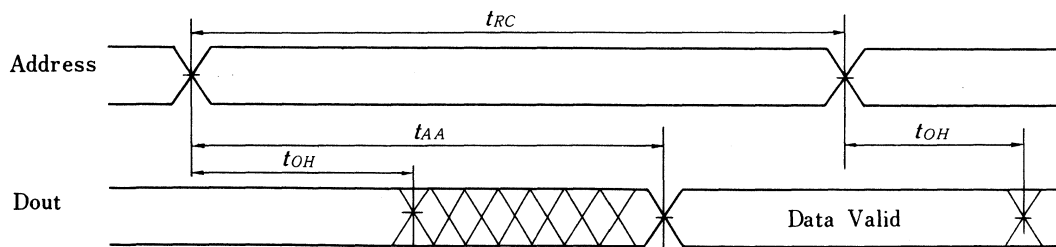
● Read Cycle

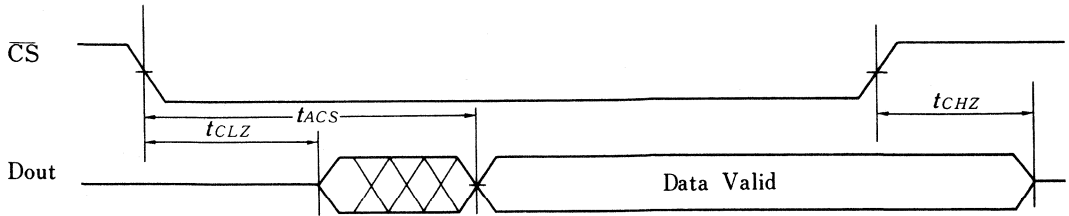
Item	Symbol	HM62256P/FP8		HM62256P/FP-10		HM62256P/FP-12		HM62256P/FP-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	—	100	—	120	—	150	—	ns
Address Access Time	t_{AA}	—	85	—	100	—	120	—	150	ns
Chip Select Access Time	t_{ACS}	—	85	—	100	—	120	—	150	ns
Output Enable to Output Valid	t_{OE}	—	45	—	50	—	60	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	10	—	10	—	10	—	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

● Timing Waveform of Read Cycle No. 1^[1]



● Timing Waveform of Read Cycle No. 2^{[1][2][4]}



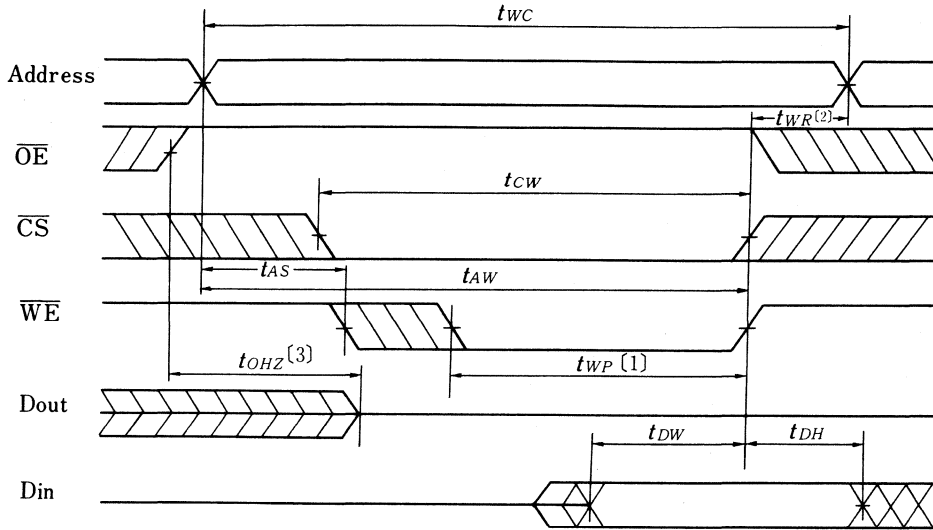
● Timing Waveform of Read Cycle No. 3^{[1][3][4]}


- Notes) 1. \overline{WE} is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $OE = V_{IL}$.

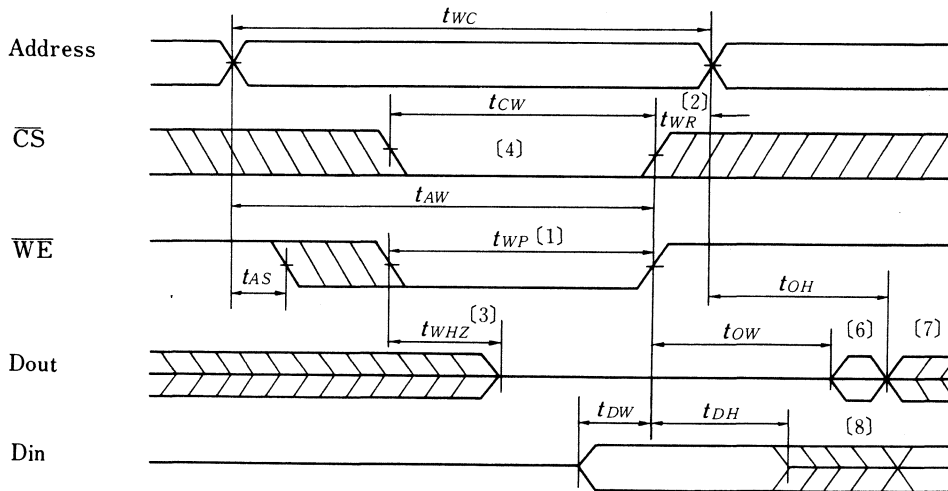
● Write Cycle

Item	Symbol	HM62256P-8		HM62256P-10		HM62256P-12		HM62256P-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	—	100	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	75	—	90	—	100	—	120	—	ns
Address Valid to End of Write	t_{AW}	75	—	90	—	100	—	120	—	ns
Address Set Up Time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	70	—	75	—	90	—	110	—	ns
Write Recovery Time	t_{WR}	10	—	0	—	0	—	0	—	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	40	—	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	5	—	ns

● Timing Waveform of Write Cycle No. 1 (\overline{OE} Clock)



● Timing Waveform of Write Cycle No. 2^[5] (\overline{OE} Low Fixed)



- Notes: 1. A write occurs during the overlap (t_{WP}) of a low \overline{CS} and a low \overline{WE} .
 2. t_{WR} is measured from the earlier of \overline{CS} or \overline{WE} going high to the end of write cycle.
 3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied.
 4. If the \overline{CS} low transition occurs simultaneously with the \overline{WE} low transition or after the \overline{WE} low transition, outputs remain in a high impedance state.
 5. \overline{OE} is continuously low. ($\overline{OE} = V_{IL}$)
 6. Dout is in the same phase of written data of this write cycle.
 7. Dout is the read data of next address.
 8. If \overline{CS} is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

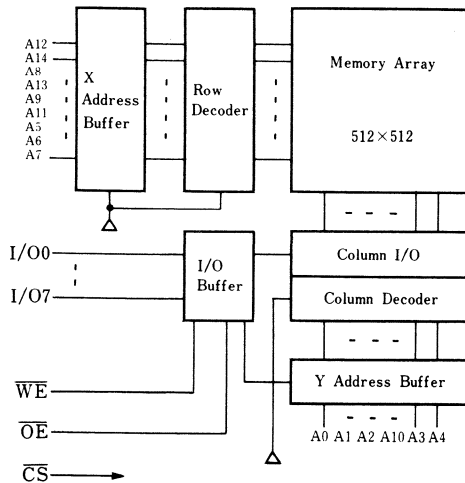
HM62256LP Series, HM62256LFP Series

32768-word X 8-bit High Speed Static CMOS RAM

■ FEATURES

- High Speed: Fast Access Time 85/100/120/150ns (max.)
- Low Power Standby and Low Power Operation;
Standby: 10μW (typ.), Operation: 40mW (typ.) ($f = 1\text{MHz}$)
- Single 5V Supply
- Completely Static RAM: No clock or Timing Strobe Required
- Equal Access and Cycle Time
- Common Data Input and Output, Three-state Output
- Directly TTL Compatible: All Input and Output
- Standard 28 pin Package Configuration
- Capability of Battery Back up Operation

■ BLOCK DIAGRAM

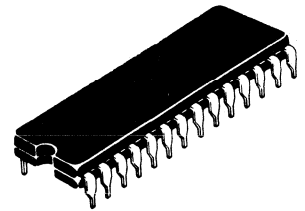


■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin with relative to GND	V_T	-0.5* to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-10 to +85	°C

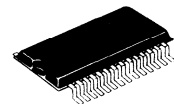
*Pulse Width 50ns: -3.0V

HM62256LP Series



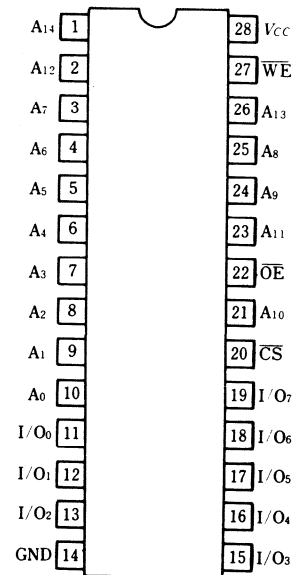
(DP-28)

HM62256LFP Series



(FP-28D)

■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

\overline{CS}	\overline{OE}	\overline{WE}	Mode	V_{CC} Current	I/O Pin	Reference Cycle
H	X	X	Not Selected	I_{SB}, I_{SB1}	High Z	-
L	L	H	Read	I_{CC}	Dout	Read Cycle No. 1~3
L	H	L	Write	I_{CC}	Din	Write Cycle No. 1
L	L	L	Write	I_{CC}	Din	Write Cycle No. 2

X means H or L

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input Voltage	V_{IH}	2.2	-	6.0	V
	V_{IL}	-3.0*	-	0.8	V

*Pulse Width: 50ns. DC: V_{IL} min = -0.5V

■ DC AND OPERATING CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, GND=0V, $T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Condition	min.	typ.*	max.	Unit
Input Leakage Current	$ I_{LI} $	$V_{IN}=\text{GND to } V_{CC}$	-	-	2	μA
Output Leakage Current	$ I_{LO} $	$\overline{CS}=V_{IH}$ or $\overline{OE}=V_{IH}$, $V_{I/O}=\text{GND to } V_{CC}$	-	-	2	μA
Operating Power Supply Current	I_{CC}	$\overline{CS}=V_{IL}$, $I_{I/O}=0\text{mA}$	-	8	15	mA
Average Operating Power Supply Current	HM62256LP/LFP-8	I_{CC1} Min. Cycle, duty=100%, $I_{I/O}=0\text{mA}$	-	50	70	mA
	HM62256LP/LFP-10		-	40	70	
	HM62256LP/LFP-12		-	35	70	
	HM62256LP/LFP-15		-	33	70	
Standby Power Supply Current	I_{CC2}	$\overline{CS}=V_{IL}$, $V_{IH}=V_{CC}$, $V_{IL}=0\text{V}$, $I_{I/O}=0\text{mA}$, $f=1\text{MHz}$	-	8	15	mA
	I_{SB}	$\overline{CS}=V_{IH}$	-	0.5	3	mA
Output Voltage	I_{SB1}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	-	2	100	μA
	V_{OL}	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	-	-	V

Notes: *: Typical values are at $V_{CC}=5.0\text{V}$, $T_a=25^\circ\text{C}$ and specified loading.

■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Item	Symbol	Test Condition	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	-	6	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O}=0\text{V}$	-	8	pF

Note) This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0$ to $+70^\circ\text{C}$ unless otherwise noted)

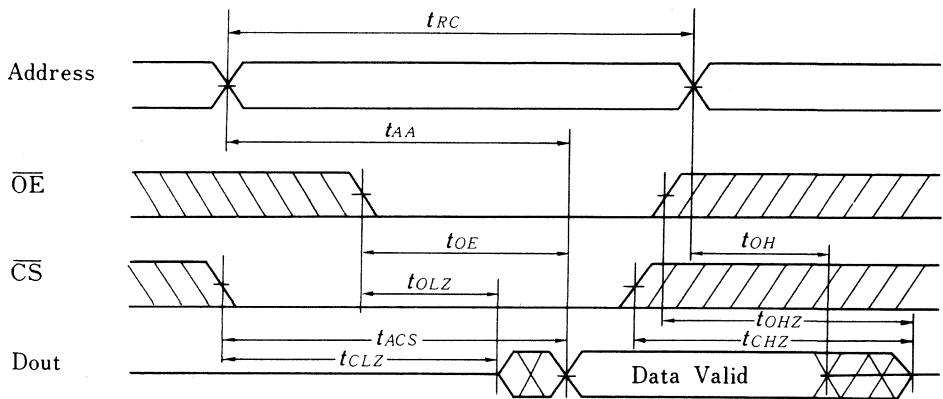
● AC Test Conditions

- Input pulse levels: 0.8V to 2.4V
- Input and Output timing reference levels: 1.5V
- Input rise and fall times: 5ns
- Output load: 1TTL Gate and $C_L = 100\text{pF}$
(Including scope and jig)

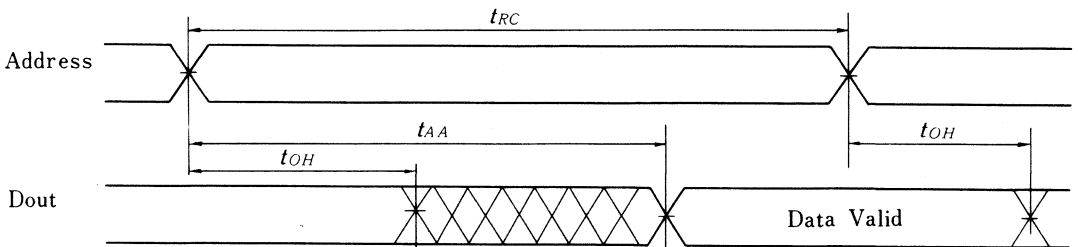
● Read Cycle

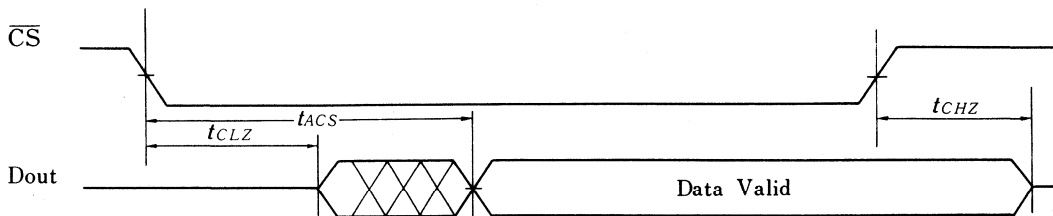
Item	Symbol	HM62256LP/LFP-8		HM62256LP/LFP-10		HM62256LP/LFP-12		HM62256LP/LFP-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Read Cycle Time	t_{RC}	85	—	100	—	120	—	150	—	ns
Address Access Time	t_{AA}	—	85	—	100	—	120	—	150	ns
Chip Select Access Time	t_{ACS}	—	85	—	100	—	120	—	150	ns
Output Enable to Output Valid	t_{OE}	—	45	—	50	—	60	—	70	ns
Output Hold from Address Change	t_{OH}	5	—	10	—	10	—	10	—	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	10	—	10	—	10	—	ns
Output Enable to Output in Low Z	t_{OLZ}	5	—	5	—	5	—	5	—	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	30	0	35	0	40	0	50	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns

● Timing Waveform of Read Cycle No. 1^[1]



● Timing Waveform of Read Cycle No. 2^{[1][2][4]}



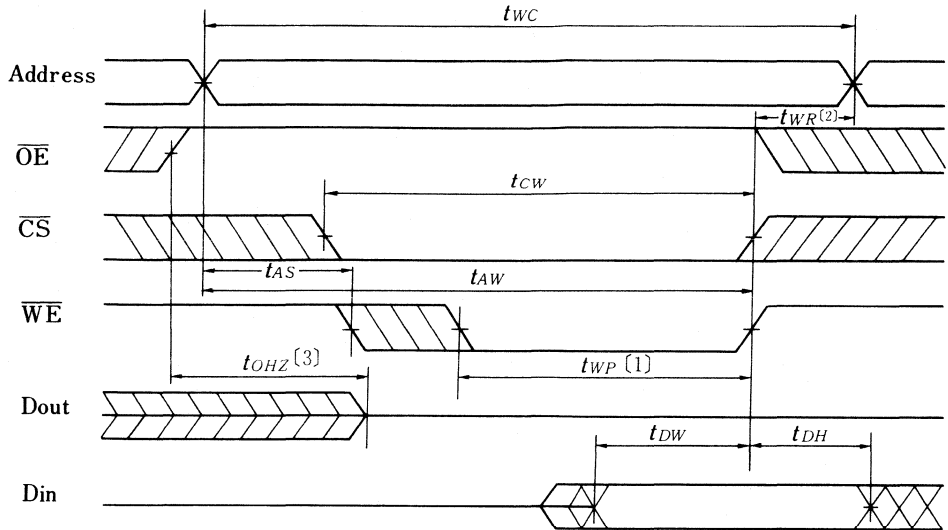
● Timing Waveform of Read Cycle No. 3^{[1][3][4]}


- Notes) 1. \overline{WE} is High for Read Cycle.
 2. Device is continuously selected, $\overline{CS} = V_{IL}$.
 3. Address Valid prior to or coincident with \overline{CS} transition Low.
 4. $\overline{OE} = V_{IL}$.

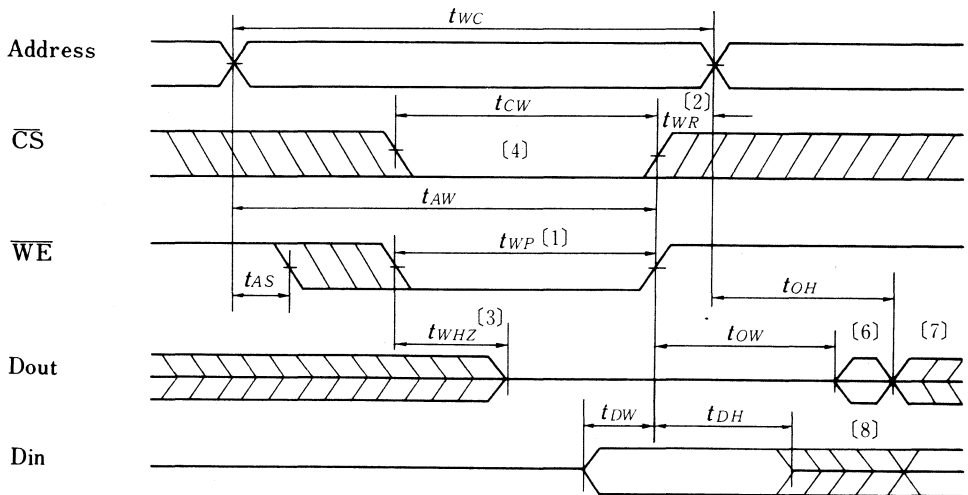
● Write Cycle

Item	Symbol	HM62256LP/LFP-8		HM62256LP/LFP-10		HM62256LP/LFP-12		HM62256LP/LFP-15		Unit
		min.	max.	min.	max.	min.	max.	min.	max.	
Write Cycle Time	t_{WC}	85	—	100	—	120	—	150	—	ns
Chip Selection to End of Write	t_{CW}	75	—	90	—	100	—	120	—	ns
Address Valid to End of Write	t_{AW}	75	—	90	—	100	—	120	—	ns
Address Set Up Time	t_{AS}	0	—	0	—	0	—	0	—	ns
Write Pulse Width	t_{WP}	70	—	75	—	90	—	110	—	ns
Write Recovery Time	t_{WR}	10	—	0	—	0	—	0	—	ns
Write to Output in High Z	t_{WHZ}	0	30	0	35	0	40	0	50	ns
Data to Write Time Overlap	t_{DW}	40	—	40	—	50	—	60	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	0	—	ns
Output Disable to Output in High Z	t_{OHZ}	0	30	0	35	0	40	0	50	ns
Output Active from End of Write	t_{OW}	5	—	5	—	5	—	5	—	ns

● Timing Waveform of Write Cycle No. 1 ($\overline{\text{OE}}$ Clock)



● Timing Waveform of Write Cycle No. 2^[5] ($\overline{\text{OE}}$ Low Fixed)



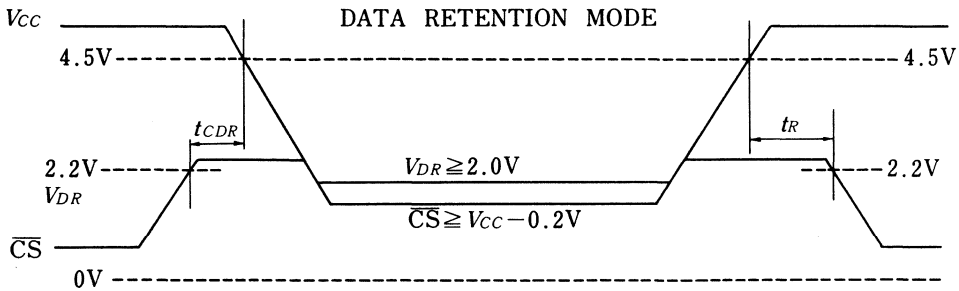
- Notes:
1. A write occurs during the overlap (t_{WP}) of a low $\overline{\text{CS}}$ and a low $\overline{\text{WE}}$.
 2. t_{WR} is measured from the earlier of $\overline{\text{CS}}$ or $\overline{\text{WE}}$ going high to the end of write cycle.
 3. During this period, I/O pins are in the output state. The input signals out of phase must not be applied
 4. If the $\overline{\text{CS}}$ low transition occurs simultaneously with the $\overline{\text{WE}}$ low transition or after the $\overline{\text{WE}}$ low transition, outputs remain in a high impedance state.
 5. $\overline{\text{OE}}$ is continuously low. ($\overline{\text{OE}} = V_{IL}$)
 6. Dout is in the same phase of written data of this write cycle.
 7. Dout is the read data of next address.
 8. If $\overline{\text{CS}}$ is low during this period, I/O pins are in the output state. The input signals out of phase must not be applied to I/O Pins.

■ **LOW V_{CC} DATA RETENTION CHARACTERISTICS** ($T_a=0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit
V_{CC} for Data Retention	V_{DR}	$\overline{CS} \geq V_{CC} - 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC} = 3.0\text{V}, \overline{CS} \geq 2.8\text{V}$	-	-	50	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R		t_{RC}^*	-	-	ns

* t_{RC} = Read Cycle Time

● **Low V_{CC} Data Retention Waveform**

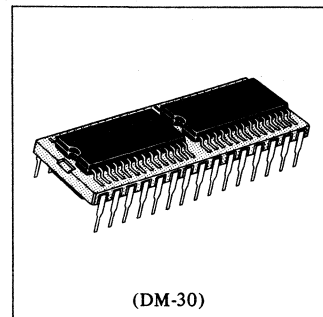


HM66202 Series

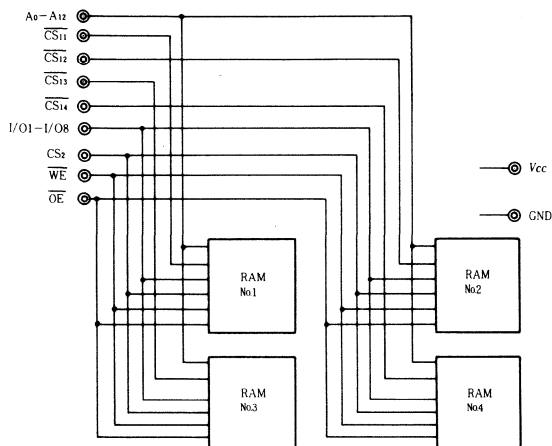
32768-word X 8-bit High Density Static RAM Module

■ FEATURES

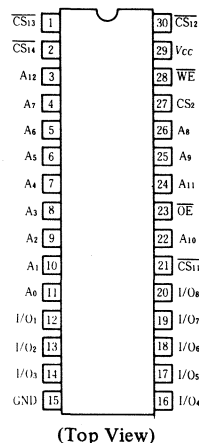
- Industry Standard 30 pin DIP Mechanical Outline.
- Single +5V Supply.
- High speed: Fast Access Time 120ns/150ns/200ns max.
- Equal Access and Cycle Time.
- Completely Static RAM: No Clock or Timing Strobe Required.
- \overline{CS}_{11} , \overline{CS}_{12} , \overline{CS}_{13} , \overline{CS}_{14} for Chip Decode.
- Low Power Standby and Low Power Operation; Standby: 0.4mW typ. Operation: 200mW typ.
- Common Data Input and Output, Three State Output.
- Directly TTL Compatible: All Input and Output.



■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ TRUTH TABLE

Mode	\overline{WE}	CS_2	\overline{OE}	I/O	Current	Ref. Cycle
Not Selected (Power Down)	X	L	X	High-Z	I_{SB} , I_{SB2}	
Output Disabled	H	H	H	High-Z	I_{CC} , I_{CC1}	
Read	H	H	L	Dout	I_{CC} , I_{CC1}	
Write	L	H	H	Din	I_{CC} , I_{CC1}	Write Cycle (1)
	L	H	L	Din	I_{CC} , I_{CC1}	Write Cycle (2)

Notes) 1. X: H or L

2. \overline{CS}_{11} , \overline{CS}_{12} , \overline{CS}_{13} and \overline{CS}_{14} are chip decode use only. When one chip is selected, others are not selected.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{in}	-0.5* to 7	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{bias}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

* -3.0V (pulse width 50ns)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	-	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.3*	-	0.8	V

* -3.0V (Pulse width 50ns)

■ DC AND OPERATING CHARACTERISTICS ($T_a=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $\text{GND}=0\text{V}$)

Parameter	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	I_{LI}	$V_{in}=\text{GND}$ to V_{CC}	-	-	10	μA
Output Leakage Current	I_{LO}	$\text{CS}2=V_{IL}$ or $\overline{\text{OE}}=V_{IH}$ or $\overline{\text{WE}}=V_{IL}$, $V_{I/O}=\text{GND}$ to V_{CC}	-	-	10	μA
Operating Power Supply Current: DC	I_{CC}	$\text{CS}2=V_{IH}$, $I_{I/O}=0\text{mA}$	-	40	90	mA
Average Operating Current	I_{CC1}	Min. cycle, duty=100%, $I_{I/O}=0\text{mA}$	-	60	120	mA
Standby Power Supply Current (1)	I_{SB}	$\text{CS}2=V_{IL}$	-	4	12	mA
Standby Power Supply Current(3):DC	I_{SB2}	$\text{CS}2 \leq 0.2\text{V}$, V_{IL} min=-0.3V	-	0.08	8	mA
Output Low Voltage	V_{OL}	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	-	-	V

*: Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^{\circ}\text{C}$ and specified loading

■ **CAPACITANCE** ($T_a=25^\circ\text{C}$, $f=1.0\text{ MHz}$) [1]

Parameter	Symbol	typ.	max.	Unit	Test Conditions
Input Capacitance	C_{in}	–	40	pF	$V_{in}=0\text{V}$
Input/Output Capacitance	$C_{I/O}$	–	40	pF	$V_{I/O}=0\text{V}$

Note) This parameter is sampled and not 100% tested.

■ **AC CHARACTERISTICS** ($T_a=0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC}=5.0\text{V}\pm 10\%$ unless otherwise noted)

● AC Test Conditions

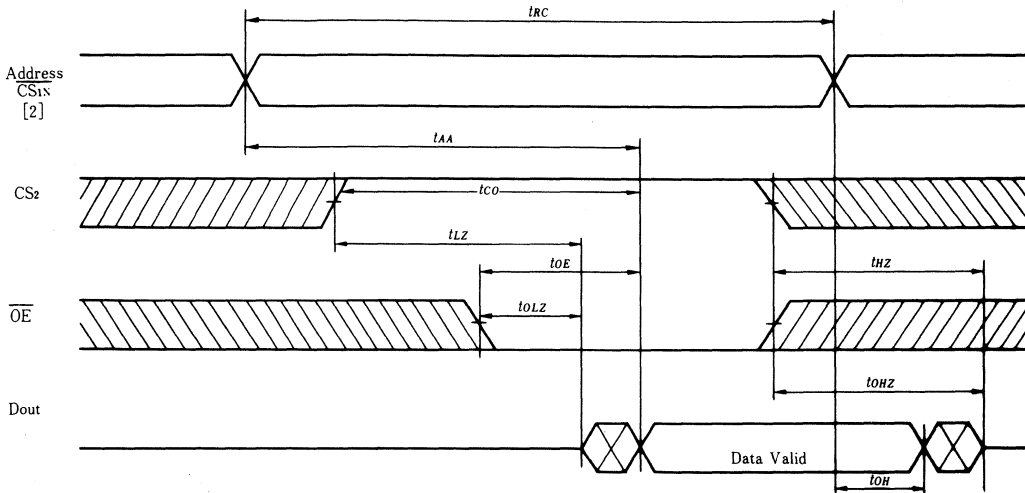
Input pulse levels	0.8V to 2.4V
Input rise and fall times	10ns
Input and Output timing reference level	1.5V
Output load	1TTL Gate and $C_L=100\text{pF}$ (Including scope & Jig)

● **READ CYCLE**

Parameter	Symbol	HM66202-12		HM66202-15		HM66202-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Selection (CS2) to Output	t_{CO}	–	120	–	150	–	200	ns
Output Enable (\overline{OE}) to Output Valid	t_{OE}	–	60	–	70	–	100	ns
Chip Selection (CS2) to Output in Low Z	t_{LZ}	10	–	15	–	15	–	ns
Output Enable (\overline{OE}) to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection (CS2) to Output in High Z	t_{HZ}^*	0	40	0	50	0	60	ns
Output Disable (\overline{OE}) to Output in High Z	t_{OHZ}^*	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	15	–	ns

Note) *: t_{HZ} and t_{OHZ} define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

● Timing Waveform of Read Cycle⁽¹⁾

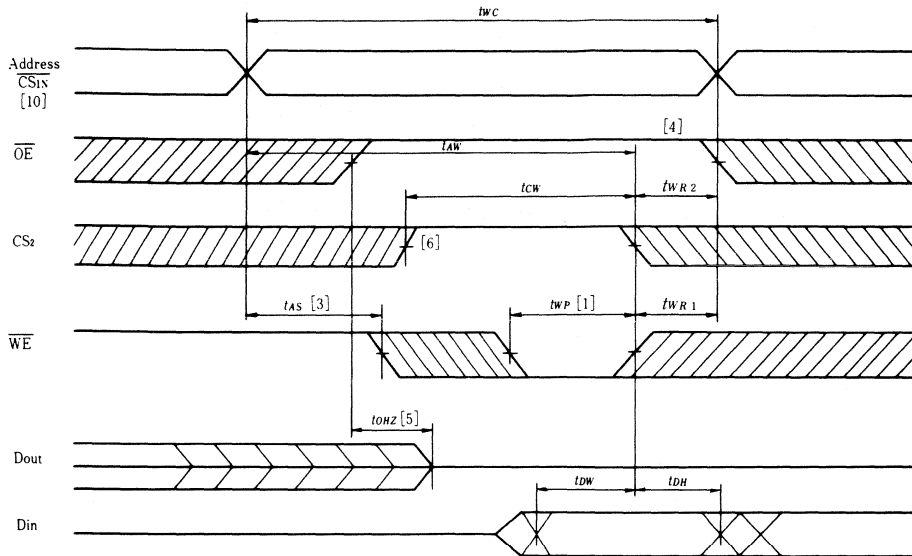


- Notes) 1. \overline{WE} is High for Read Cycle.
 2. \overline{CS}_{11} , \overline{CS}_{12} , \overline{CS}_{13} and \overline{CS}_{14} are used only for chip decoding. When one chip is selected, others are not selected. When one \overline{CS}_{1N} pin is in V_{IL} level, other \overline{CS}_{1N} pins must not be in V_{IL} level. N=1, 2, 3, 4.

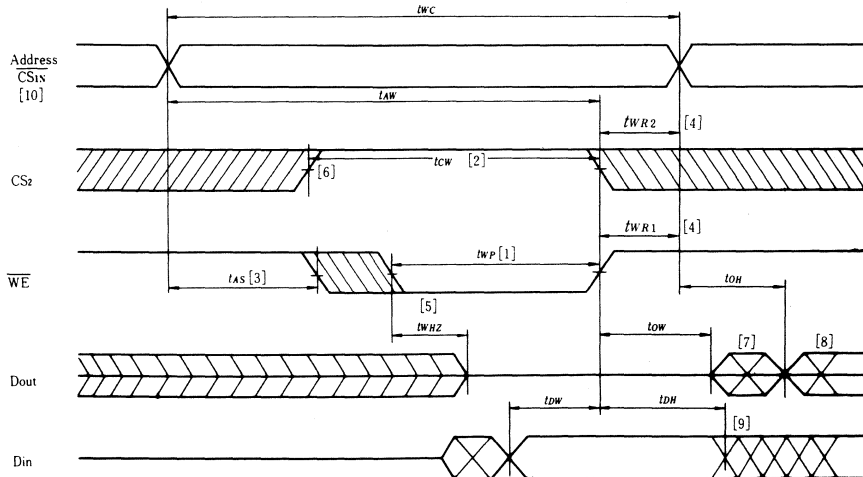
● WRITE CYCLE

Parameter	Symbol	HM66202-12		HM66202-15		HM66202-20		Unit	
		min	max	min	max	min	max		
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns	
Chip Selection to End of Write	t_{CW}	85	—	100	—	120	—	ns	
Address Set Up Time	t_{AS}	0	—	0	—	0	—	ns	
Address Valid to End of Write	t_{AW}	85	—	100	—	120	—	ns	
Write Pulse Width	t_{WP}	70	—	90	—	100	—	ns	
Write Recovery Time	\overline{WE}	t_{WR1}	10	—	10	—	10	—	ns
	CS_2	t_{WR2}	15	—	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	40	0	50	0	60	ns	
Data to Write Time Overlap	t_{DW}	50	—	60	—	70	—	ns	
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns	
Output Disable (\overline{OE}) to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns	
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns	

● Timing Waveform of Write Cycle⁽¹⁾ ($\overline{\text{OE}}$ Clock)

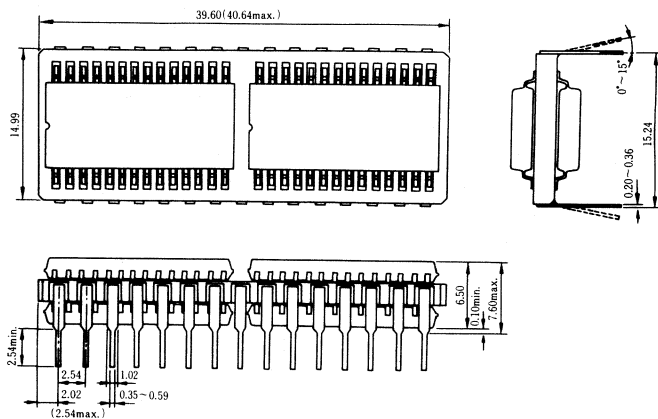


● Timing Waveform of Write Cycle⁽²⁾ ($\overline{\text{OE}}$ Low Fixed)



- Notes):
1. A write occurs during the overlap of a high CS_2 and a low $\overline{\text{WE}}$. A write begins at the later transition of CS_2 going high or $\overline{\text{WE}}$ going low. A write ends at the earlier transition of CS_2 going low or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
 2. t_{CW} is measured from CS_2 going high to the end of write.
 3. t_{AS} is measured from the address valid to the beginning of write.
 4. t_{WR} is measured from the end of write to the address change.
 5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
 6. If CS_2 goes high simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
 7. Dout is the same phase of the latest written data in this write cycle.
 8. Dout is the read data of next address.
 9. If CS_2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
 10. $\overline{\text{CS}}_{11}$, $\overline{\text{CS}}_{12}$, $\overline{\text{CS}}_{13}$ and $\overline{\text{CS}}_{14}$ are used only for chip decoding. When one chip is selected, others are not selected. When one CS_{1N} pin is in V_{IL} level, other CS_{1N} pins must not be in V_{IL} level. $N=1, 2, 3, 4$.

■ PACKAGE OUTLINE (Dimensions in mm)

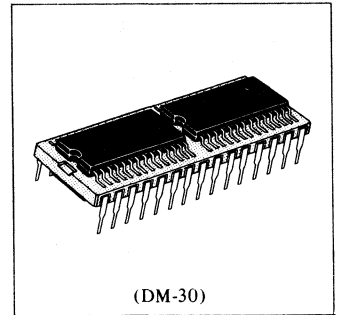


HM66202L Series

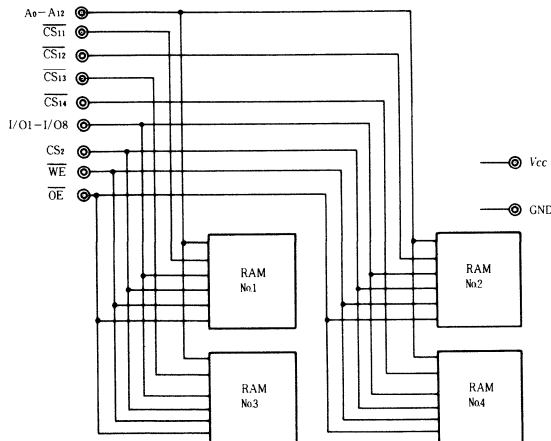
32768-word X 8-bit High Density Static RAM Module

■ FEATURES

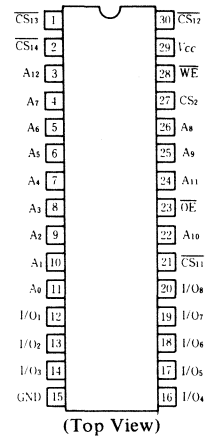
- Industry Standard 30 pin DIP Mechanical Outline.
- Single +5V Supply.
- High speed: Fast Access Time 120ns/150ns/200ns max.
- Equal Access and Cycle Time.
- Completely Static RAM: No Clock or Timing Strobe Required.
- $\overline{CS}_{1,1}$, $\overline{CS}_{1,2}$, $\overline{CS}_{1,3}$, $\overline{CS}_{1,4}$ for Chip Decode.
- Low Power Standby and Low Power Operation; Standby: 40 μ W typ. Operation: 200mW typ.
- Common Data Input and Output, Three State Output.
- Directly TTL Compatible: All Input and Output.



■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ TRUTH TABLE

Mode	\overline{WE}	CS2	\overline{OE}	I/O	Current	Ref. Cycle
Not Selected (Power Down)	X	L	X	High-Z	I_{SB} , I_{SB2}	
Output Disabled	H	H	H	High-Z	I_{CC} , I_{CC1}	
Read	H	H	L	Dout	I_{CC} , I_{CC1}	
Write	L	H	H	Din	I_{CC} , I_{CC1}	Write Cycle (1)
	L	H	L	Din	I_{CC} , I_{CC1}	Write Cycle (2)

Notes) 1. X: H or L

2. $\overline{CS}_{1,1}$, $\overline{CS}_{1,2}$, $\overline{CS}_{1,3}$ and $CS_{1,4}$ are chip decode use only. When one chip is selected, others are not selected.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on Any Pin Relative to GND	V_{in}	-0.5* to 7	V
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{bias}	-10 to +85	°C
Power Dissipation	P_T	1.0	W

*: -3.0V (Pulse Width 50ns)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	GND	0	0	0	V
Input High (logic 1) Voltage	V_{IH}	2.2	-	6.0	V
Input Low (logic 0) Voltage	V_{IL}	-0.3*	-	0.8	V

*: -3.0V (Pulse width 50ns)

■ DC AND OPERATING CHARACTERISTICS ($T_a=0^{\circ}\text{C}$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $\text{GND}=0\text{V}$)

Parameter	Symbol	Test Conditions	min	typ*	max	Unit
Input Leakage Current	I_{LI}	$V_{in}=\text{GND}$ to V_{CC}	-	-	2	μA
Output Leakage Current	I_{LO}	$\text{CS}2=V_{IL}$ or $\overline{\text{OE}}=V_{IH}$ or $\overline{\text{WE}}=V_{IL}$, $V_{I/O}=\text{GND}$ to V_{CC}	-	-	2	μA
Operating Power Supply Current: DC	I_{CC}	$\text{CS}2=V_{IH}$, $I_{I/O}=0\text{mA}$	-	40	90	mA
Average Operating Current	I_{CC1}	Min. cycle, duty -100%, $I_{I/O}=0\text{mA}$	-	60	120	mA
Standby Power Supply Current (1)	I_{SB}	$\text{CS}2=V_{IL}$	-	4	12	mA
Standby Power Supply Current(3):DC	I_{SB2}	$\text{CS}2 \leq 0.2\text{V}$, V_{IL} min = -0.3V	-	8	400	μA
Output Low Voltage	V_{OL}	$I_{OL}=2.1\text{mA}$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH}=-1.0\text{mA}$	2.4	-	-	V

*: Typical limits are at $V_{CC}=5.0\text{V}$, $T_a=+25^{\circ}\text{C}$ and specified loading

■ **CAPACITANCE** ($T_a=25^\circ\text{C}$, $f=1.0\text{ MHz}$) [1]

Parameter	Symbol	typ.	max.	Unit	Test Conditions
Input Capacitance	C_{in}	–	40	pF	$V_{in}=0\text{V}$
Input/Output Capacitance	$C_{I/O}$	–	40	pF	$V_{I/O}=0\text{V}$

Note) This parameter is sampled and not 100% tested.

■ **AC CHARACTERISTICS** ($T_a=0^\circ\text{C}$ to $+70^\circ\text{C}$, $V_{CC}=5.0\text{V}\pm 10\%$ unless otherwise noted)

● AC Test Conditions

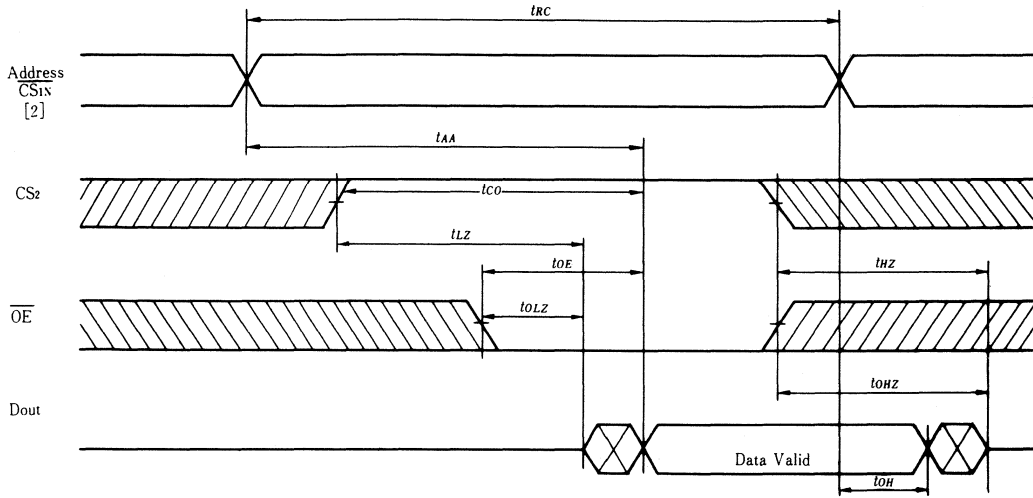
Input pulse levels	0.8V to 2.4V
Input rise and fall times	10ns
Input and Output timing reference level	1.5V
Output load	ITTL Gate and $C_L=100\text{pF}$ (Including scope & Jig).

● **READ CYCLE**

Parameter	Symbol	HM66202L-12		HM66202L-15		HM66202L-20		Unit
		min	max	min	max	min	max	
Read Cycle Time	t_{RC}	120	–	150	–	200	–	ns
Address Access Time	t_{AA}	–	120	–	150	–	200	ns
Chip Selection (CS2) to Output	t_{CO}	–	120	–	150	–	200	ns
Output Enable (\overline{OE}) to Output Valid	t_{OE}	–	60	–	70	–	100	ns
Chip Selection (CS2) to Output in Low Z	t_{LZ}	10	–	15	–	15	–	ns
Output Enable (\overline{OE}) to Output in Low Z	t_{OLZ}	5	–	5	–	5	–	ns
Chip Deselection (CS2) to Output in High Z	t_{HZ}^*	0	40	0	50	0	60	ns
Output Disable (\overline{OE}) to Output in High Z	t_{OHZ}^*	0	40	0	50	0	60	ns
Output Hold from Address Change	t_{OH}	10	–	15	–	15	–	ns

Note) *: t_{HZ} and t_{OHZ} define the time at which the output achieves the open circuit condition and are not referenced to output voltage levels.

● Timing Waveform of Read Cycle⁽¹⁾

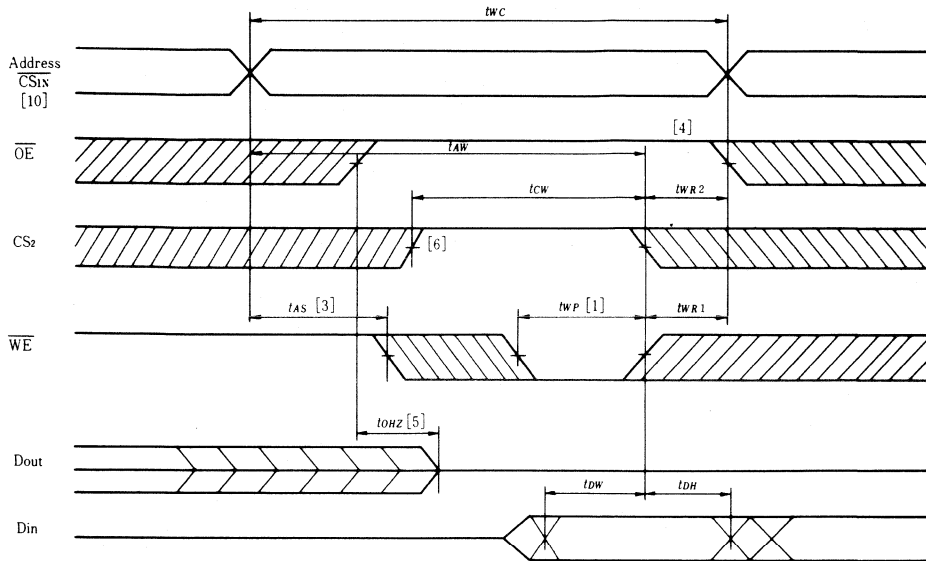


- Notes) 1. \overline{WE} is High for Read Cycle.
 2. \overline{CS}_{11} , \overline{CS}_{12} , \overline{CS}_{13} and \overline{CS}_{14} are used only for chip decoding. When one chip is selected, others are not selected. When one \overline{CS}_{IN} pin is in V_{IL} level, other \overline{CS}_{IN} pins must not be in V_{IL} level. N=1, 2, 3, 4.

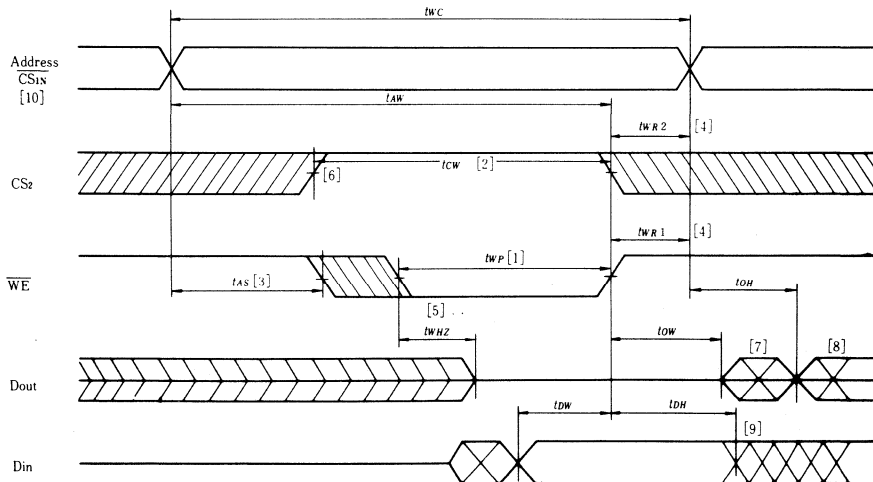
● WRITE CYCLE

Parameter	Symbol	HM66202L-12		HM66202L-15		HM66202L-20		Unit
		min	max	min	max	min	max	
Write Cycle Time	t_{WC}	120	—	150	—	200	—	ns
Chip Selection to End of Write	t_{CW}	85	—	100	—	120	—	ns
Address Set Up Time	t_{AS}	0	—	0	—	0	—	ns
Address Valid to End of Write	t_{AW}	85	—	100	—	120	—	ns
Write Pulse Width	t_{WP}	70	—	90	—	100	—	ns
Write Recovery Time	\overline{WE} t_{WR1}	10	—	10	—	10	—	ns
	CS_2 t_{WR2}	15	—	15	—	15	—	ns
Write to Output in High Z	t_{WHZ}	0	40	0	50	0	60	ns
Data to Write Time Overlap	t_{DW}	50	—	60	—	70	—	ns
Data Hold from Write Time	t_{DH}	0	—	0	—	0	—	ns
Output Disable (\overline{OE}) to Output in High Z	t_{OHZ}	0	40	0	50	0	60	ns
Output Active from End of Write	t_{OW}	5	—	10	—	10	—	ns

● Timing Waveform of Write Cycle⁽¹⁾ ($\overline{\text{OE}}$ Clock)



● Timing Waveform of Write Cycle⁽²⁾ ($\overline{\text{OE}}$ Low Fixed)



- Notes): 1. A write occurs during the overlap of a high CS_2 and a low $\overline{\text{WE}}$. A write begins at the later transition of CS_2 going high or $\overline{\text{WE}}$ going low. A write ends at the earlier transition of CS_2 going low or $\overline{\text{WE}}$ going high. t_{WP} is measured from the beginning of write to the end of write.
2. t_{CW} is measured from CS_2 going high to the end of write.
3. t_{AS} is measured from the address valid to the beginning of write.
4. t_{WR} is measured from the end of write to the address change.
5. During this period, I/O pins are in the output state, therefore the input signals of opposite phase to the outputs must not be applied.
6. If CS_2 goes high simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
7. Dout is the same phase of the latest written data in this write cycle.
8. Dout is the read data of next address.
9. If CS_2 is high during this period, I/O pins are in the output state. Therefore, the input signals of opposite phase to the outputs must not be applied to them.
10. $\overline{\text{CS}}_{11}$, $\overline{\text{CS}}_{12}$, $\overline{\text{CS}}_{13}$ and $\overline{\text{CS}}_{14}$ are used only for chip decoding. When one chip is selected, others are not selected. When one CS_{1N} pin is in V_{IL} level, other CS_{1N} pins must not be in V_{IL} level. $N=1, 2, 3, 4$.

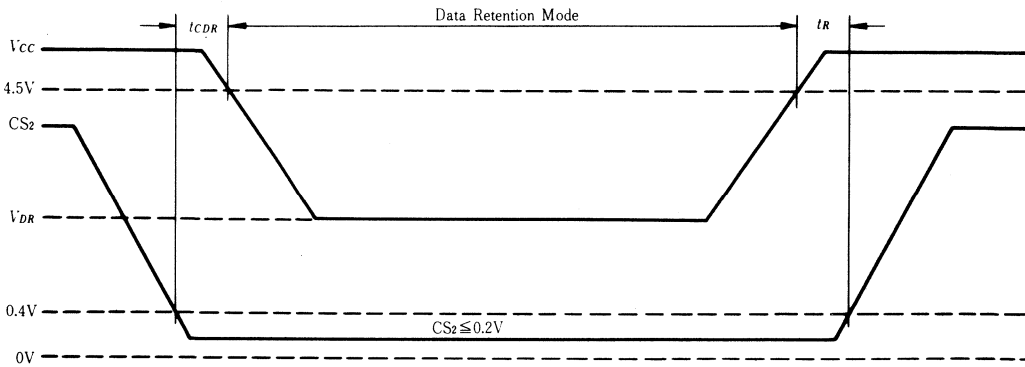
■ LOW V_{CC} DATA RETENTION CHARACTERISTICS ($T_a=0$ to $+70^{\circ}\text{C}$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
V_{CC} for Data Retention	V_{DR}	$CS2 \leq 0.2\text{V}$	2.0	-	-	V
Data Retention Current	I_{CCDR}	$V_{CC}=3.0\text{V}$, $CS2 \leq 0.2\text{V}$, $V_{IL} \text{ min} = -0.3\text{V}$	-	4	200*	μA
Chip Deselect to Data Retention Time	t_{CDR}	See Retention Waveform	0	-	-	ns
Operation Recovery Time	t_R		** t_{RC}	-	-	ns

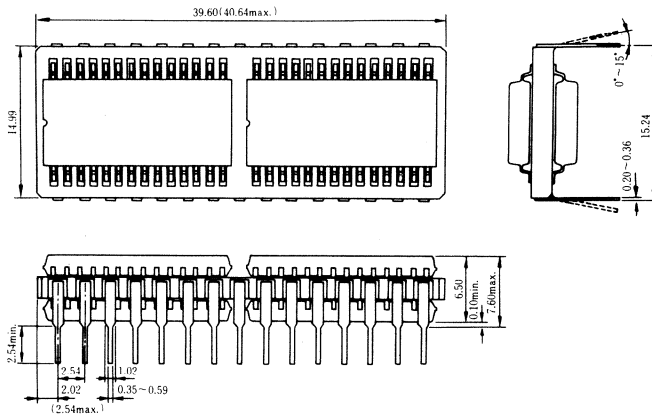
* $80\mu\text{A}$ max. under the condition of $T_a=0$ to $+40^{\circ}\text{C}$

** t_{RC} =Read Cycle Time

■ Low V_{CC} Data Retention Waveform



■ PACKAGE OUTLINE (Dimensions in mm)



HM66203Series, HM66203L Series

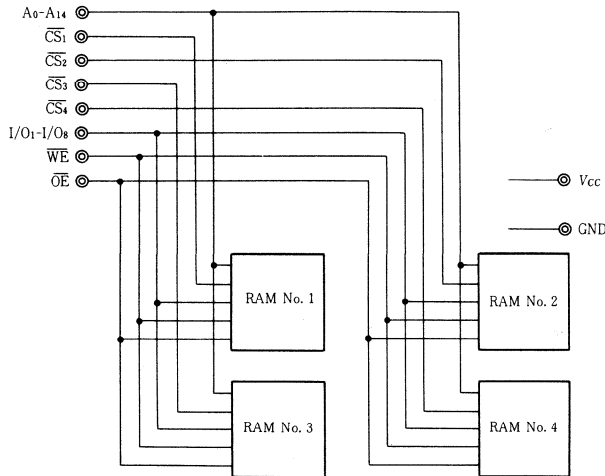
Under Development

131072-word x 8-bit High Density Static RAM Module

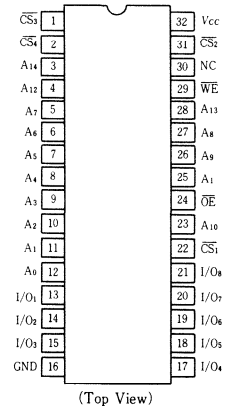
■FEATURES

- Industry Standard 32 pin DIP Mechanical Outline.
- High speed: Fast Access Time 100ns/120ns/150ns max.
- Completely Static RAM:
 - No Clock or Timing Strobe Required.
- Low Power Standby and Low Power Operation;
 - Standby: 40μW typ. (L Type)
 - Operation: 50mW typ. (f = 1MHz)
- Common Data Input and Output, Three State Outputs.
- Directly TTL Compatible: All Inputs and Outputs.

■BLOCK DIAGRAM



■PIN ARRANGEMENT



■TRUTH TABLE

Mode	CS1~CS4	WE	OE	I/O	Current	Note
Not Selected (Power Down)	H	×	×	High-Z	I_{SB}, I_{SB1}	
Read	*L	H	L	Dout	I_{CC}	Read Cycle (1)~(3)
Write	*L	L	H	Din	I_{CC}	Write Cycle (1)
	*L	L	L	Din	I_{CC}	Write Cycle (2)

×: Don't Care (H or L)

*: CS1, CS2, CS3, and CS4 pins are used for chip decoding.

Only one chip should be selected.

Two or more chips must not be selected at one time.

MOS PSEUDO STATIC RAM

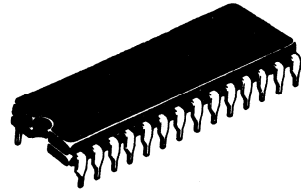
HM65256AP Series, HM65256ASP Series

32768-word X 8-bit High Speed Pseudo Static RAM

■ FEATURES

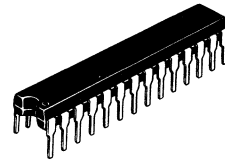
- Single 5V ($\pm 10\%$)
- High Speed
 - Access Time
 - \overline{CE} Access Time 120/150/200ns
 - Address Access Time 60/75/100ns
 - (in static column mode)
 - Cycle Time
 - Random Read/Write Cycle Time 190/235/310ns
 - Static Column Mode Cycle Time 65/80/105ns
- Low Power
 - 175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
 - Address Refresh
 - Automatic Refresh
 - Self Refresh
 - Hidden Refresh

HM65256AP Series



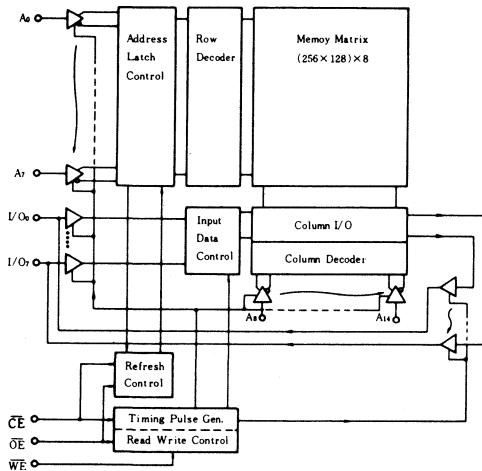
(DP-28)

HM65256ASP Series

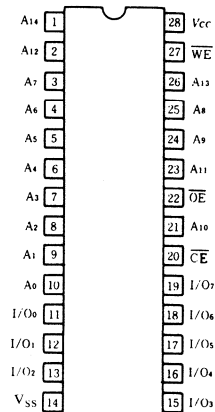


(DP-28N)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

\overline{CE}	\overline{OE} at \overline{CE} going Low	\overline{OE}	\overline{WE}	I/O Pin	Mode	Notes
L	H	L	H	Low Z	Read	
L	H	H	L	High Z	Write	
L	H	H	H	High Z	–	
L	L	L	X	Low Z	Hidden Refresh	Output Buffers must keep Low Impedance State in previous Precharge Cycle.
L	L	X	X	High Z	Auto-matic Refresh	Output Buffers must turn off in previous Precharge Cycle.
L	X	X	X	High Z	Self Refresh	\overline{CE} Pulse Width $\geq 300\mu$ sec.
H	X	H	X	High Z	Standby	
H	X	L	X	X	–	Once Dout Buffers turn off, Output Buffers remain in High Impedance State.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Ratings	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Power Dissipation	P_T	1	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Temperature under Bias	T_{bias}	-10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-1.0	–	0.8	V

■ DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $T_a=0$ to +70°C)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O} = 0$ $t_{cyc} = \text{min.}$	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE} = V_{IH}$, $\overline{OE} = V_{IH}$	–	1	2	mA
Standby Power Supply Current	I_{SB2}	$\overline{CE} > V_{CC} - 0.2V$ $\overline{OE} > V_{CC} - 0.2V$	–	0.4	0.6	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE} = V_{IL}$	–	0.6	1	mA
Input Leakage Current	I_{LI}	$V_{CC} = 5.5V$ $V_{in} = V_{SS}$ to V_{CC}	-10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	-10	–	10	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1$ mA	–	–	0.4	V
	V_{OH}	$I_{OH} = -1$ mA	2.4	–	–	V

■ **AC CHARACTERISTICS** ($V_{CC} = 5V \pm 10\%$, $T_a = 0$ to $+70^\circ C$)

● **AC TEST CONDITIONS**

- Input Pulse Levels . . . 0.4 to 2.4V
- Input Rise and Fall Times . . . 5 ns
- Input Timing Reference Levels . . . 0.8V, 2.2V
- Output Timing Reference Levels . . . $V_{OH} = 2.0V$,
 $V_{OL} = 0.8V$
- Output Load . . . 1TTL Gate and $C_L = 100pF$
(including jig and scope)

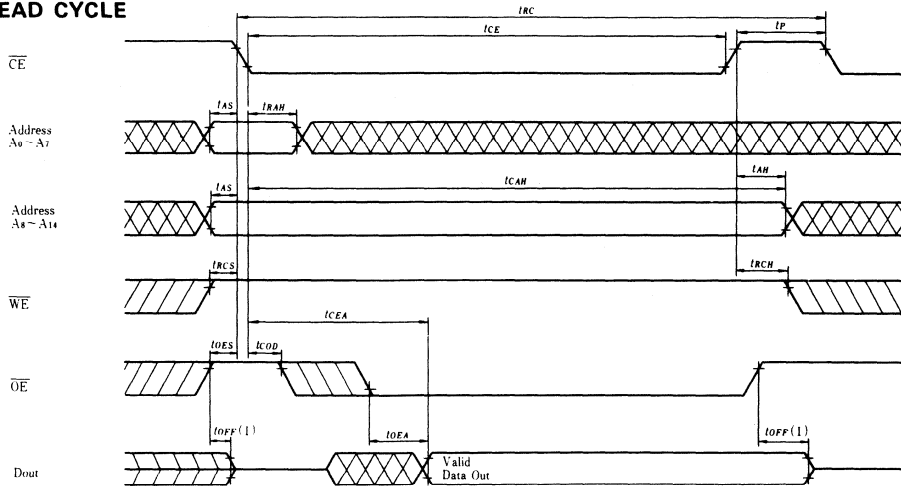
● **READ AND WRITE MODE**

Item	Symbol	HM65256A-12		HM65256A-15		HM65256A-20		Unit	Note
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	190	—	235	—	310	—	ns	
Read Modify Write Cycle Time	t_{RWC}	265	—	325	—	425	—	ns	
Chip Enable Access Time	t_{CEA}	—	120	—	150	—	200	ns	
Address Access Time	t_{AA}	—	60	—	75	—	100	ns	
Output Enable Access Time	t_{OEA}	—	50	—	60	—	75	ns	
Output Buffer Turn-off Delay	t_{OFF}	5	20	5	25	5	35	ns	(1)
Chip Enable Pulse Width	t_{CE}	120	10000	150	10000	200	10000	ns	
Chip Enable Precharge Time	t_p	60n	4m	75n	4m	100n	4m	s	
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	20	—	25	—	30	—	ns	
Column Address Hold Time	t_{CAH}	120	—	150	—	200	—	ns	
Column Address Hold Time from CE going High	t_{AH}	0	—	0	—	0	—	ns	
Static Mode Read or Write Cycle Time	t_{RSC}	65	—	80	—	105	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Output Enable Set-up Time	t_{OES}	0	—	0	—	0	—	ns	
Chip Enable to Output Enable Delay Time	t_{COD}	20	—	25	—	30	—	ns	
Output Hold Time from Column Address	t_{OH}	5	—	5	—	10	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	
Write Command Hold Time	t_{WCH}	30	—	35	—	40	—	ns	
Write Command Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Command to Chip Enable Lead Time	t_{WCL}	45	—	55	—	70	—	ns	
Column Address Set-up Time for Write	t_{ASW}	0	—	0	—	0	—	ns	
Write Command to Column Address Lead Time	t_{WAL}	45	—	55	—	70	—	ns	
Data In Set-up Time	t_{DS}	0	—	0	—	0	—	ns	
Data In Hold Time for Early Write	t_{DHC}	30	—	35	—	40	—	ns	
Data In Hold Time for Late Write	t_{DHW}	20	—	25	—	30	—	ns	
Output Enable to Data In Delay Time	t_{ODD}	20	—	25	—	35	—	ns	(4)
Data In Floating to Output Enable Delay Time	t_{DFO}	0	—	0	—	0	—	ns	(4)
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	(7)
Refresh Command Set-up Time	t_{RFS}	0	—	0	—	0	—	ns	
Refresh Command Hold Time	t_{RFH}	20	—	25	—	30	—	ns	
Chip Enable Pulse Width for Self Refresh	t_{CEF}	300	—	300	—	300	—	μs	

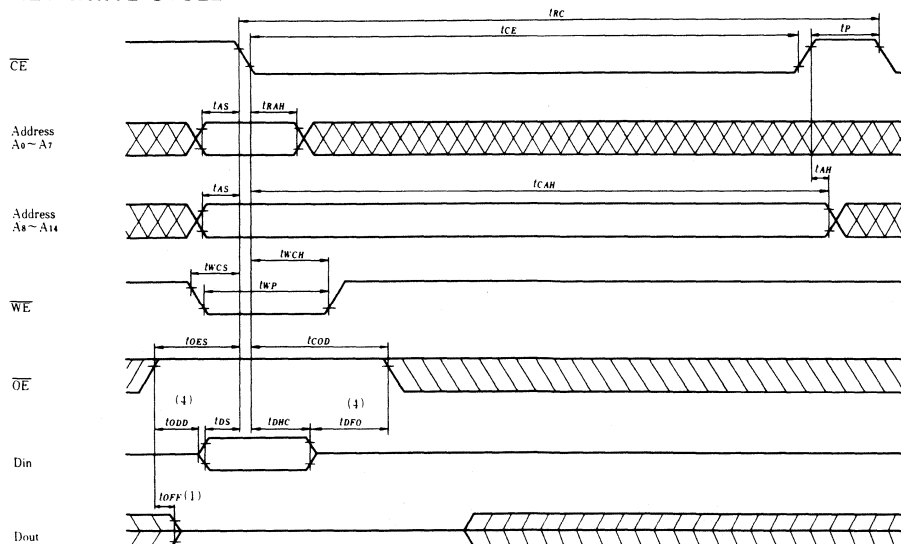
Item	Symbol	HM65256A-12		HM65256A-15		HM65256A-20		Unit	Note
		min	max	min	max	min	max		
Chip Enable Pre-charge Time after Self Refresh	t_{PF}	190	-	235	-	310	-	ns	
Refresh Period	t_{REF}	-	4	-	4	-	4	ms	256 cycle

- Notes:
- t_{OFF} (max) defines the time at which the output achieves the open circuit condition.
 - Write starts with the later of \overline{CE} or \overline{WE} going low (except during a refresh cycle).
 - If the first write pulse is applied within t_{CE} (min), the second write pulse must be applied after t_{CE} (min).
 - If input signals of opposite phase to the outputs are applied in write cycle, \overline{OE} must disable output buffers prior to applying data to the device and data inputs must be floating prior to \overline{OE} turning on output buffers.
 - Once \overline{OE} goes high and output buffers turn off in precharge cycle, automatic refresh cycle can start. Output buffers remain in high impedance state in automatic refresh cycle.
 - Output buffers are in high impedance state, and not controlled by \overline{OE} in self refresh mode.
 - V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .

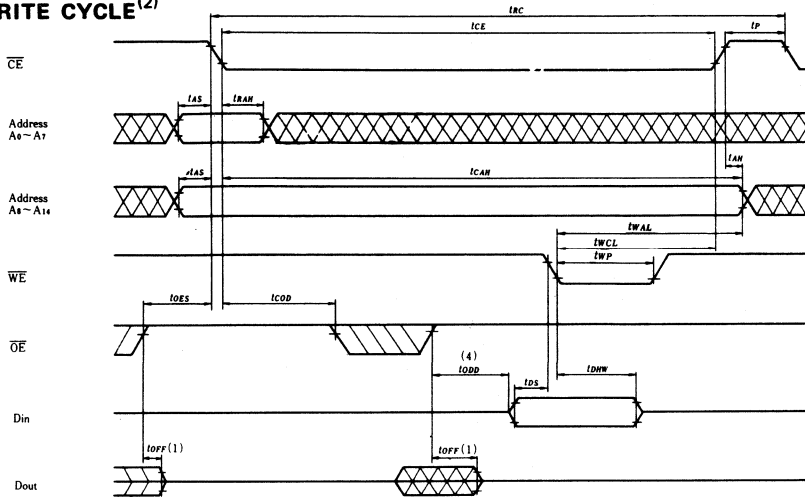
● READ CYCLE



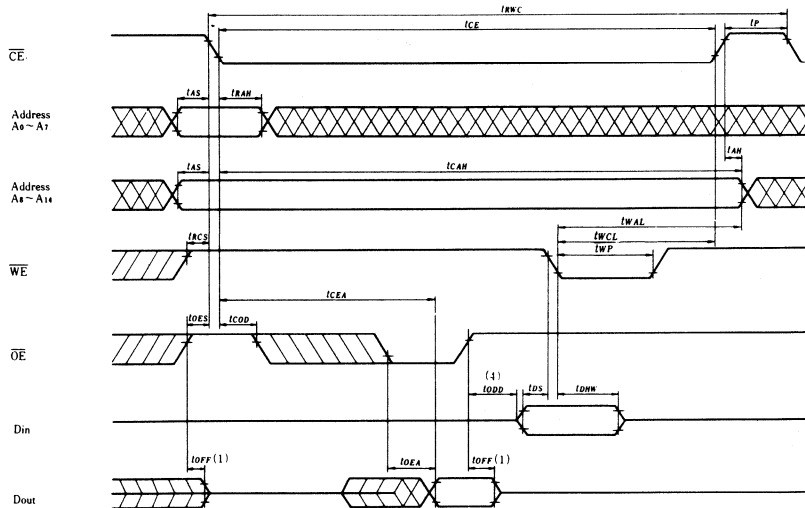
● EARLY WRITE CYCLE (2)



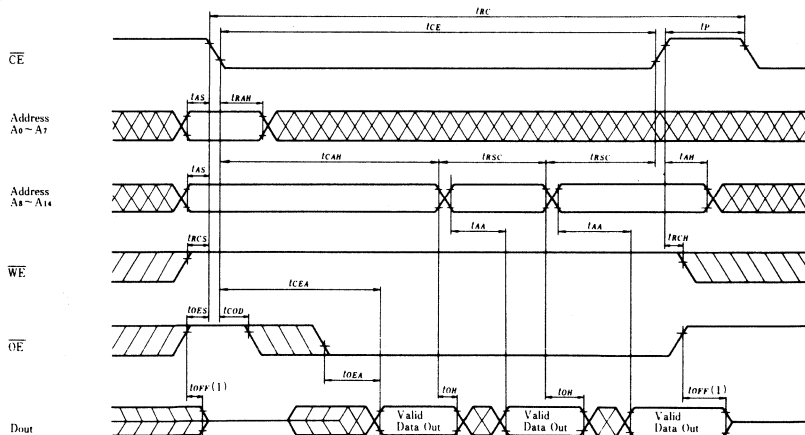
● LATE WRITE CYCLE (2)



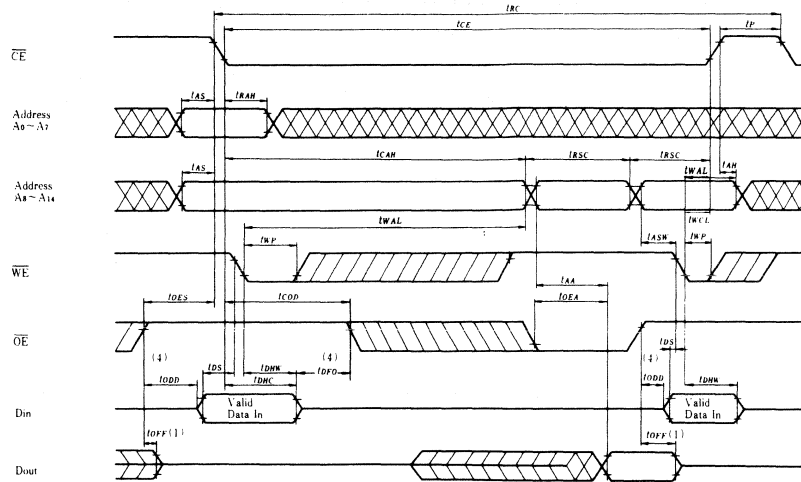
● READ MODIFY WRITE CYCLE (2)



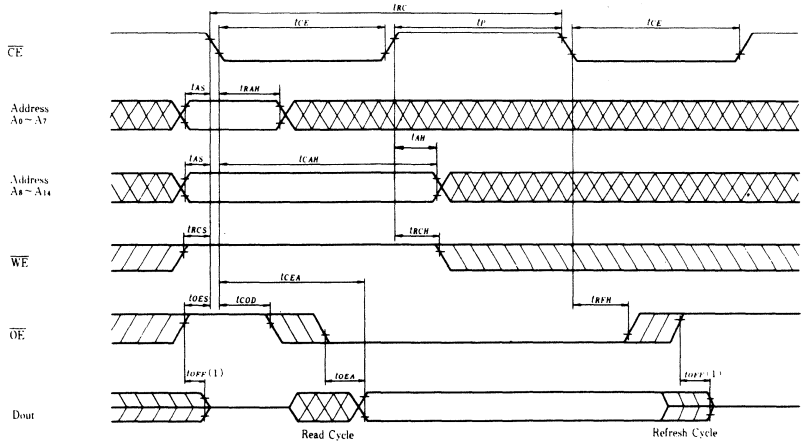
● STATIC COLUMN MODE READ CYCLE



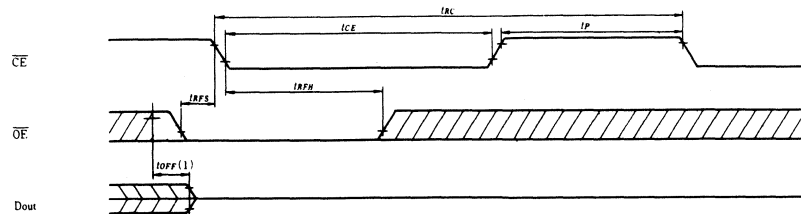
● **STATIC COLUMN MODE WRITE CYCLE (2),(3)**



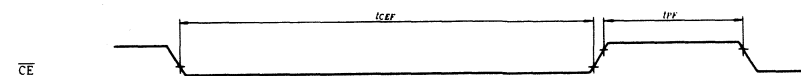
● **HIDDEN REFRESH CYCLE**



● **AUTOMATIC REFRESH CYCLE (5)**



● **SELF REFRESH CYCLE (6)**



● Capacitance ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Item	Symbol	min	typ	max	Unit	Conditions
Input Pin Capacitance	C_{in}	–	–	5	pF	$V_{in} = 0\text{ V}$
I/O Pin Capacitance	$C_{I/O}$	–	–	7	pF	$V_{I/O} = 0\text{ V}$

Note) These parameters are not 100% tested.

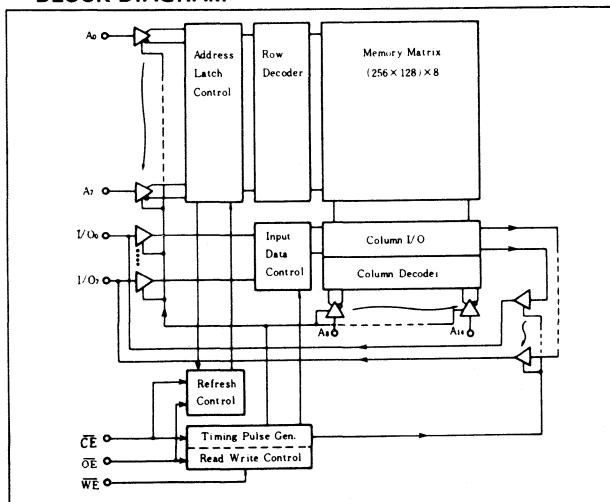
HM65256BP Series, HM65256BSP Series, HM65256BFP Series

32768-word X 8-bit High Speed Pseudo Static RAM

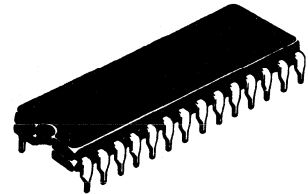
■ FEATURES

- Single 5V ($\pm 10\%$)
- High Speed
 - Access Time
 - \overline{CE} Access Time 120/150/200ns
 - Address Access Time 60/75/100ns
 - (in Static Column Mode)
 - Cycle Time
 - Random Read/Write Cycle Time 190/235/310ns
 - Static Column Mode Cycle Time 65/80/105ns
- Low Power
 - 175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
 - Address Refresh
 - Automatic Refresh
 - Self Refresh

■ BLOCK DIAGRAM

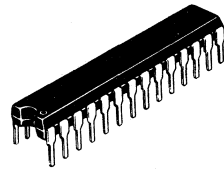


HM65256BP Series



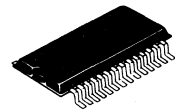
(DP-28)

HM65256BSP Series



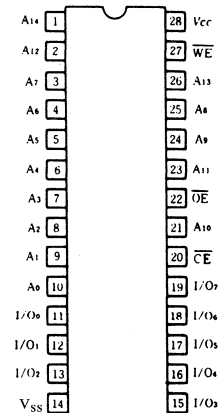
(DP-28N)

HM65256BFP Series



(FP-28D)

■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{WE}	I/O Pin	mode
L	L	H	Low Z	Read
L	x	L	High Z	Write
L	H	H	High Z	–
H	L	x	High Z	Refresh
H	H	x	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	-1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-1.0	–	0.8	V

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O} = 0$ $t_{cyc} = \text{min.}$	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IH}$	–	1	2	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE} = V_{IH}$ $\overline{OE} = V_{IL}$	–	1	2	mA
Input Leakage Current	I_{L1}	$V_{CC} = 5.5V$ $V_{in} = V_{SS}$ to V_{CC}	-10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	-10	–	10	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1 \text{ mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1 \text{ mA}$	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0V$	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ Electrical Characteristics and Recommended AC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

● AC Test Conditions

Input Pulse Levels 2.4V, 0.4V

Input Rise and Fall Times 5ns

Timing Measurement Level 2.2V, 0.8V

Reference Level $V_{OH} = 2.0\text{V}$, $V_{OL} = 0.8\text{V}$

Output Load 1 TTL and 100pF

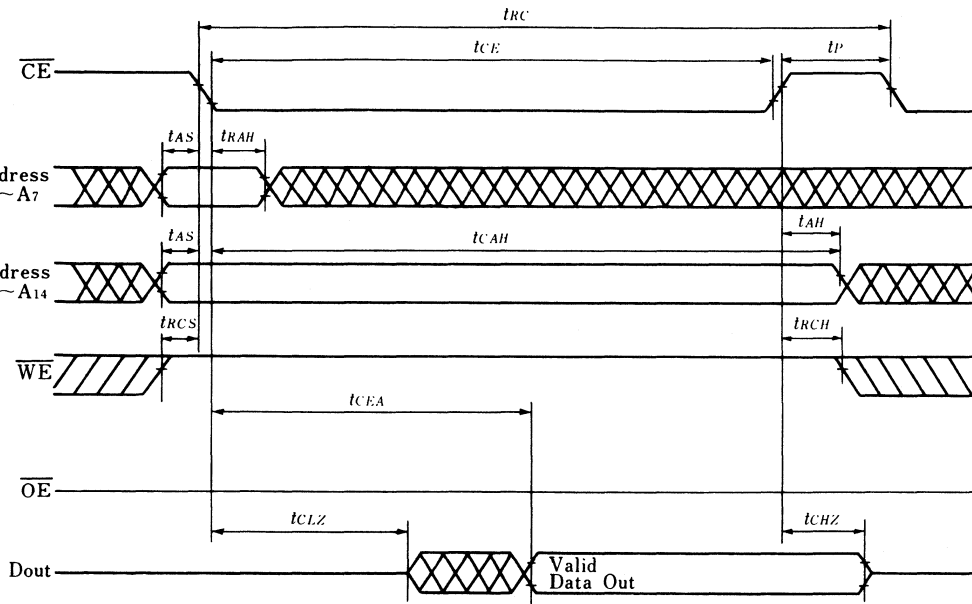
Item	Symbol	HM65256B-12		HM65256B-15		HM65256B-20		Unit
		min.	max.	min.	max.	min.	max.	
Random Read or Write Cycle Time	t_{RC}	190	—	235	—	310	—	ns
Static Column Mode Read or Write Cycle Time	t_{RSC}	65	—	80	—	105	—	ns
Chip Enable Access Time	t_{CEA}	—	120	—	150	—	200	ns
Address Access Time	t_{AA}	—	60	—	75	—	100	ns
Output Enable Access Time	t_{OEA}	—	50	—	60	—	75	ns
Chip Disable to Output in High Z	t_{CHZ}	—	25	—	30	—	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	—	35	—	40	—	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	—	25	—	30	—	35	ns
Chip Enable Pulse Width	t_{CE}	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	60	—	75	—	100	—	ns
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns
Row Address Hold Time	t_{RAH}	20	—	25	—	30	—	ns
Column Address Hold Time	t_{CAH}	120	—	150	—	200	—	ns
Column Address Hold Time from CE going High	t_{AH}	0	—	0	—	0	—	ns
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns
Output Enable Hold Time	t_{OHC}	0	—	0	—	0	—	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	—	0	—	0	—	ns
Output Hold Time from Column Address	t_{OH}	5	—	5	—	10	—	ns
Write Command Pulse Width	t_{WP}	25	—	30	—	35	—	ns
Chip Enable to End of Write	t_{CW}	120	—	150	—	200	—	ns
Column Address Set-up Time	t_{ASW}	0	—	0	—	0	—	ns
Column Address Hold Time after Write	t_{AHW}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	20	—	25	—	30	—	ns
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	5	—	5	—	0	—	ns
Write to Output in High Z	t_{WHZ}	—	25	—	30	—	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	60	—	75	—	100	—	ns
Refresh Precharge Time	t_{FP}	30	—	30	—	30	—	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	190	—	235	—	310	—	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	—	10000	—	10000	—	ns
Refresh Reset Time for Self Refresh	t_{FRS}	190	—	235	—	310	—	ns
Refresh Period	t_{REF}	—	4	—	4	—	4	ms

Notes:

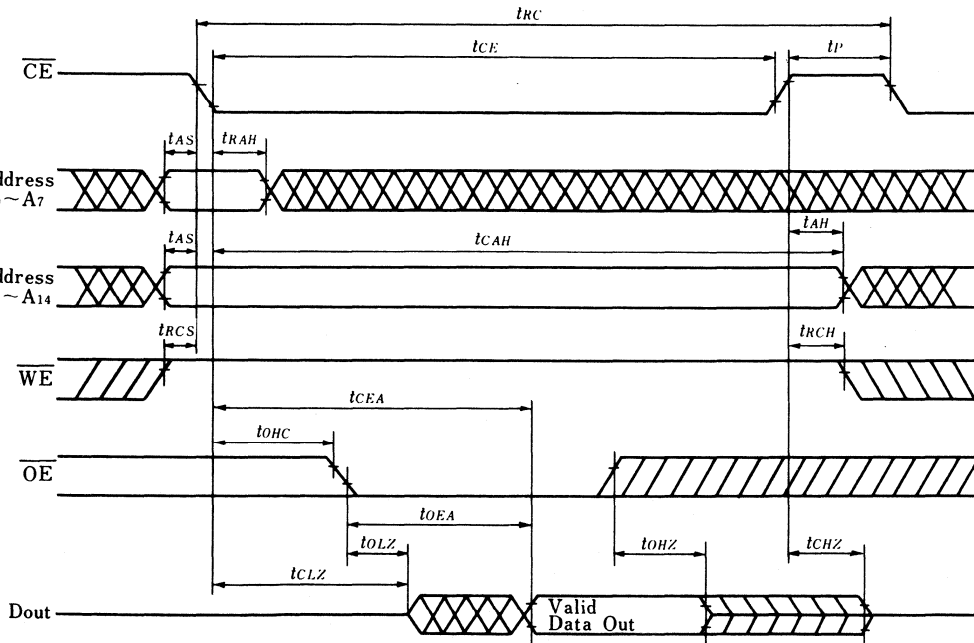
- (1) t_{CHZ} , t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit conditions.
- (2) t_{CLZ} , t_{OLZ} and t_{OW} are sampled under the condition of $t_T=5\text{ns}$, and not 100% tested.
- (3) A write occurs during the overlap of a low $\overline{\text{CE}}$ and low $\overline{\text{WE}}$.
- (4) If $\overline{\text{CE}}$ goes low simultaneously with $\overline{\text{WE}}$ going low or after $\overline{\text{WE}}$ going low, the outputs remain in high impedance state.
- (5) If input signals of opposite phase to the outputs are applied in write cycle, $\overline{\text{OE}}$ or $\overline{\text{WE}}$ must disable output buffers prior to applying data to the device and data inputs must be floating prior to $\overline{\text{OE}}$ or $\overline{\text{WE}}$ turning on output buffers.
- (6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- (7) An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

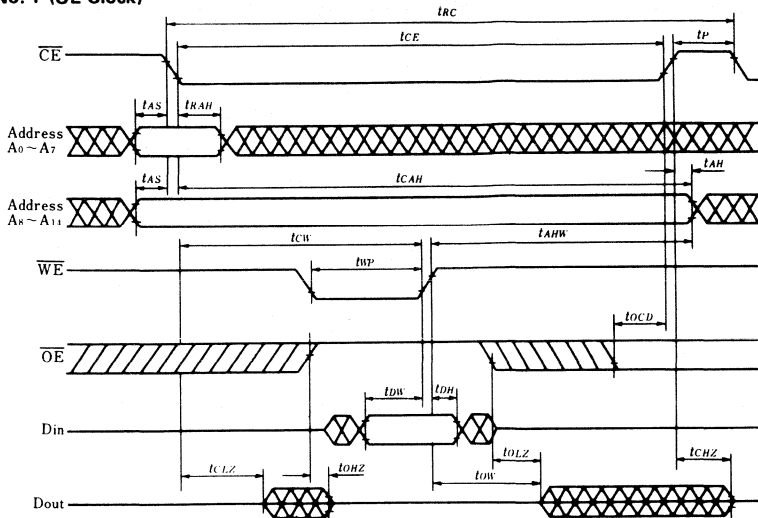
● Read Cycle No. 1 (\overline{CE} controlled)



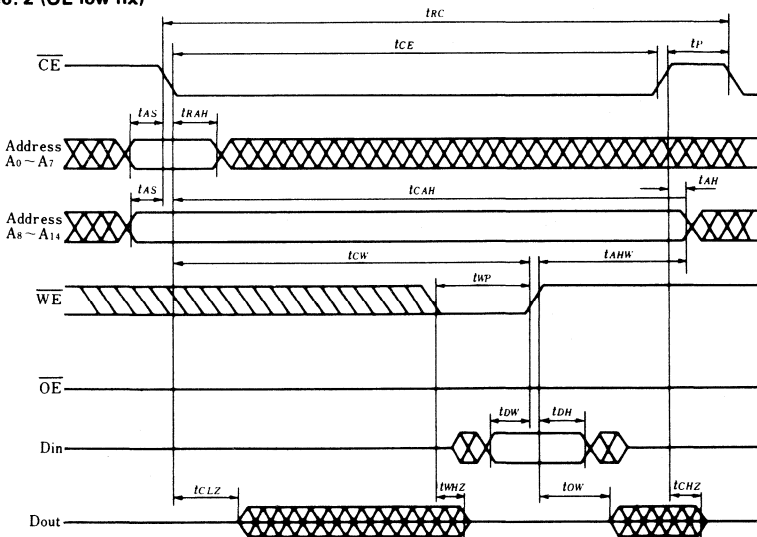
● Read Cycle No. 2 (\overline{OE} controlled)



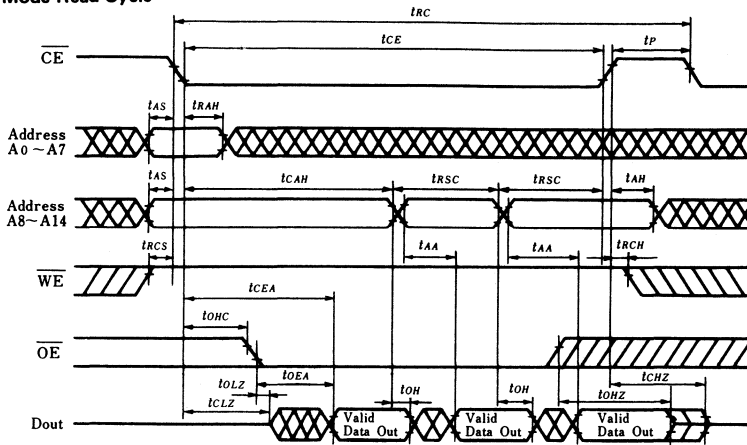
● Write Cycle No. 1 (\overline{OE} Clock)



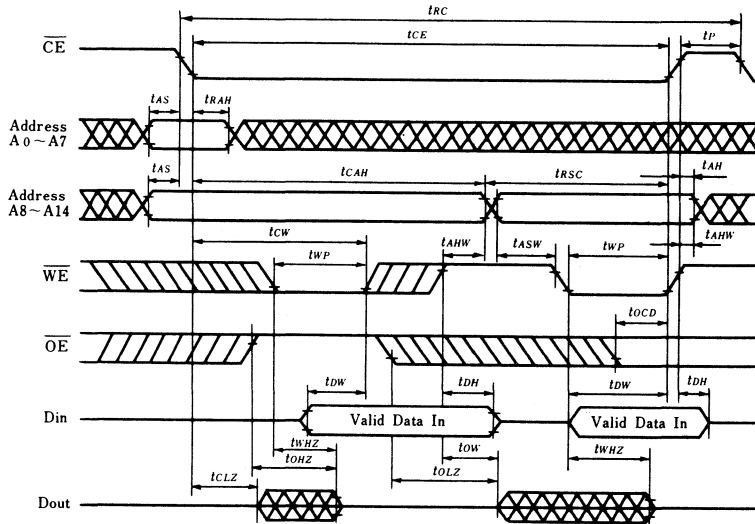
● Write Cycle No. 2 (\overline{OE} low fix)



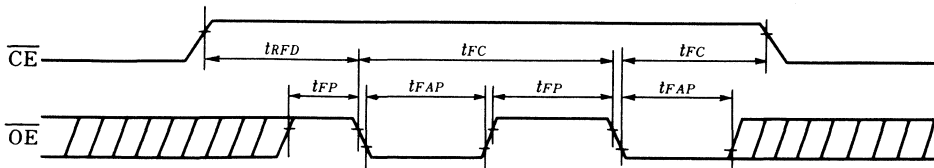
● Static Column Mode Read Cycle



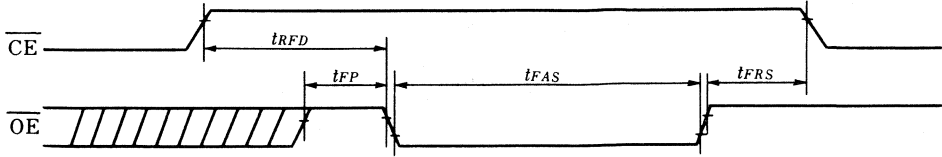
● Static Column Mode Write Cycle



● Automatic Refresh Cycle



• Self Refresh Cycle



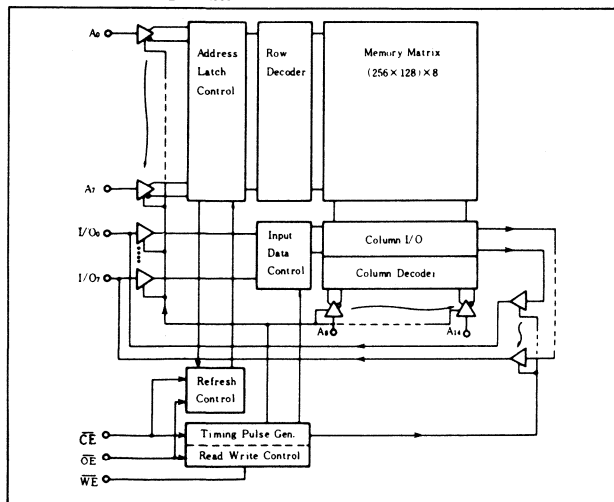
HM65256BLP Series, HM65256BLSP Series, HM65256BLFP Series

32768-word X 8-bit High Speed Pseudo Static RAM

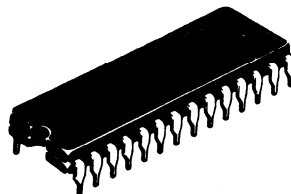
■ FEATURES

- Single 5V ($\pm 10\%$)
- High Speed
Access Time
 \overline{CE} Access Time 120/150/200ns
 Address Access Time 60/75/100ns
 (in Static Column Mode)
 Cycle Time
 Random Read/Write Cycle Time 190/235/310ns
 Static Column Mode Cycle Time 65/80/105ns
- Low Power
175mW typ. Active.
- All inputs and outputs TTL compatible
- Static Column Mode Capability
- Non Multiplexed Address
- 256 Refresh Cycles (4ms)
- Refresh Functions
Address Refresh
Automatic Refresh
Self Refresh

■ BLOCK DIAGRAM

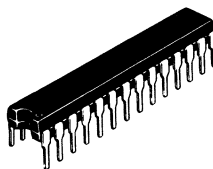


HM65256BLP Series



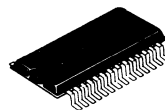
(DP-28)

HM65256BLSP Series



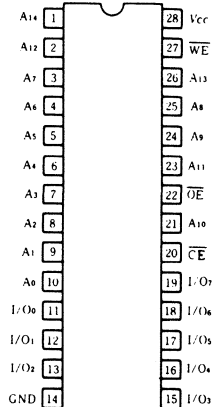
(DP-28N)

HM65256BLFP Series



(FP-28D)

■ PIN ARRANGEMENT



(Top View)

■ TRUTH TABLE

\overline{CE}	\overline{OE}	\overline{WE}	I/O Pin	mode
L	L	H	Low Z	Read
L	x	L	High Z	Write
L	H	H	High Z	–
H	L	x	High Z	Refresh
H	H	x	High Z	Standby

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Terminal Voltage with Respect to V_{SS}	V_T	-1.0 to +7.0	V
Power Dissipation	P_T	1.0	W
Operating Temperature	T_{opr}	0 to +70	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature Under Bias	T_{bias}	-10 to +85	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Item	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
	V_{SS}	0	0	0	V
Input Voltage	V_{IH}	2.2	–	6.0	V
	V_{IL}	-1.0	–	0.8	V

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Operating Power Supply Current	I_{CC1}	$I_{I/O}=0$ $t_{cyc} = \text{min.}$	–	35	65	mA
Standby Power Supply Current	I_{SB1}	$\overline{CE} = V_{IH}, \overline{OE} = V_{IH}$	–	1	2	mA
	I_{SB2}	$\overline{CE} \geq V_{CC} - 0.2V, \overline{OE} \geq V_{CC} - 0.2V$	–	0.05	0.1	mA
Operating Power Supply Current in Self Refresh Mode	I_{CC2}	$\overline{CE} = V_{IH}, \overline{OE} = V_{IL}$	–	0.6	1	mA
	I_{CC3}	$\overline{CE} \geq V_{CC} - 0.2V, \overline{OE} \leq 0.2V$	–	50	100	μA
Input Leakage Current	I_{L1}	$V_{CC} = 5.5V$ $V_{in} = V_{SS}$ to V_{CC}	-10	–	10	μA
Output Leakage Current	I_{LO}	$\overline{OE} = V_{IH}$ $V_{I/O} = V_{SS}$ to V_{CC}	-10	–	10	μA
Output Voltage	V_{OL}	$I_{OL} = 2.1 \text{ mA}$	–	–	0.4	V
	V_{OH}	$I_{OH} = -1 \text{ mA}$	2.4	–	–	V

■ CAPACITANCE

Item	Symbol	Test Conditions	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0V$	–	5	pF
Input/Output Capacitance	$C_{I/O}$	$V_{I/O} = 0V$	–	7	pF

Note) This Parameter is sampled and not 100% tested.

■ Electrical Characteristics and Recommended AC Operating Conditions ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

● AC Test Conditions

- Input Pulse Levels 2.4V, 0.4V
- Input Rise and Fall Times 5ns
- Timing Measurement Level 2.2V, 0.8V
- Reference Level $V_{OH} = 2.0\text{V}$, $V_{OL} = 0.8\text{V}$
- Output Load 1 TTL and 100pF

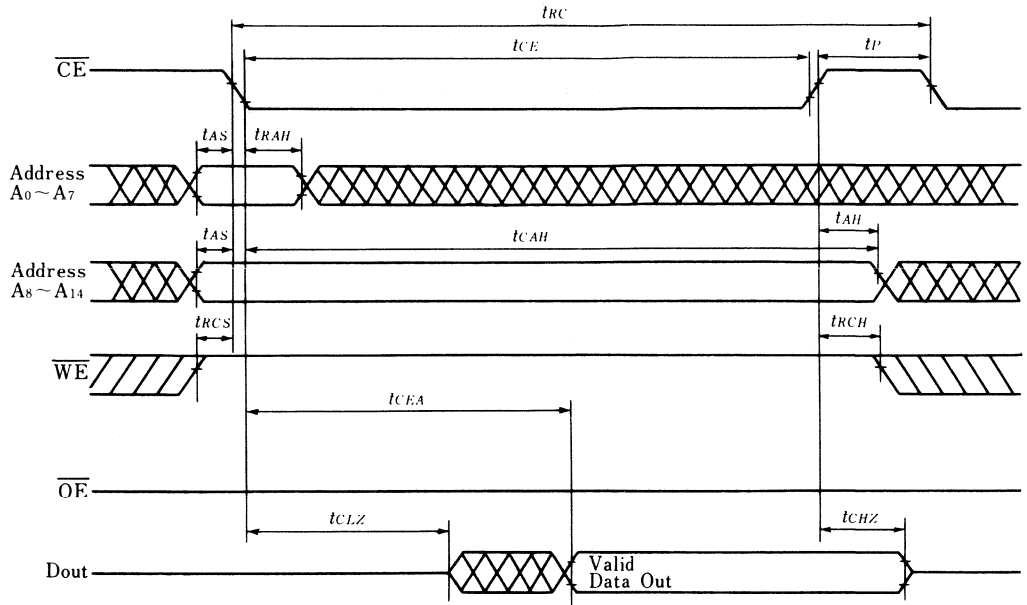
Item	Symbol	HM65256BL-12		HM65256BL-15		HM65256BL-20		Unit
		min.	max.	min.	max.	min.	max.	
Radom Read or Write Cycle Time	t_{RC}	190	—	235	—	310	—	ns
Static Column Mode Read or Write Cycle Time	t_{RSC}	65	—	80	—	105	—	ns
Chip Enable Access Time	t_{CEA}	—	120	—	150	—	200	ns
Address Access Time	t_{AA}	—	60	—	75	—	100	ns
Output Enable Access Time	t_{OEA}	—	50	—	60	—	75	ns
Chip Disable to Output in High Z	t_{CHZ}	—	25	—	30	—	35	ns
Chip Enable to Output in Low Z	t_{CLZ}	30	—	35	—	40	—	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	10	—	10	—	ns
Output Disable to Output in High Z	t_{OHZ}	—	25	—	30	—	35	ns
Chip Enable Pulse Width	t_{CE}	120n	4m	150n	4m	200n	4m	s
Chip Enable Precharge Time	t_P	60	—	75	—	100	—	ns
Address Set-up Time	t_{AS}	0	—	0	—	0	—	ns
Row Address Hold Time	t_{RAH}	20	—	25	—	30	—	ns
Column Address Hold Time	t_{CAH}	120	—	150	—	200	—	ns
Column Address Hold Time from CE going High	t_{AH}	0	—	0	—	0	—	.is
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns
Output Enable Hold Time	t_{OHC}	0	—	0	—	0	—	ns
Output Enable to Chip Enable Delay Time	t_{OCD}	0	—	0	—	0	—	ns
Output Hold Time from Column Address	t_{OH}	5	—	5	—	10	—	ns
Write Command Pulse Width	t_{WP}	25	—	30	—	35	—	ns
Chip Enable to End of Write	t_{CW}	120	—	150	—	200	—	ns
Column Address Set-up Time	t_{ASW}	0	—	0	—	0	—	ns
Column Address Hold Time after Write	t_{AHW}	0	—	0	—	0	—	ns
Data Valid to End of Write	t_{DW}	20	—	25	—	30	—	ns
Data In Hold Time for Write	t_{DH}	0	—	0	—	0	—	ns
Output Active from End of Write	t_{OW}	5	—	5	—	0	—	ns
Write to Output in High Z	t_{WHZ}	—	25	—	30	—	35	ns
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns
Refresh Command Delay Time	t_{RFD}	60	—	75	—	100	—	ns
Refresh Precharge Time	t_{FP}	30	—	30	—	30	—	ns
Refresh Command Pulse Width for Automatic Refresh	t_{FAP}	80	10000	80	10000	80	10000	ns
Automatic Refresh Cycle Time	t_{FC}	190	—	235	—	310	—	ns
Refresh Command Pulse Width for Self Refresh	t_{FAS}	10000	—	10000	—	10000	—	ns
Refresh Reset Time for Self Refresh	t_{FRS}	190	—	235	—	310	—	ns
Refresh Period	t_{REF}	—	4	—	4	—	4	ms

Notes:

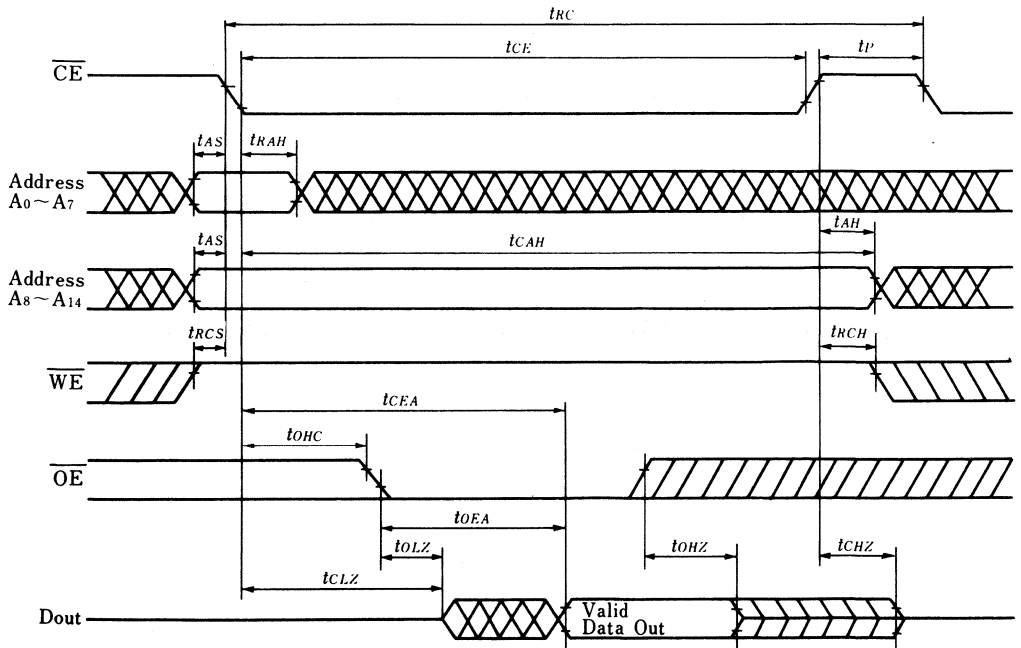
- (1) t_{CHZ} , t_{OHZ} and t_{WHZ} define the time at which the output achieves the open circuit conditions.
- (2) t_{CLZ} , t_{OLZ} and t_{OW} are sampled under the condition of $t_T=5\text{ns}$, and not 100% tested.
- (3) A write occurs during the overlap of a low CE and low WE.
- (4) If CE goes low simultaneously with WE going low or after WE going low, the outputs remain in high impedance state.
- (5) If input signals of opposite phase to the outputs are applied in write cycle, OE or WE must disable output buffers prior to applying data to the device and data inputs must be floating prior to OE or WE turning on output buffers.
- (6) V_{IH} (min) and V_{IL} (max) are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- (7) An initial pause of 100μs is required after power-up followed by a minimum of 8 initialization cycles.

■ TIMING WAVEFORMS

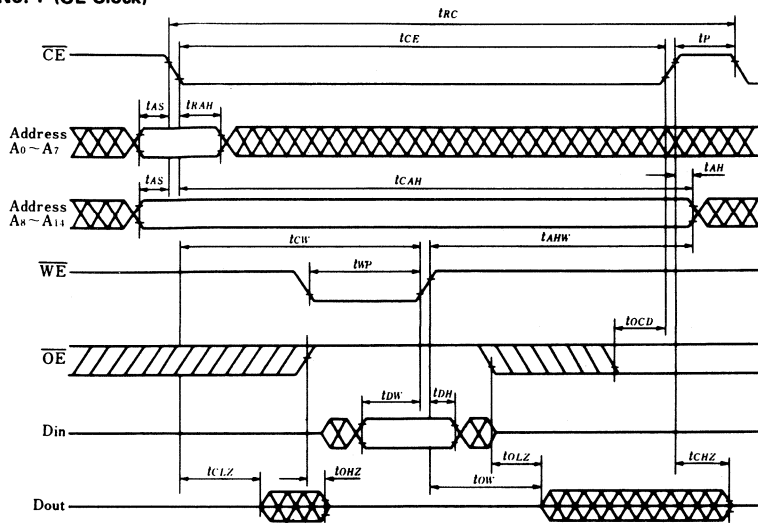
● Read Cycle No. 1 ($\overline{\text{CE}}$ controlled)



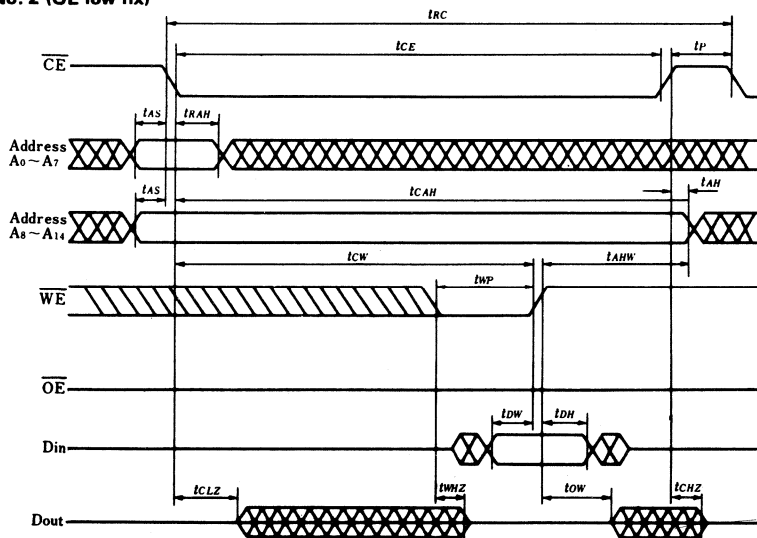
● Read Cycle No. 2 ($\overline{\text{OE}}$ controlled)



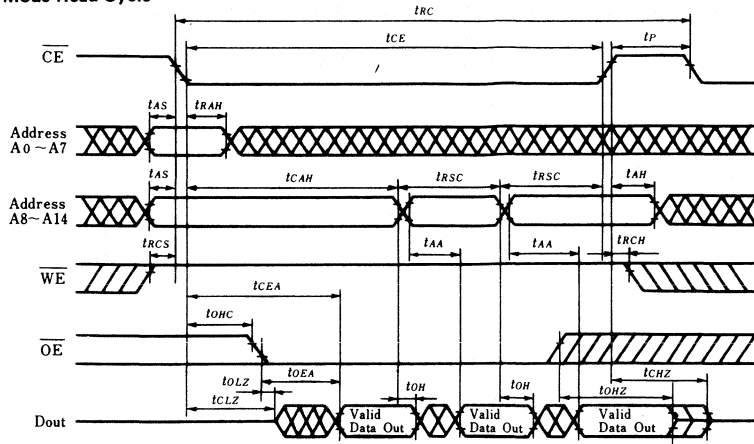
● Write Cycle No. 1 (\overline{OE} Clock)



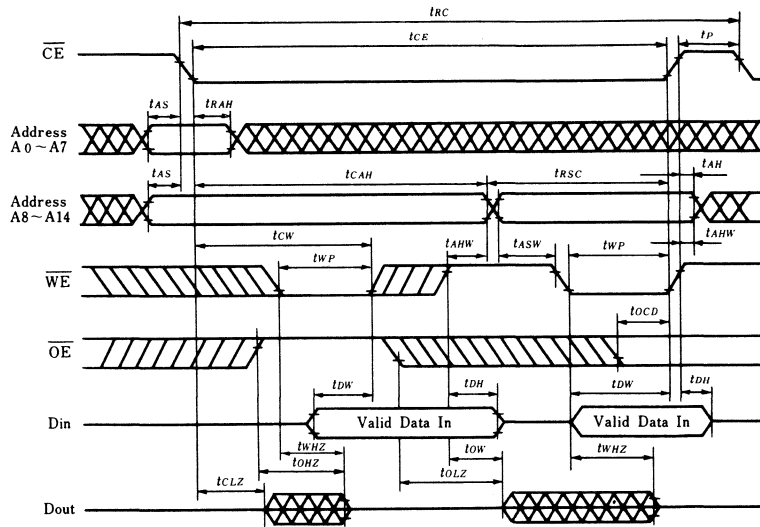
● Write Cycle No. 2 (\overline{OE} low fix)



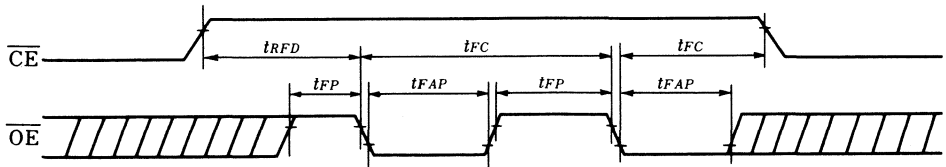
● Static Column Mode Read Cycle



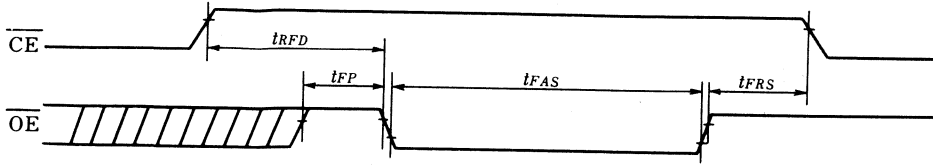
● Static Column Mode Write Cycle



● Automatic Refresh Cycle



• Self Refresh Cycle



MOS DYNAMIC RAM

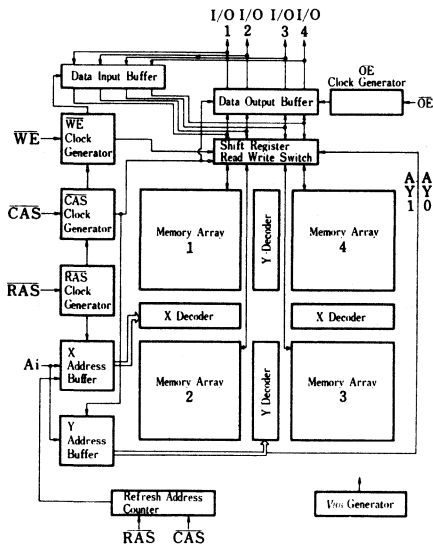
HM50464P Series, HM50464CP Series

65536-word x 4-bit Dynamic Random Access Memory

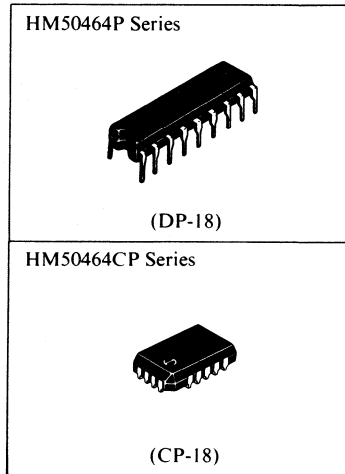
■ FEATURES

- Page mode capability
- Single 5V ($\pm 10\%$)
- On chip substrate bias generator
- Low power: 350 mW active, 20 mW standby
- High speed: Access Time 120ns/150ns/200ns
- Output data controlled by CAS or OE
- TTL compatible
- 256 refresh cycles 4 ms
- 3 variations of refresh RAS only refresh
CAS before RAS refresh
Hidden refresh

■ BLOCK DIAGRAM

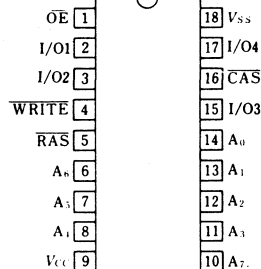


$A_0 \sim A_7$	Address Inputs
CAS	Column Address Strobe
I/O1 ~ I/O4	Data In/Data Out
OE	Output Enable
RAS	Row Address Strobe
WRITE	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$ (Row)	Refresh Address Inputs



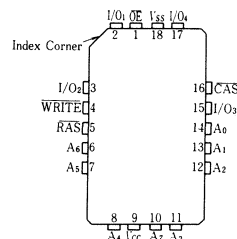
■ PIN ARRANGEMENT

● HM50464P Series



(Top View)

● HM50464CP Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	-1 to +7	V
Operating Temperature (Ambient)	T_{opr}	0 to +70	°C
Storage Temperature (Ambient)	T_{stg}	-55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	I_{out}	50	mA

■ RECOMMENDED DC OPERATING CONDITION ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

Note) All voltage referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	HM50464P/CP-12		HM50464P/CP-15		HM50464P/CP-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current ($t_{RC} = \text{min.}$)	I_{CC1}	-	83	-	70	-	55	mA	1
Standby Current ($\overline{\text{RAS}} = V_{IH}$, Dout = Disable)	I_{CC2}	-	4.5	-	4.5	-	4.5	mA	
Refresh Current ($\overline{\text{RAS}}$ only refresh, $t_{RC} = \text{min.}$)	I_{CC3}	-	62	-	53	-	42	mA	
Standby Current ($\overline{\text{RAS}} = V_{IH}$, Dout = Enable)	I_{CC5}	-	10	-	10	-	10	mA	1
Refresh Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, $t_{RC} = \text{min.}$)	I_{CC6}	-	69	-	58	-	45	mA	1
Operating Current (Page mode, $t_{PC} = \text{min.}$)	I_{CC7}	-	57	-	48	-	37	mA	1
Input Leakage Current ($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output Leakage Current ($0 < V_{out} < 7V$, Dout = Disable)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output High Voltage ($I_{out} = -5 \text{ mA}$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage ($I_{out} = 4.2 \text{ mA}$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^\circ\text{C}$)

Parameter		Symbol	typ.	max.	Unit	Note
Input Capacitance	Address	C_{I1}	-	5	pF	1
	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C_{I2}	-	10	pF	1
Output Capacitance	Data In/Data Out	$C_{I/O}$	-	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	HM50464P/CP-12		HM50464P/CP-15		HM50464P/CP-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	-	120	-	150	-	200	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	-	60	-	75	-	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{\text{CAS}}$	t_{OFF1}	-	30	-	40	-	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	-	260	-	330	-	ns	
RAS Precharge Time	t_{RP}	90	-	100	-	120	-	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
RAS Hold Time	t_{RSH}	60	-	75	-	100	-	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	-	150	-	200	-	ns	
$\overline{\text{CAS}}$ to RAS Precharge Time	t_{CRP}	10	-	10	-	10	-	ns	
Row Address Set-up Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	15	-	15	-	20	-	ns	

(to be continued)

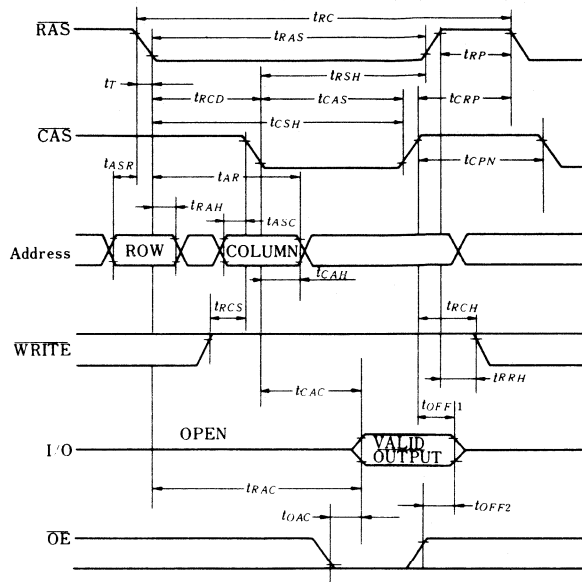
Parameter	Symbol	HM50464P/CP-12		HM50464P/CP-15		HM50464P/CP-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to RAS	t_{AR}	80	—	100	—	130	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to CAS Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time referenced to RAS	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
Read-Write Cycle Time	t_{RWC}	305	—	360	—	450	—	ns	
CAS to \overline{WE} Delay Time	t_{CWD}	100	—	125	—	160	—	ns	8
RAS to \overline{WE} Delay Time	t_{RWD}	160	—	200	—	260	—	ns	8
CAS Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
CAS Set-up Time (CAS before RAS refresh)	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS refresh)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to CAS Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Access Time from \overline{OE}	t_{OAC}	—	30	—	35	—	45	ns	
Output Buffer Turn-off Delay referenced to \overline{OE}	t_{OFF2}	—	30	—	40	—	50	ns	
\overline{OE} to Data-in Delay Time	t_{ODD}	30	—	40	—	50	—	ns	
\overline{OE} Hold Time referenced to WRITE	t_{OEH}	25	—	30	—	40	—	ns	
Page Mode Cycle Time	t_{PC}	120	—	145	—	190	—	ns	
CAS Precharge Time (for Page-mode Cycle Only)	t_{CP}	50	—	60	—	80	—	ns	
CAS Read-modify-write Cycle Time (Page-mode)	t_{PCM}	205	—	245	—	310	—	ns	

Notes)

- AC measurements assume $t_T = 5\text{ns}$.
- Assume that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
- $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met; $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
- An initial pause of 100 μs is required after power-up followed by a minimum of 8 initialization of cycles.
- Minimum of 8 CAS before RAS refresh is required before using internal refresh counter.
- In delayed write or read-modify-write cycles, \overline{OE} must disable output buffers prior to applying data to the device.

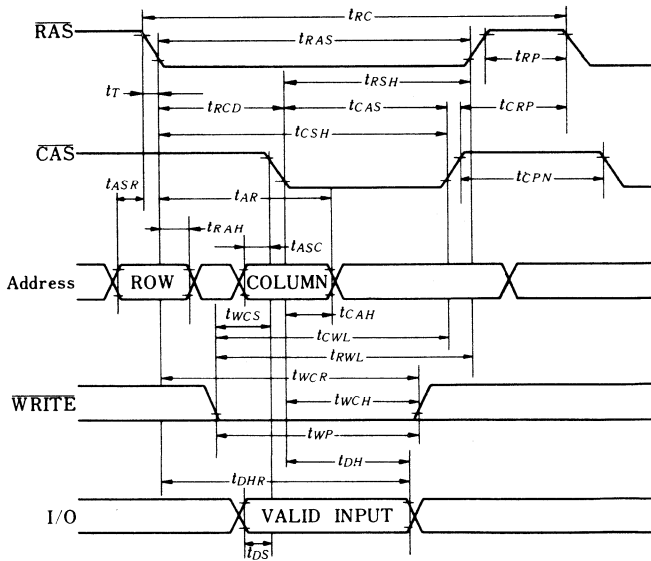
■ TIMING WAVEFORMS

● READ CYCLE



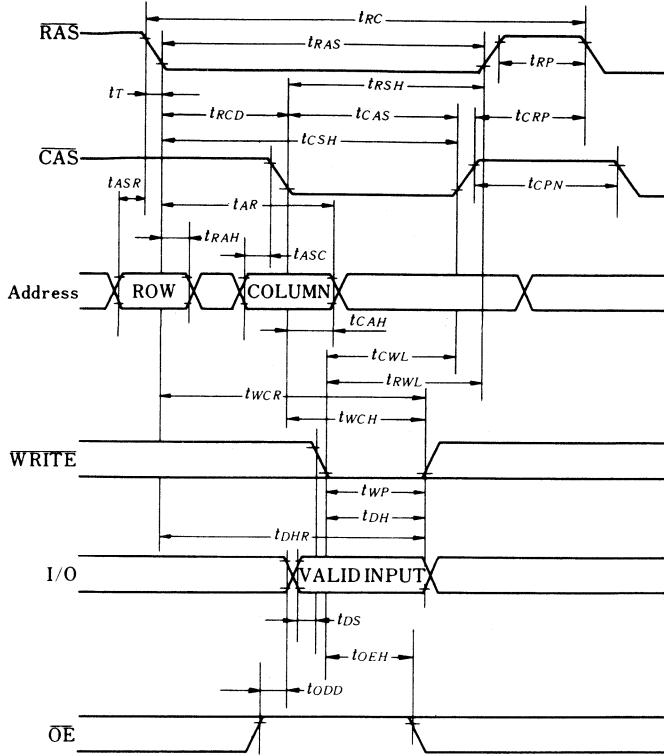
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
● EARLY WRITE CYCLE



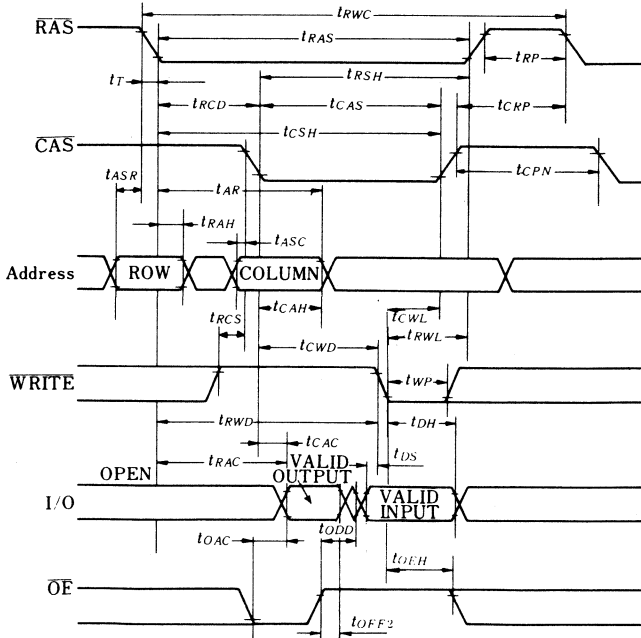
* \overline{OE} : Don't care
 * : Don't care


● DELAYED WRITE CYCLE



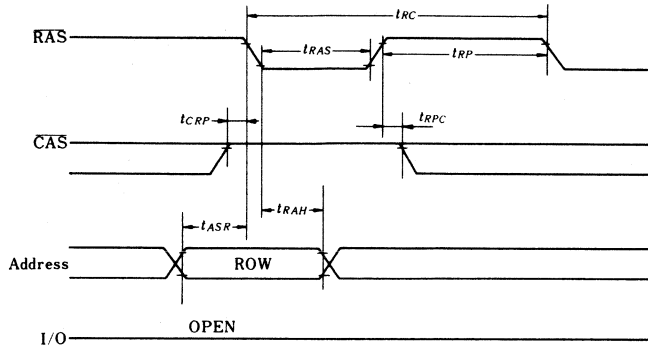
*  : Don't care

● READ MODIFY WRITE CYCLE



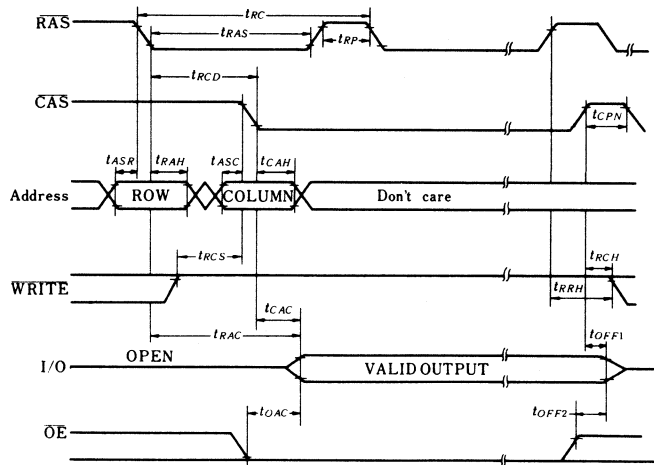
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● **RAS ONLY REFRESH CYCLE**



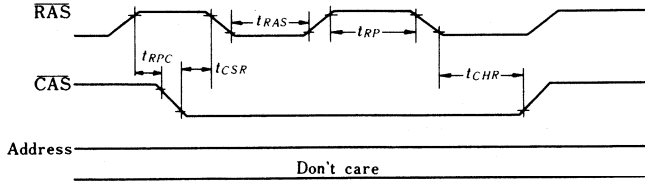
* $\overline{\text{OE}}, \overline{\text{WE}}$: Don't care
 * \square : Don't care

● **HIDDEN REFRESH CYCLE**

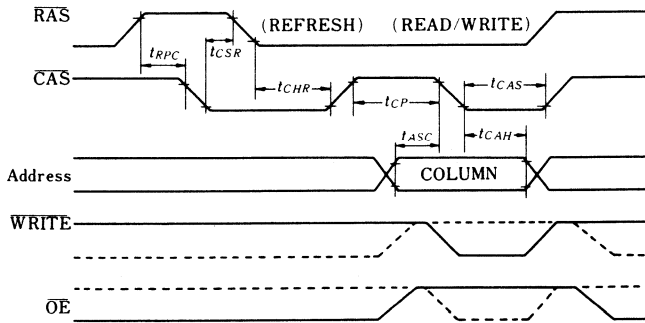


* \square : Don't care

• **CAS BEFORE RAS REFRESH CYCLE**

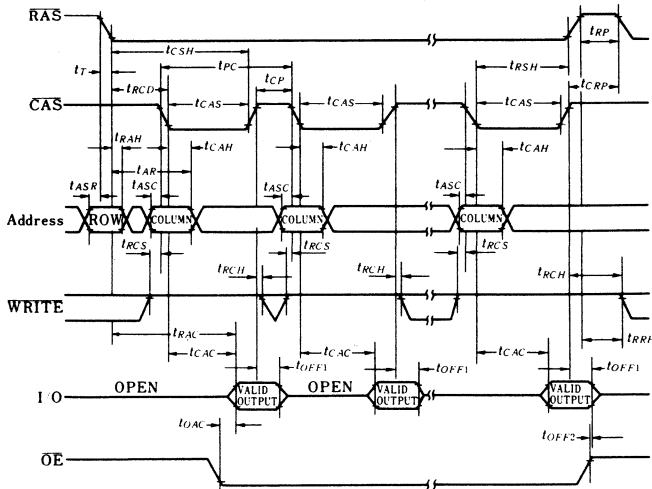


• **COUNTER TEST**



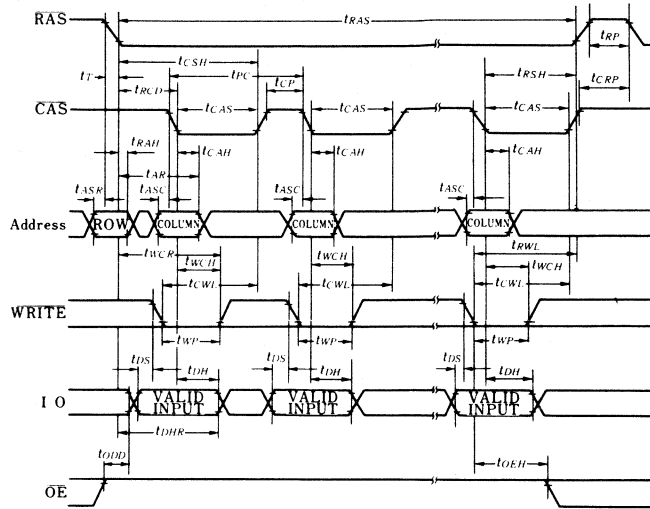
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
• **PAGE MODE READ CYCLE**



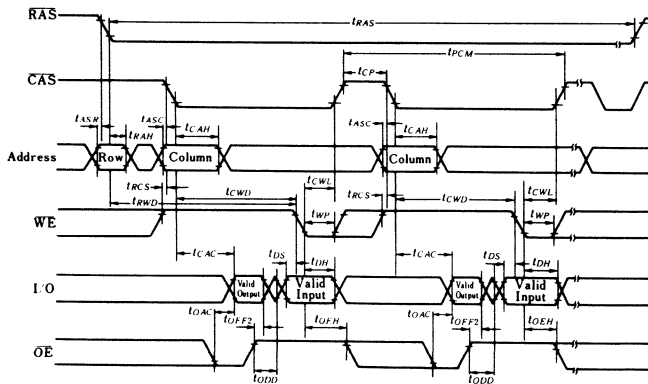
* : Don't care


● PAGE MODE WRITE CYCLE



*  : Don't care

● PAGE MODE READ MODIFY WRITE CYCLE



*  : Don't care

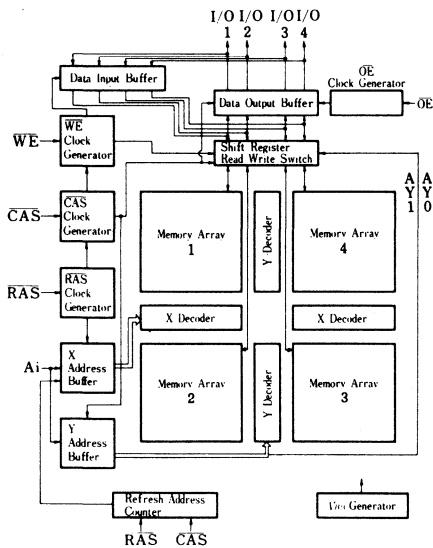
HM50465P Series, HM50465CP Series

65536-word x 4-bit Dynamic Random Access Memory

■ FEATURES

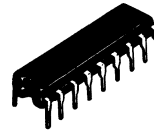
- Nibble mode capability
- Single 5V ($\pm 10\%$)
- On chip substrate bias generator
- Low power; 350 mW active, 20 mW standby
- High Speed: Access time 120 ns/150 ns/200 ns (max.)
- Output data controlled by CAS or OE
- TTL compatible
- 256 refresh cycles 4 ms
- 3 variations of refresh RAS only refresh
CAS before RAS refresh
Hidden refresh

■ BLOCK DIAGRAM



$A_0 \sim A_7$	Address Inputs
CAS	Column Address Strobe
I/O1 ~ I/O4	Data In/Data Out
OE	Output Enable
RAS	Row Address Strobe
WRITE	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$ (Row)	Refresh Address Inputs
A_0, A_1 (Column)	Nibble Address Inputs

HM50465P Series



(DP-18)

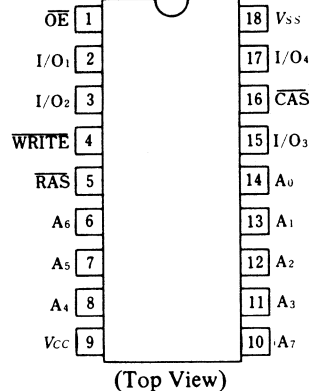
HM50465CP Series



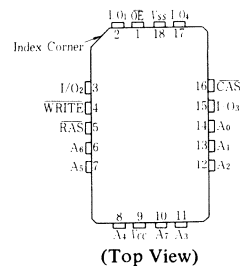
(CP-18)

■ PIN ARRANGEMENT

● HM50465P Series



● HM50465CP Series



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1 to +7	V
Supply Voltage relative to V_{SS}	V_{CC}	-1 to +7	V
Operating Temperature (Ambient)	T_{opr}	0 to +70	°C
Storage Temperature (Ambient)	T_{stg}	-55 to +125	°C
Power Dissipation	P_T	1.0	W
Short Circuit Output Current	I_{out}	50	mA

■ RECOMMENDED DC OPERATING CONDITION ($T_a = 0$ to +70°C)

Parameter	Symbol	min.	typ.	max.	unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-1.0	-	0.8	V

Note) All voltage referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to +70°C)

Parameter	Symbol	HM50465P/CP-12		HM50465P/CP-15		HM50465P/CP-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Operating Current ($t_{RC} = \text{min.}$)	I_{CC1}	-	83	-	70	-	55	mA	1
Standby Current ($\overline{\text{RAS}} = V_{IH}$, Dout = Disable)	I_{CC2}	-	4.5	-	4.5	-	4.5	mA	
Refresh Current (RAS only refresh, $t_{RC} = \text{min.}$)	I_{CC3}	-	62	-	53	-	42	mA	
Standby Current ($\overline{\text{RAS}} = V_{IH}$, Dout = Enable)	I_{CC5}	-	10	-	10	-	10	mA	1
Refresh Current (CAS before RAS refresh, $t_{RC} = \text{min.}$)	I_{CC6}	-	69	-	58	-	45	mA	1
Operating Current (Nibble mode, $t_{RC} = \text{min.}$)	I_{CC8}	-	57	-	48	-	37	mA	1
Input Leakage Current ($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output Leakage Current ($0 < V_{out} < 7V$, Dout = Disable)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output High Voltage ($I_{out} = -5 \text{ mA}$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output Low Voltage ($I_{out} = 4.2 \text{ mA}$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^\circ\text{C}$)

Parameter	Symbol	typ.	max.	Unit	Note	
						Input Capacitance
	$\overline{\text{RAS}}$, $\overline{\text{CAS}}$, $\overline{\text{WE}}$, $\overline{\text{OE}}$	C_{I2}	-	10	pF	1
Output Capacitance	Data In/Data Out	$C_{I/O}$	-	10	pF	1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{\text{CAS}} = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to +70°C)

Parameter	Symbol	HM50465P/CP-12		HM50465P/CP-15		HM50465P/CP-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	-	120	-	150	-	200	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	-	60	-	75	-	100	ns	3, 4
Output Buffer Turn-off Delay referenced to $\overline{\text{CAS}}$	t_{OFF1}	-	30	-	40	-	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	-	260	-	330	-	ns	
RAS Precharge Time	t_{RP}	90	-	100	-	120	-	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
RAS to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
RAS Hold Time	t_{RSH}	60	-	75	-	100	-	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	-	150	-	200	-	ns	
$\overline{\text{CAS}}$ to RAS Precharge Time	t_{CRP}	10	-	10	-	10	-	ns	
Row Address Set-up Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	15	-	15	-	20	-	ns	

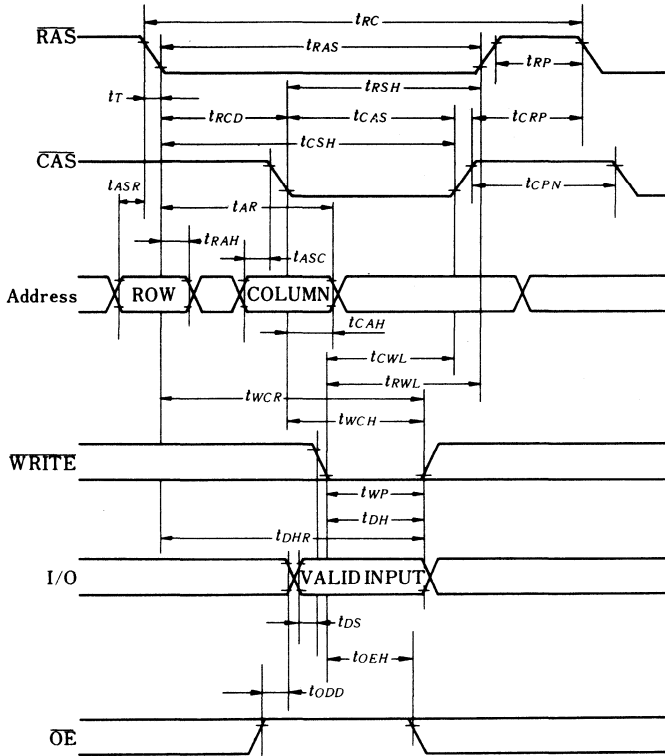
(to be continued)

Parameter	Symbol	HM50465P / CP-12		HM50465P / CP-15		HM50465P / CP-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to RAS	t_{AR}	80	—	100	—	130	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to \overline{CAS} Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	9
Data-in Hold Time referenced to RAS	t_{DHR}	100	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to \overline{CAS}	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
Read-Write Cycle Time	t_{RWC}	305	—	360	—	450	—	ns	
\overline{CAS} to \overline{WE} Delay	t_{CWD}	100	—	125	—	160	—	ns	8
RAS to \overline{WE} Delay	t_{RWD}	160	—	200	—	260	—	ns	8
\overline{CAS} Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
\overline{CAS} set-up Time (\overline{CAS} before RAS refresh)	t_{CSN}	10	—	10	—	10	—	ns	
\overline{CAS} Hold Time (\overline{CAS} before RAS refresh)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to \overline{CAS} Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Access Time from OE	t_{OAC}	—	30	—	35	—	45	ns	
Output Buffer Turn-off Delay referenced to \overline{OE}	t_{OFF2}	—	30	—	40	—	50	ns	
\overline{OE} to Data-in Delay Time	t_{ODD}	30	—	40	—	50	—	ns	
\overline{OE} Hold Time referenced to \overline{WRITE}	t_{OEH}	25	—	30	—	40	—	ns	
Nibble Mode Access Time	t_{NAC}	—	30	—	35	—	45	ns	
Nibble Mode RAS Cycle Time	t_{NRC}	410	—	480	—	610	—	ns	
Nibble Mode RAS Pulse Width	t_{NRA}	310	—	370	—	480	—	ns	
Nibble Mode Cycle Time	t_{NC}	60	—	70	—	90	—	ns	
Nibble Mode \overline{CAS} Precharge Time	t_{NCP}	20	—	25	—	35	—	ns	
Nibble Mode \overline{CAS} Pulse Width	t_{NCA}	30	—	35	—	45	—	ns	
Nibble Mode Write Command Hold Time	t_{NWC}	30	—	35	—	45	—	ns	
Nibble Mode RAS Hold Time	t_{NRSH}	40	—	45	—	55	—	ns	
Nibble Mode Read-Write Cycle Time	t_{NRWC}	135	—	160	—	200	—	ns	
Nibble Mode \overline{CAS} to \overline{WE} Delay	t_{NCWD}	70	—	85	—	105	—	ns	
Nibble Mode Write Command to \overline{CAS} Lead Time	t_{NCWL}	30	—	35	—	45	—	ns	
Nibble Mode Write Command Pulse Width	t_{NWP}	30	—	35	—	45	—	ns	

Notes)

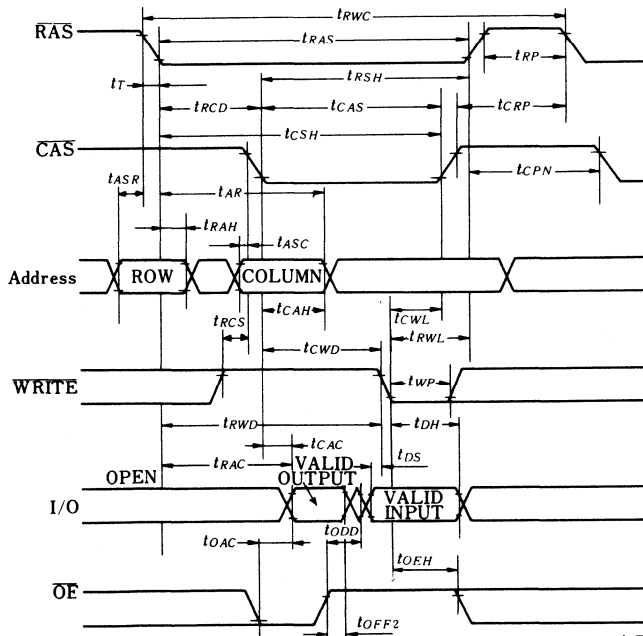
- AC measurements assume $t_T = 5$ ns.
- Assumes that $t_{RCD} \leq t_{RCD}(\max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100 pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\max)$.
- $t_{OFF}(\max)$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- $V_{IH}(\min)$ and $V_{IL}(\max)$ are reference level for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{RCD}(\max)$ limit insures that $t_{RAC}(\max)$ can be met, $t_{RCD}(\max)$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\max)$ limit, then access time is controlled exclusively by t_{CAC} .
- t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\min)$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\min)$ and $t_{RWD} \geq t_{RWD}(\min)$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to \overline{CAS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write on read-modify-write cycles.
- An initial pause of 100 μ s is required after power-up followed by a minimum of 8 initialization of cycles.
- Minimum of 8 \overline{CAS} before RAS refresh is required before using internal refresh counter.
- In delayed write or read-modify-write cycles, \overline{OE} must disable output buffers prior to applying data to the device.

● Delayed Write Cycle



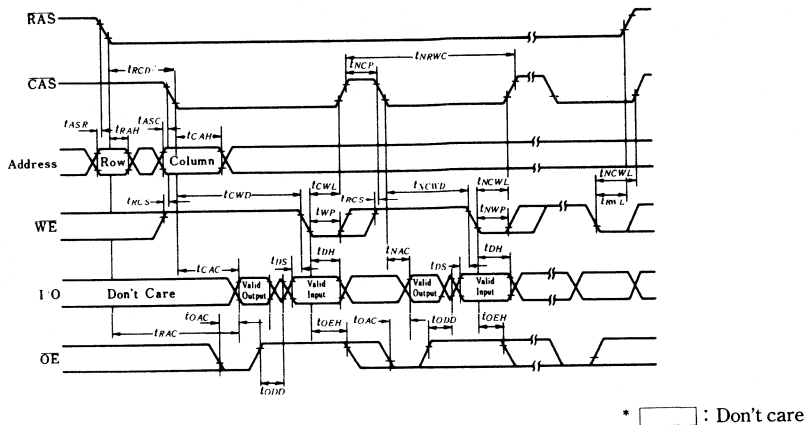
● Read Modify Write Cycle

* : Don't care



* : Don't care

• Nibble Mode Read Modify Write Cycle



HM50256P Series, HM50256CP Series, HM50256ZP Series

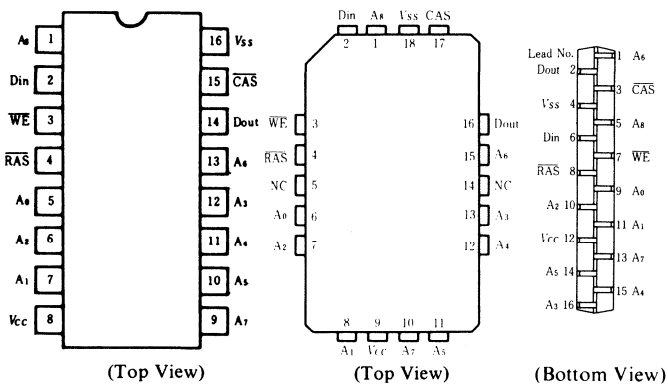
262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

- Industry Standard 16-Pin DIP, 18-Pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns(max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles ··· (4ms)
- 3 variations of refresh ··· $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh

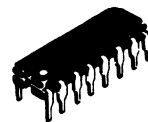
■ PIN ARRANGEMENT

- HM50256P Series
- HM50256CP Series
- HM50256ZP Series



$A_0 - A_7$	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
WE	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 - A_7$	Refresh Address Inputs

HM50256P Series



(DP-16B)

HM50256CP Series



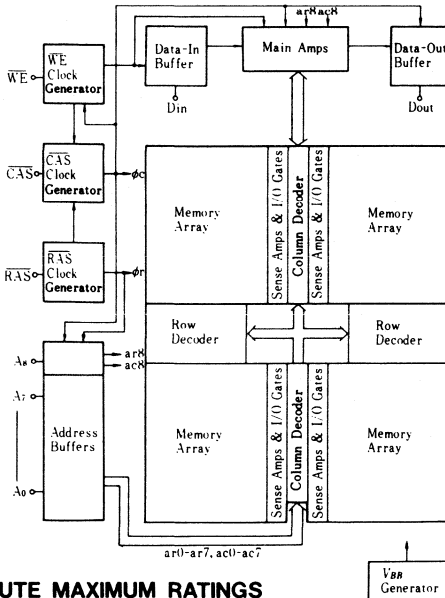
(CP-18)

HM50256ZP Series



(ZP-16)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} -1V to +7V
- Operating temperature, T_a (Ambient) 0°C to +70°C
- Storage temperature -55°C to +125°C
- Short circuit output current 50mA
- Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to +70°C, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current(RAS, CAS Cycling : $t_{RC} = \text{min}$)	I_{CC1}	—	83	—	70	—	55	mA	1
Standby Current(RAS = V_{IH} , Dout = High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current(RAS only Refresh, $t_{RC} = \text{min}$)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current(RAS = V_{IH} , Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current(CAS before RAS Refresh, $t_{RC} = \text{min}$)	I_{CC6}	—	69	—	58	—	45	mA	
Page Mode Supply Current (RAS = V_{IL} , CAS Cycling, $t_{PC} = \text{min}$)	I_{CC7}	—	57	—	48	—	37	mA	
Input leakage($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output leakage($0 < V_{out} < 7V$, Dout = Disable)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output levels High($I_{OH} = -5mA$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low($I_{OL} = 4.2mA$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. $I_{CC \text{ max}}$ is specified at the output open condition.

■ CAPACITANCE ($V_{CC}=5V \pm 10\%$, $T_a=25^\circ C$)

Parameter		Symbol	typ	max	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7		1, 2
Output Capacitance	Data-out	C_O	—	7		1, 2

- Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. CAS= V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a=0$ to $+70^\circ C$, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)^{1), 10), 11)}

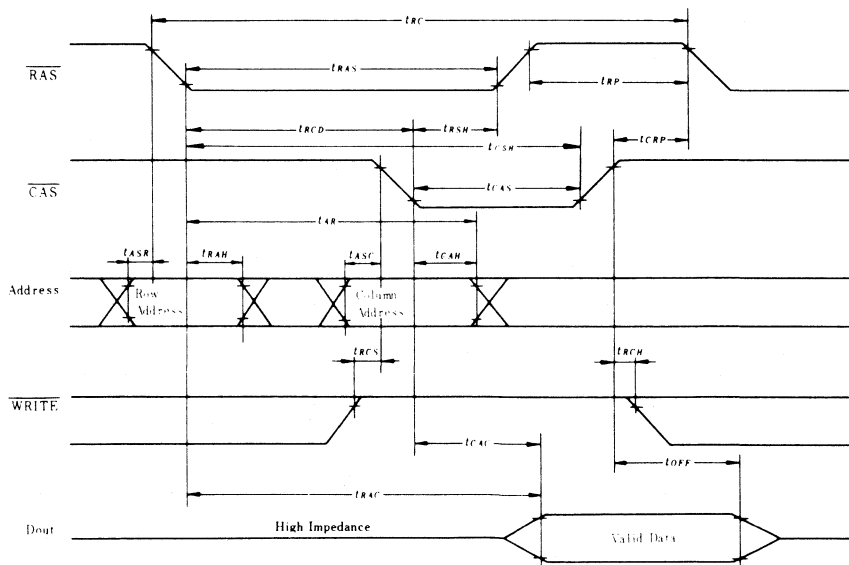
Parameter	Symbol	HM50256-12		HM50256-15		HM50256-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
RAS to \overline{CAS} Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
Access Time from RAS	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
RAS Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
RAS Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
\overline{CAS} Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
CAS Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to \overline{RAS}	t_{AR}	80	—	100	—	130	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to \overline{CAS}	t_{RCH}	0	—	0	—	0	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to \overline{RAS}	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to \overline{CAS} Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to \overline{RAS}	t_{DHR}	100	—	120	—	155	—	ns	
RAS to \overline{WE} Delay	t_{RWD}	120	—	150	—	200	—	ns	
\overline{CAS} to \overline{WE} Delay	t_{CWD}	60	—	75	—	100	—	ns	8
Page Mode Read or Write Cycle	t_{PC}	120	—	145	—	190	—	ns	
Page Mode Read Modify Write Cycle	t_{PCM}	165	—	195	—	250	—	ns	
\overline{CAS} Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns	
Read Command Hold Time referenced to \overline{RAS}	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
\overline{CAS} Set-up Time	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to \overline{CAS} Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

Notes

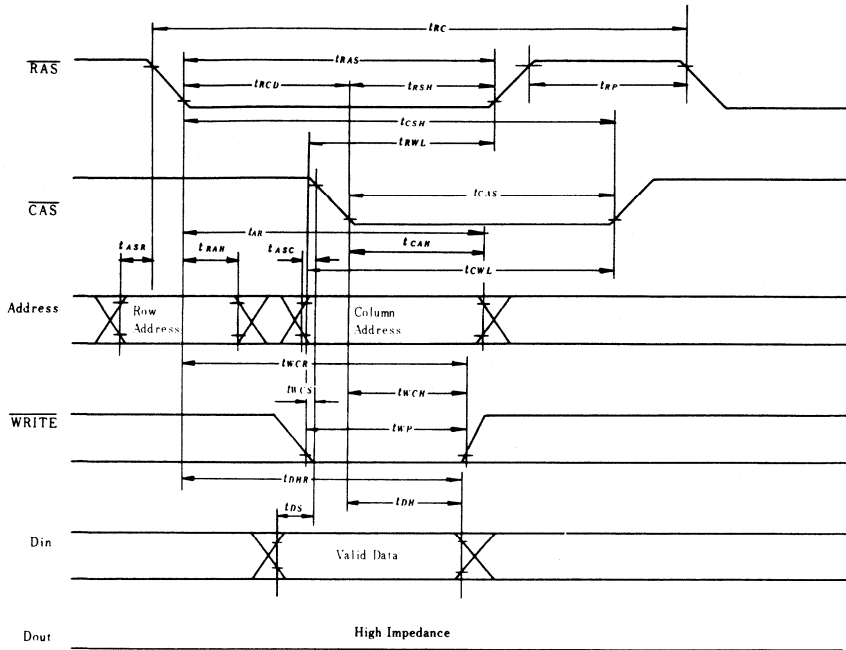
1. AC measurements assume $t_T = 5\text{ns}$.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .
8. t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up then execute at least 8 initialization cycles.
11. At least, 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles are required before using internal refresh counter.

■ TIMING WAVEFORMS

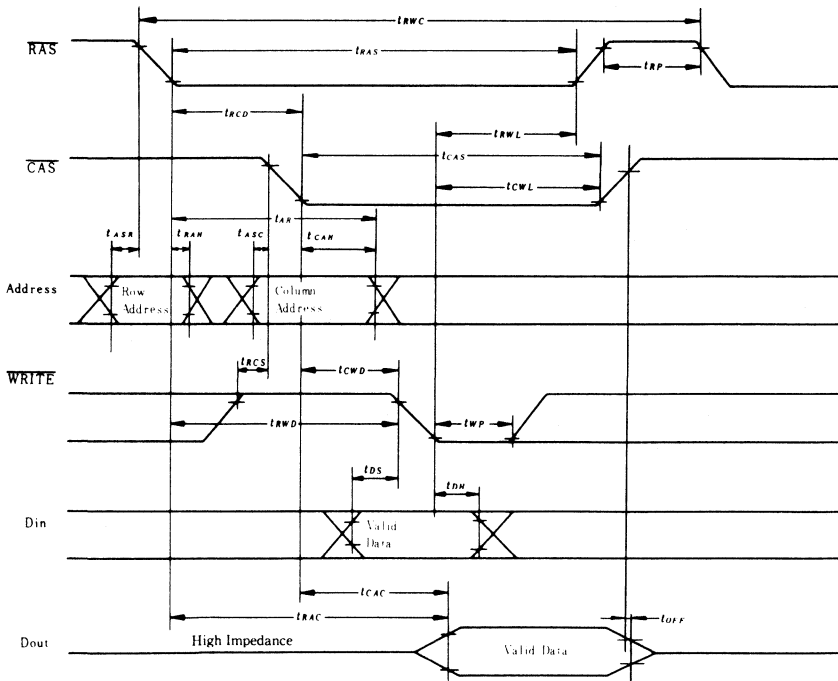
● READ CYCLE



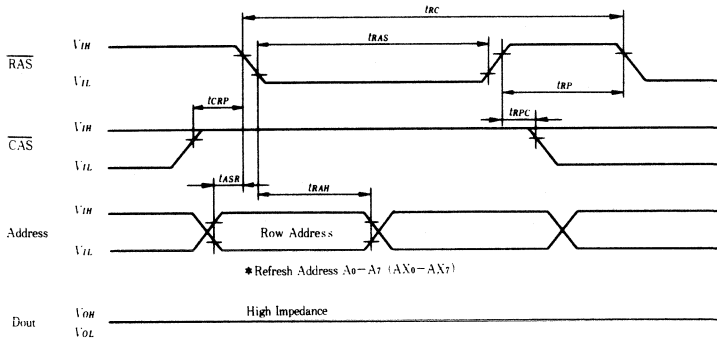
● WRITE CYCLE



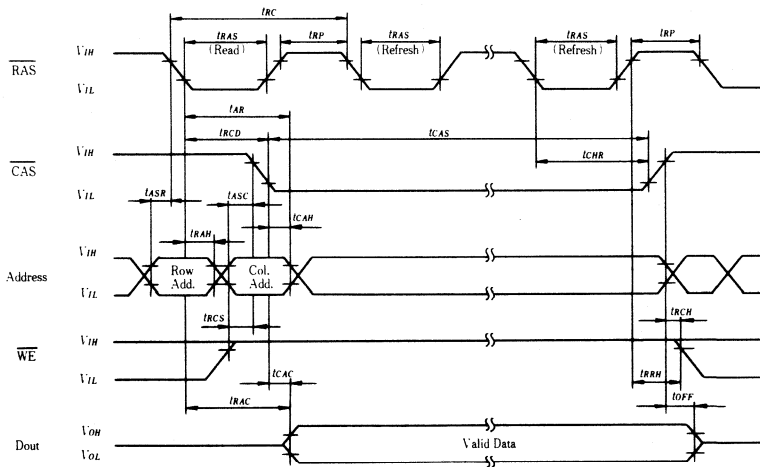
● READ MODIFY WRITE CYCLE



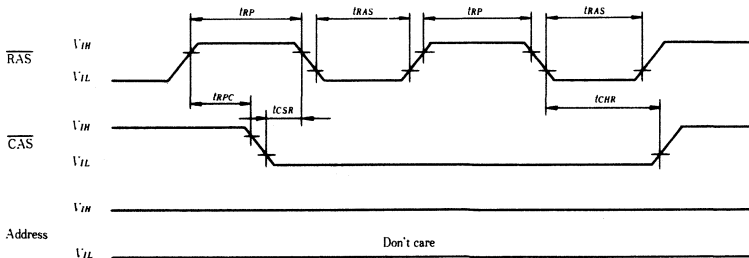
● RAS ONLY REFRESH CYCLE



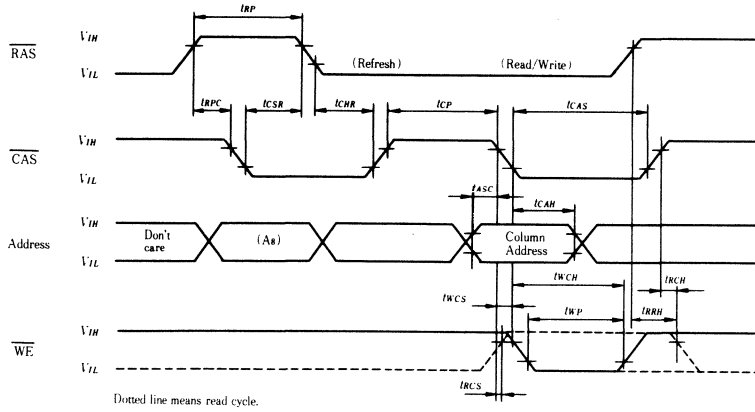
● HIDDEN REFRESH CYCLE



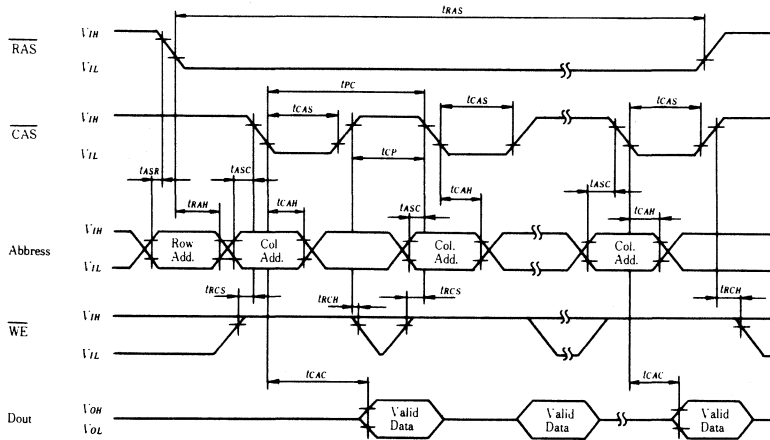
● CAS BEFORE RAS REFRESH CYCLE



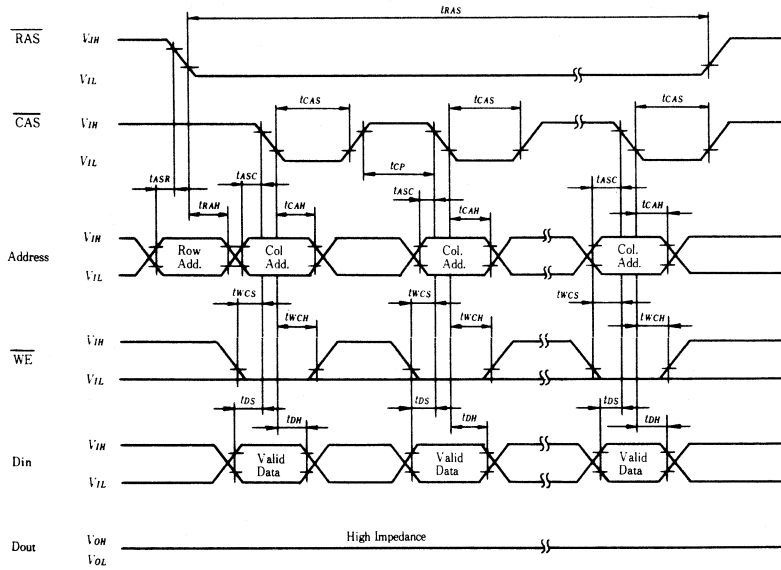
● COUNTER TEST



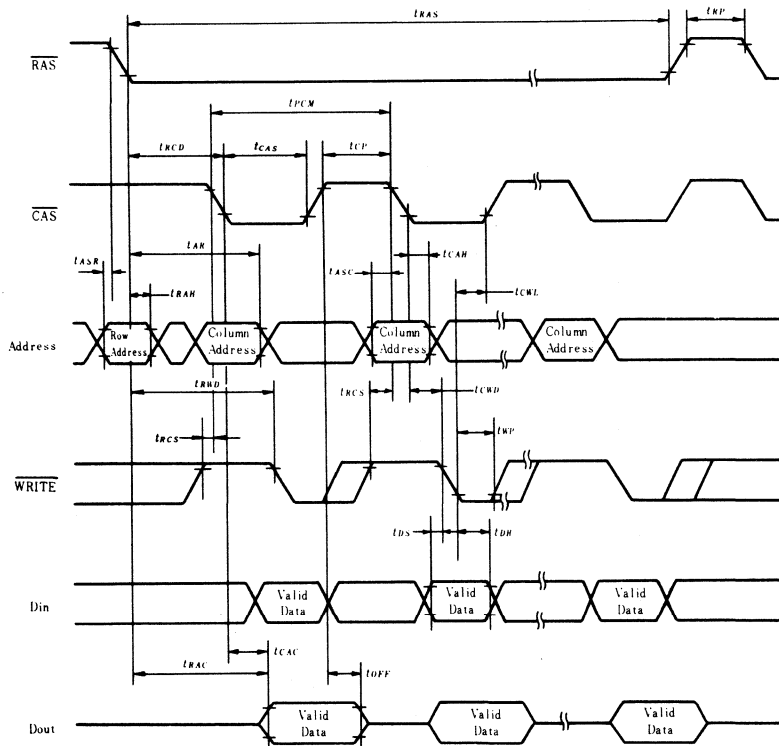
● PAGE MODE READ CYCLE



● PAGE MODE WRITE CYCLE



● PAGE MODE READ MODIFY WRITE CYCLE

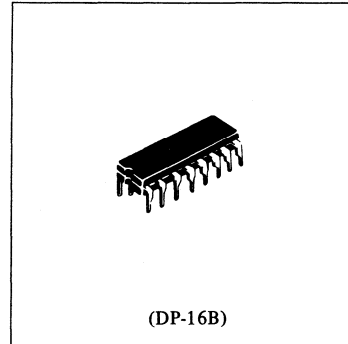


HM50256AP Series — Under Development

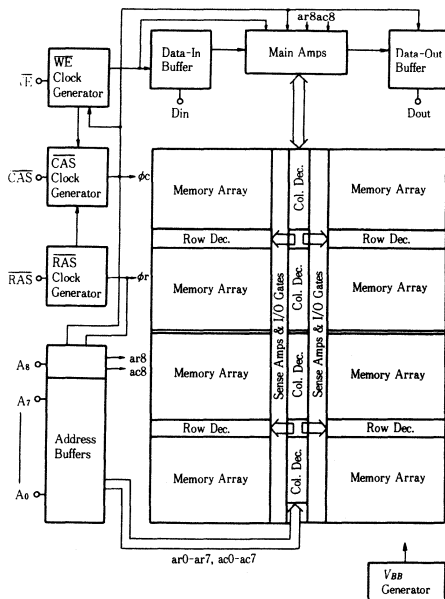
262144-word x 1-bit Dynamic Random Access Memory

■FEATURES

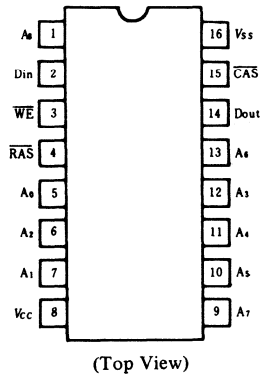
- Industry Standard 16-Pin DIP (plastic)
- Single 5V ($\pm 10\%$)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 100/ 120ns/150ns/ (max.)
- Common I/O capability using early write operation
- Page mode capability
- TTL compatible
- 256 refresh cycles . . . (4ms)
- 3 variation of refresh . . . RAM only refresh
CAS before RAS refresh
Hidden refresh



■BLOCK DIAGRAM



■PIN ARRANGEMENT



$A_0 \sim A_8$	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
Vcc	Power (+5V)
Vss	Ground
$A_0 \sim A_7$	Refresh Address Inputs

■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} -1V to +7V
 Operating temperature, T_a (Ambient) 0°C to +70°C
 Storage temperature -55°C to +125°C
 Short circuit output current 50mA
 Power dissipation 1W

■RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS} .

HM50257P Series, HM50257CP Series, HM50257ZP Series

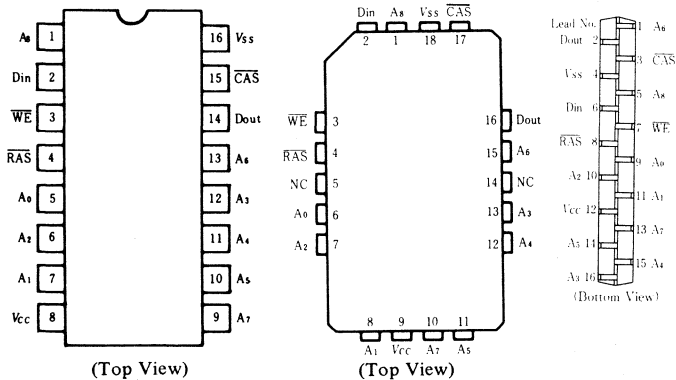
262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

- Industry standard 16-pin DIP, 18-pin PLCC, 16-Pin ZIP
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 120ns/150ns/200ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles (4ms)
- 3 Variations of refresh; $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh

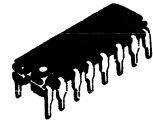
■ PIN ARRANGEMENT

- HM50257P Series
- HM50257CP Series
- HM50257ZP Series



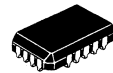
$A_0 \sim A_7$	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

HM50257P Series



(DP-16B)

HM50257CP Series



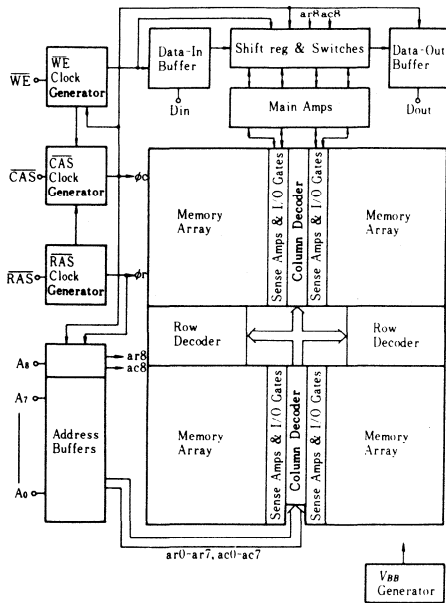
(CP-18)

HM50257ZP Series



(ZP-16)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} -1V to +7V
- Operating temperature, T_a (Ambient) 0°C to +70°C
- Storage temperature -55°C to +125°C
- Short circuit output current 50mA
- Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note 1) All voltages referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to +70°C, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Operating Current (\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = \min$)	I_{CC1}	—	83	—	70	—	55	mA	1
Stand by Current ($RAS = V_{IH}$, Dout=High Impedance)	I_{CC2}	—	4.5	—	4.5	—	4.5	mA	
Refresh Current (RAS only Refresh, $t_{RC} = \min$)	I_{CC3}	—	62	—	53	—	42	mA	
Standby Current ($\overline{RAS} = V_{IH}$, Dout Enable)	I_{CC5}	—	10	—	10	—	10	mA	1
Refresh Current (\overline{CAS} before \overline{RAS} Refresh, $t_{RC} = \min$)	I_{CC6}	—	69	—	58	—	45	mA	
Nibble Mode Supply Current ($RAS = V_{IL}$, \overline{CAS} Cycling, $t_{RC} = \min$)	I_{CC8}	—	57	—	48	—	37	mA	
Input leakage ($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output leakage ($0 < V_{out} < 7V$, Dout=Disable)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output levels High ($I_{out} = -5mA$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low ($I_{out} = 4.2mA$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. $I_{CC \max}$, is specified at the output open condition.

■ **CAPACITANCE** ($V_{CC} = 5V \pm 10\%$, $T_a = 25^\circ C$)

Parameter	Symbol	typ	max	Unit	Notes	
Input Capacitance	Address, Data-In	C_{I1}	—	5	pF	1
	Clocks	C_{I2}	—	7		1, 2
Output Capacitance	Data-Out	C_O	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. $CAS = V_{IH}$ to disable Dout.

■ **ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS**

($T_a = 0$ to $+70^\circ C$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)^{1), 10), 11)}

Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
RAS to CAS Delay Time	t_{RCD}	25	60	25	75	30	100	ns	7
Access Time from RAS	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	t_{CAC}	—	60	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
RAS Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
RAS Hold Time	t_{RSH}	60	—	75	—	100	—	ns	
CAS Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
CAS Pulse Width	t_{CAS}	60	10000	75	10000	100	10000	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time referenced to RAS	t_{AR}	80	—	100	—	130	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	40	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	t_{WCR}	100	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	40	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	40	—	45	—	55	—	ns	
Write Command to CAS Lead Time	t_{CWL}	40	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	40	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to RAS	t_{DHR}	100	—	120	—	155	—	ns	
RAS to WE Delay	t_{RWD}	120	—	150	—	200	—	ns	
CAS to WE Delay	t_{CWD}	60	—	75	—	100	—	ns	8
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
CAS Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS Refresh)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to CAS Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Nibble Mode Access Time	t_{NAC}	—	25	—	25	—	35	ns	
Nibble Mode RAS Cycle Time	t_{NRC}	390	—	460	—	590	—	ns	
Nibble Mode RAS Pulse Width	t_{NRA}	290	—	350	—	460	—	ns	
Nibble Mode Cycle Time	t_{NXC}	55	—	60	—	80	—	ns	
Nibble Mode CAS Precharge Time	t_{NCP}	20	—	25	—	35	—	ns	
Nibble Mode CAS Pulse Width	t_{NCA}	25	—	25	—	35	—	ns	

(to be continued)

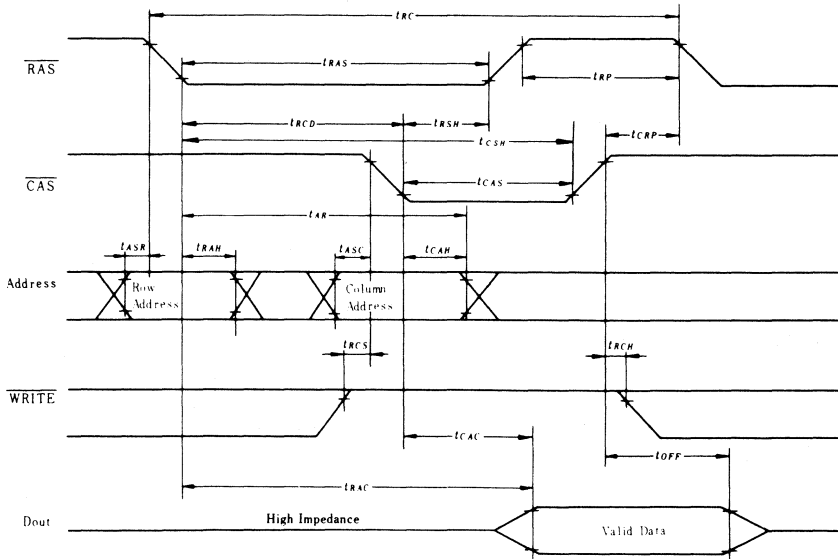
Parameter	Symbol	HM50257-12		HM50257-15		HM50257-20		Unit	Notes
		min	max	min	max	min	max		
Nibble Mode $\overline{\text{RAS}}$ Hold Time	t_{NRSH}	40	—	45	—	55	—	ns	
Nibble Mode $\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t_{NCWD}	20	—	25	—	35	—	ns	
Nibble Mode Write Command to $\overline{\text{CAS}}$ Lead Time	t_{NCWL}	20	—	25	—	35	—	ns	
Nibble Mode Write Command to $\overline{\text{RAS}}$ Lead Time	t_{NRWL}	40	—	45	—	55	—	ns	
Nibble Mode Write Command Pulse Width	t_{NWP}	20	—	25	—	35	—	ns	
Nibble Mode Read/Write Cycle Time	t_{NRWC}	75	—	90	—	120	—	ns	
Nibble Mode Read/Write $\overline{\text{CAS}}$ Pulse Width	t_{NCAS}	45	—	55	—	75	—	ns	

Notes

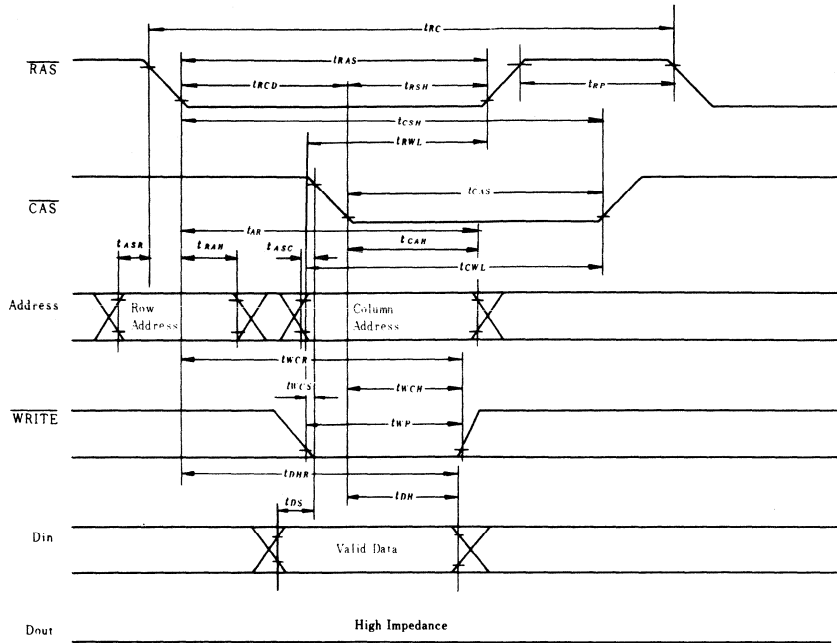
- AC measurements assume $t_T = 5\text{ns}$.
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
- $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
- $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .
- t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
- An initial pause of 100 μs is required after power-up then excute at least 8 initialization cycles.
- At least, 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

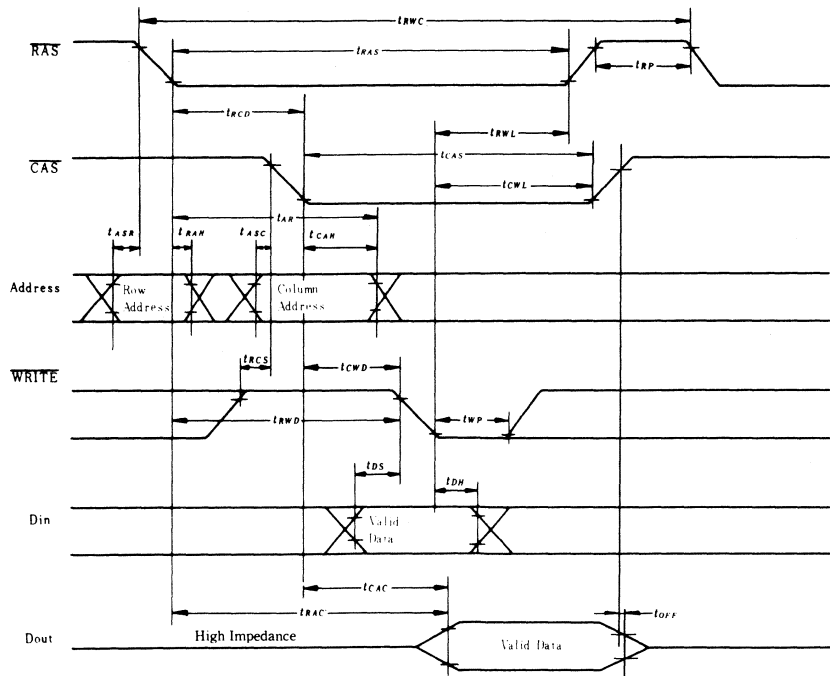
● READ CYCLE



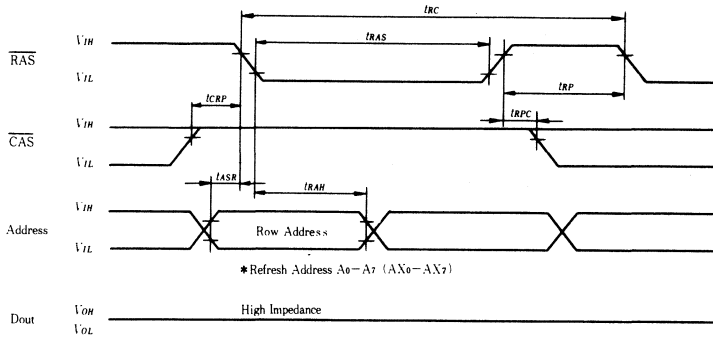
● WRITE CYCLE



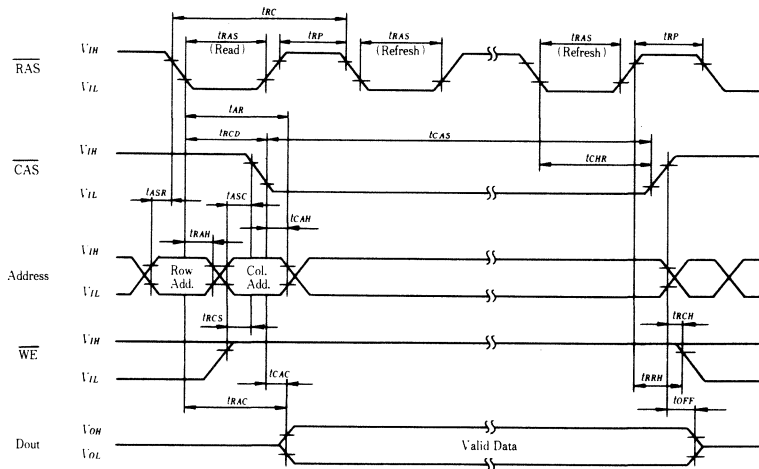
● READ MODIFY WRITE CYCLE



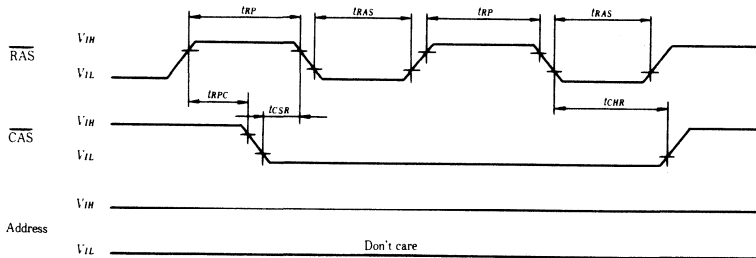
● RAS ONLY REFRESH CYCLE



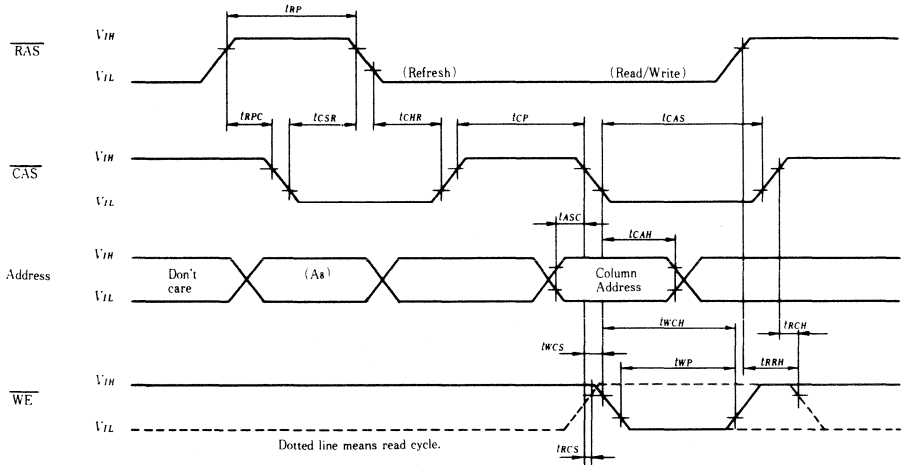
● HIDDEN REFRESH CYCLE



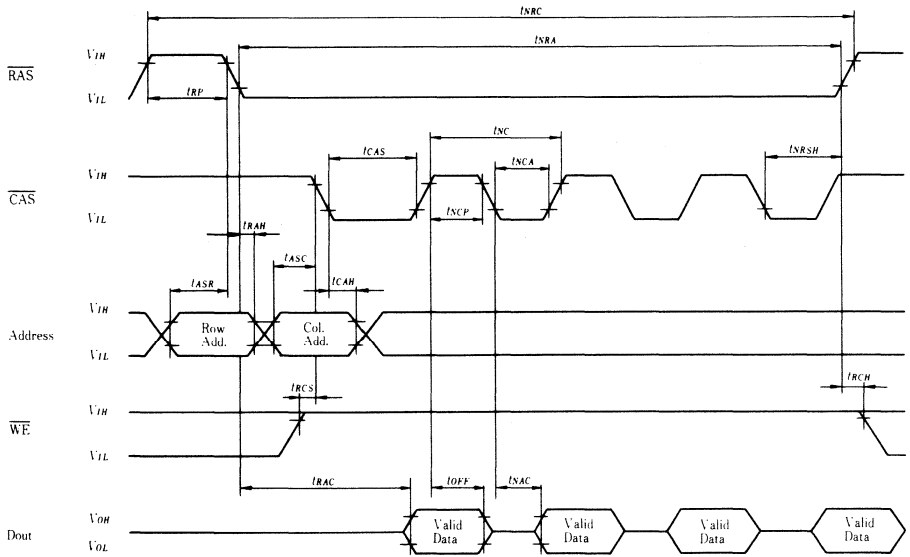
● CAS BEFORE RAS REFRESH CYCLE



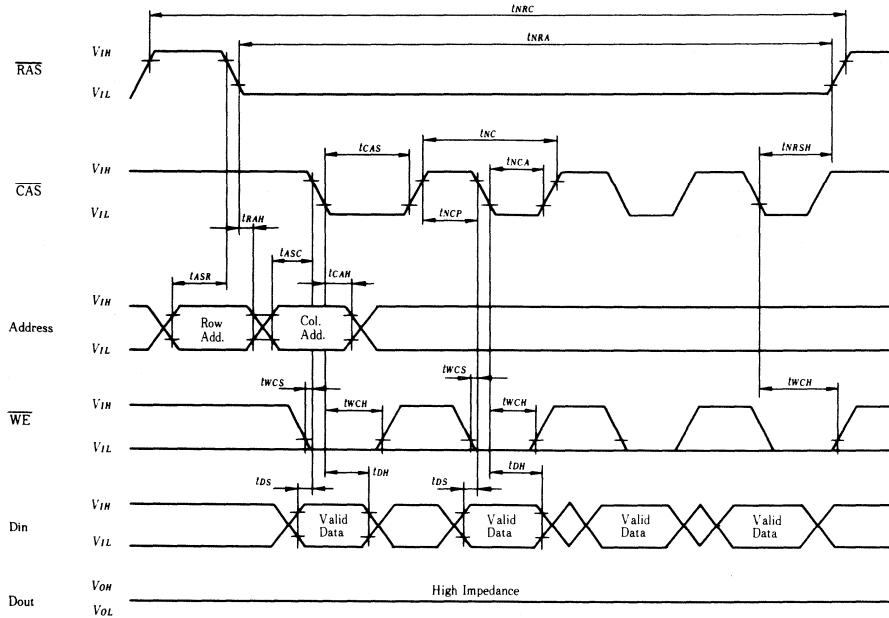
● COUNTER TEST



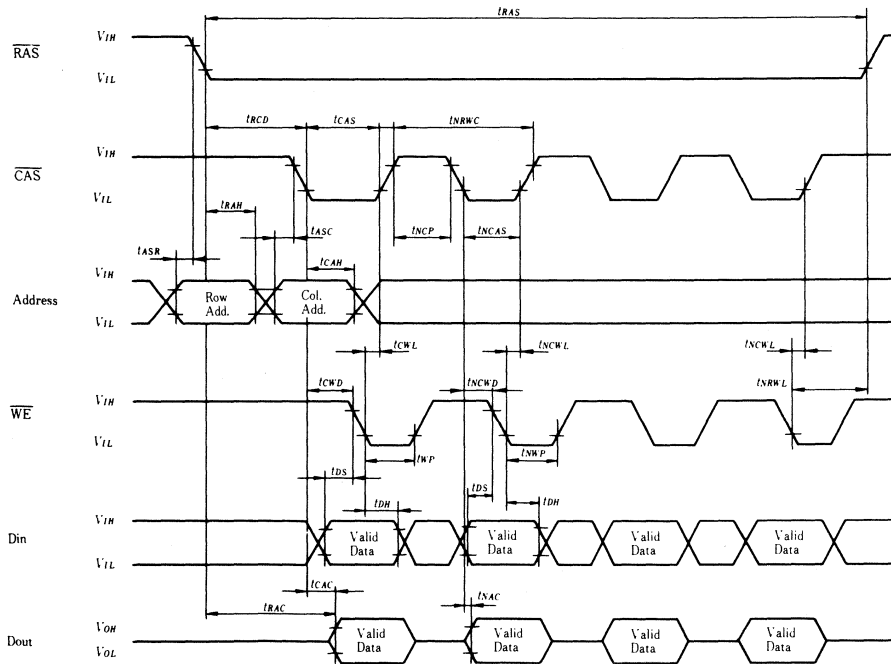
● NIBBLE MODE READ CYCLE



● NIBBLE MODE WRITE CYCLE



● NIBBLE MODE READ MODIFY WRITE CYCLE

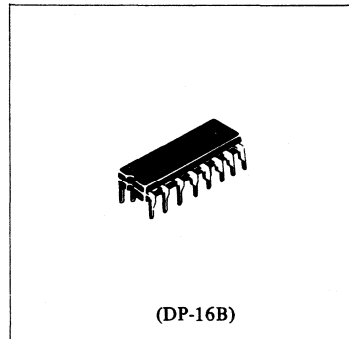


HM50257AP Series — Under development

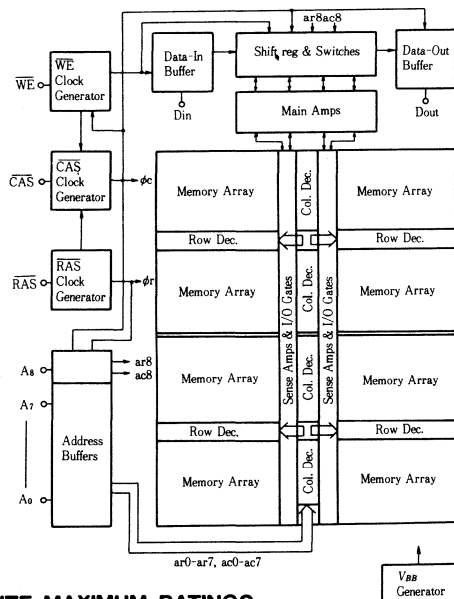
262144-word × 1-bit Dynamic Random Access Memory

■ FEATURES

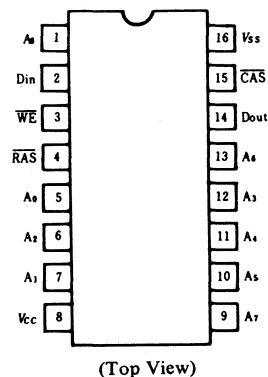
- Industry standard 16-pin DIP (plastic)
- Single 5V (±10%)
- On chip substrate bias generator
- Low Power: 350mW active, 20mW standby
- High speed: Access Time 100ns/120ns/150ns (max.)
- Common I/O capability using early write operation
- Nibble mode capability
- TTL compatible
- 256 refresh cycles (4ms)
- 3 Variations of refresh; $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh



■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



A ₀ ~A ₇	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V _{cc}	Power (+5V)
V _{ss}	Ground
A ₀ ~A ₇	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} -1V to +7V
- Operating temperature, T_a (Ambient) 0°C to +70°C
- Storage temperature -55°C to +125°C
- Short circuit output current 50mA
- Power dissipation 1W

■ RECOMMENDED DC OPERATING CONDITIONS (T_a=0 to +70°C)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V _{cc}	4.5	5.0	5.5	V	1
Input High Voltage	V _{IH}	2.4	—	6.5	V	1
Input Low Voltage	V _{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}.

HM51256P Series HM51256CP Series

Preliminary

262144-word × 1-bit CMOS Dynamic Random Access Memory

■ FEATURE

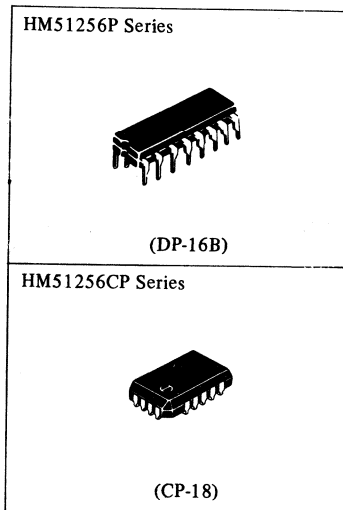
- 262, 144 word x 1 bit DRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Policide Process, high performance CMOS
- Power supply voltage: 5V ± 10%
- Access time
 - Row access time: 100/120/150ns
 - Address access time: 45/55/70ns
- Cycle time
 - Random read/write cycle time: 180/210/250ns
 - High speed page mode cycle time: 55/65/80ns
- Lower power
 - Standby: 11mW
 - Active: 330/275/220mW
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: $\overline{\text{RAS}}$ only refresh, $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast CAS output control

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} -1V to +7V
 Operating temperature, T_a (Ambient) 0°C to +70°C
 Storage temperature -55°C to +125°C
 Short circuit output current 50mA
 Power dissipation 1W

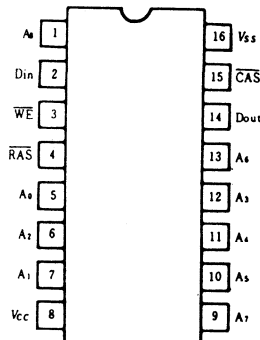
$A_0 \sim A_8$	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_9 \sim A_7$	Refresh Address Inputs

Note) The specifications of this device are subject to change without notice.
 Please contact your nearest Hitachi's Sales Dept. regarding specifications.



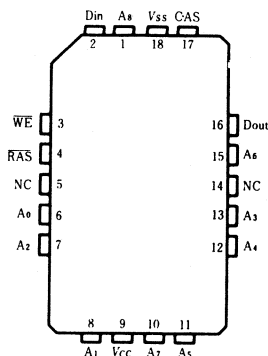
■ PIN ARRANGEMENT

● HM51256P Series



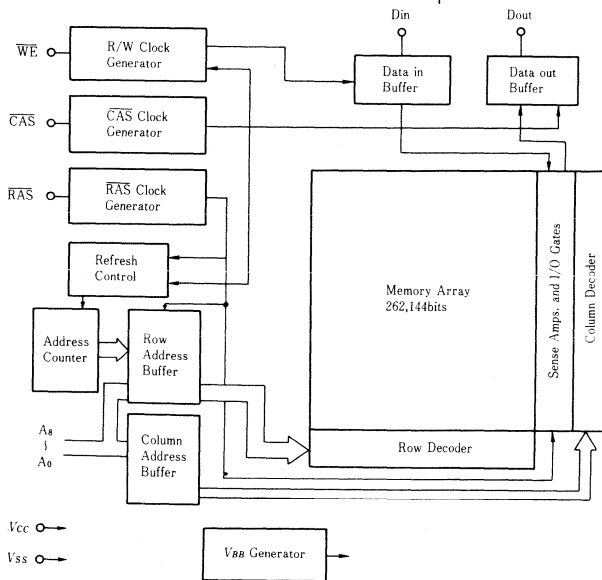
(Top View)

● HM51256CP Series



(Top View)

■ BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
Operating Current ($\overline{\text{RAS}}$, $\overline{\text{CAS}}$ Cycling: $t_{RC}=\text{min}$)	I_{CC1}	—	60	—	50	—	40	mA	1
Standby Current ($\overline{\text{RAS}}=V_{IH}$, Dout=High Impedance)	I_{CC2}	—	2	—	2	—	2	mA	
Refresh Current ($\overline{\text{RAS}}$ only Refresh, $t_{RC}=\text{min}$)	I_{CC3}	—	60	—	50	—	40	mA	
Standby Current ($\overline{\text{RAS}}=V_{IH}$, Dout Enable)	I_{CC4}	—	6	—	6	—	6	mA	1
Refresh Current ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh, $t_{RC}=\text{min}$)	I_{CC5}	—	55	—	45	—	35	mA	
Page Mode Supply Current ($\overline{\text{RAS}}=V_{IL}$, $\overline{\text{CAS}}$ Cycling, $t_{PC}=\text{min}$)	I_{CC6}	—	60	—	50	—	40	mA	
Input leakage ($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	μA	
Output leakage ($0 < V_{out} < 7V$, Dout=Disable)	I_{LO}	-10	10	-10	10	-10	10	μA	
Output levels High ($I_{out}=-5\text{mA}$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low ($I_{out}=4.2\text{mA}$)	V_{OL}	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max. is specified at the output open condition.

■ CAPACITANCE ($V_{CC}=5V \pm 10\%$, $T_a=25^\circ\text{C}$)

Parameter	Symbol	typ	max	Unit	Notes	
Input Capacitance	Address, Data-in	C_{I1}	—	5	pF	1
	Clocks	C_R	—	7		1
Output Capacitance	Data-out	C_O	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
2. $\overline{\text{CAS}}=V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	180	—	210	—	250	—	ns	
RAS Precharge Time	t_{RP}	70	—	80	—	90	—	ns	
RAS Pulse Width	t_{RAS}	65	10000	75	10000	95	10000	ns	
CAS Pulse Width	t_{CAS}	25	—	30	—	35	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time to RAS	t_{AR}	75	—	90	—	110	—	ns	
RAS to CAS Delay Time	t_{RCD}	25	75	25	90	30	115	ns	8
RAS to Column Address Delay Time	t_{RAD}	20	55	20	65	25	80	ns	9
RAS Hold Time	t_{RSH}	25	—	30	—	35	—	ns	
CAS Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	

● Read Cycle

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
Access Time from RAS	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from CAS	t_{CAC}	—	25	—	30	—	35	ns	3, 4
Access Time from Address	t_{AA}	—	45	—	55	—	70	ns	3, 5, 14
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	45	—	55	—	70	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	25	0	30	0	35	ns	6

● Write Cycle

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	25	—	30	—	35	—	ns	
Write Command Hold Time to RAS	t_{WCR}	80	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WCP}	20	—	25	—	30	—	ns	
Write Command to RAS Lead Time	t_{RWL}	25	—	30	—	35	—	ns	
Write Command to CAS Lead Time	t_{CWL}	25	—	30	—	35	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	25	—	30	—	ns	10, 11
Data-in Hold Time to RAS	t_{DHR}	75	—	90	—	110	—	ns	

● Read-Modify-Write Cycle

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	210	—	245	—	290	—	ns	
RAS to WE Delay Time	t_{RWD}	100	—	120	—	150	—	ns	10
CAS to WE Delay Time	t_{CWD}	25	—	30	—	35	—	ns	10
Column Address to WE Delay Time	t_{AWD}	45	—	55	—	70	—	ns	10

● Refresh Cycle

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
CAS Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

● High Speed Page Mode Cycle

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	18, 20
High Speed Page Mode $\overline{\text{RAS}}$ Pulse Width	t_{RAPC}	65	75000	75	75000	95	75000	ns	19
$\overline{\text{RAS}}$ to Second $\overline{\text{WE}}$ Delay Time	t_{RSW}	105	—	125	—	155	—	ns	
CAS Precharge Time	t_{CP}	15	—	20	—	20	—	ns	
Write Invalid Time	t_{WI}	10	—	15	—	15	—	ns	
Access Time from Column Precharge Time	t_{CAP}	—	50	—	60	—	75	ns	20

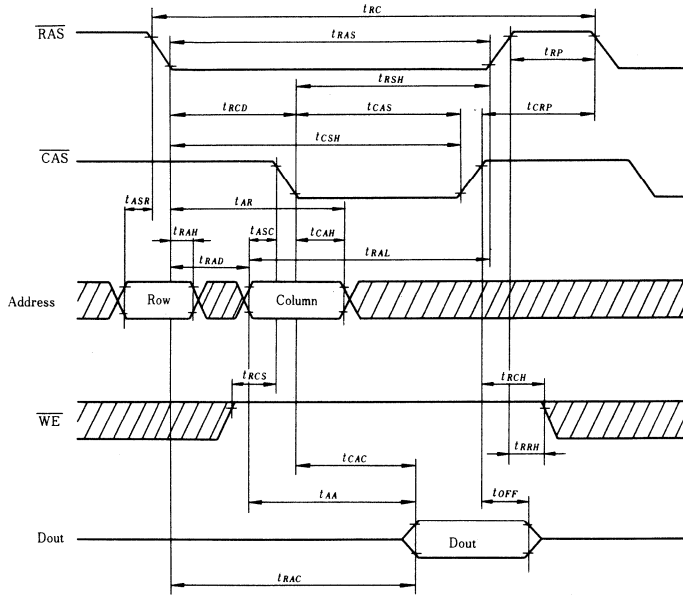
● High Speed Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM51256P/CP-10		HM51256P/CP-12		HM51256P/CP-15		Unit	Notes
		min	max	min	max	min	max		
High Speed Page Mode Cycle Time on Read-Write	t_{RWPC}	95	—	115	—	145	—	ns	12
Access Time from Previous $\overline{\text{WE}}$	t_{PWA}	—	90	—	110	—	140	ns	3, 13
Previous $\overline{\text{WE}}$ to Column Address Delay Time	t_{WAD}	25	45	30	55	35	70	ns	15

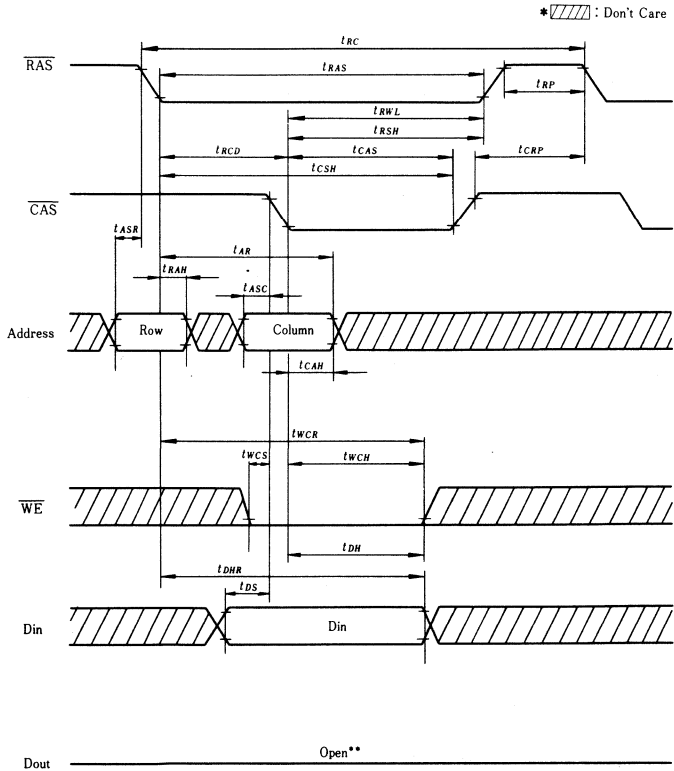
- Notes:
1. AC measurements assume $t_T = 5\text{ns}$.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value show in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$, $t_{RAD} \leq t_{RAD}(\text{max})$.
 5. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
 6. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 7. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 8. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 9. Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a Reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 12. $t_{RWPC}(\text{min}) = t_{AWD}(\text{min}) + t_{WAD}(\text{max}) + t_T$.
 13. Assumes that $t_{WAD} \leq t_{WAD}(\text{max})$. If t_{WAD} is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
 14. Assumes that $t_{WAD} \geq t_{WAD}(\text{max})$.
 15. Operation with the $t_{WAD}(\text{max})$ limit insures that $t_{PWA}(\text{max})$ can be met, $t_{WAD}(\text{max})$ is specified as a reference point only, if t_{WAD} is greater than the specified $t_{WAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 16. An initial pause of 100 μs is required after power-up then execute at least 8 initialization cycles.
 17. At least, 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles are required before using internal refresh counter.
 18. Assumes that $t_{ASC} = t_{CP} - 5\text{ns}$.
 19. t_{RAPC} defines $\overline{\text{RAS}}$ pulse width in High Speed Page mode cycle.
 20. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP} .

■ TIMING WAVEFORMS

● Read Cycle

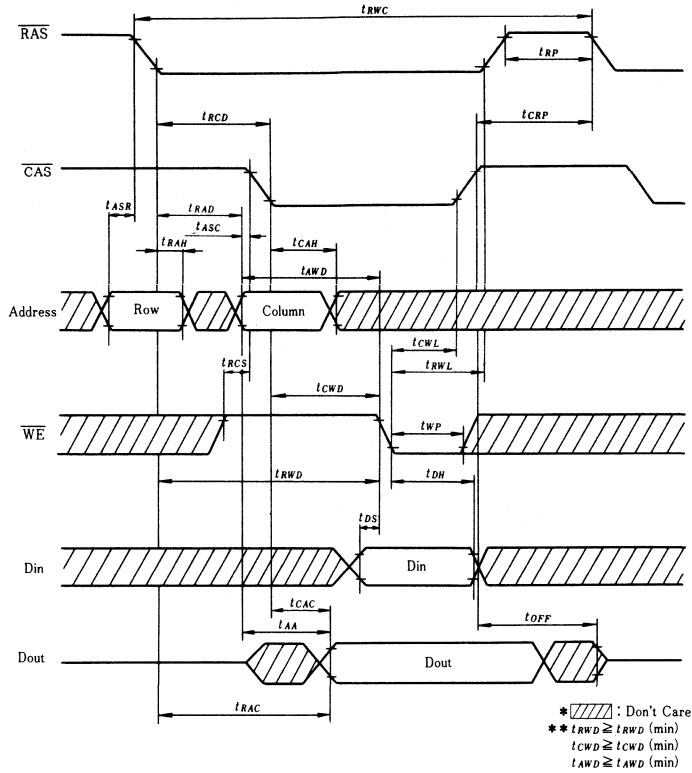


● Write Cycle

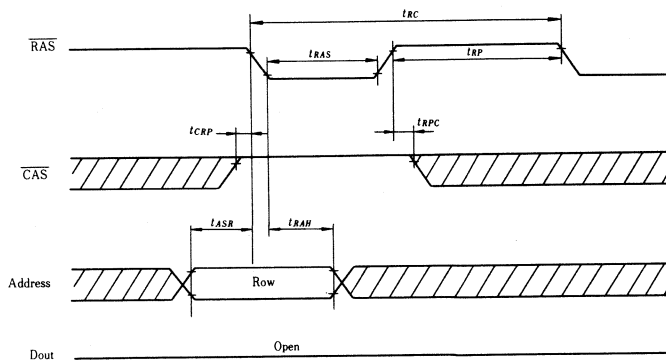


* : Don't Care
 ** $t_{wcs} \geq t_{wcs}(\text{min})$

● Read Modify Write Cycle



● RAS Only Refresh Cycle



* ▨ : Don't Care

HM51256LP Series

HM51256LCP Series

Preliminary

262144-word x 1-bit CMOS Dynamic Random Access Memory

FEATURE

- 262, 144 word x 1-bit DRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Polycide process high performance CMOS
- Power supply voltage: $5V \pm 10\%$
- Access time
 - Row access time: 100/120/150ns
 - Address access time: 45/55/70ns
- Cycle time
 - Random read/write cycle time: 180/210/250ns
 - High speed page mode cycle time: 55/65/80ns
- Lower power
 - Standby: 11mW (TTL level), 1.1 mW (CMOS level)
 - Active: 330/275/220mW
 - Data Retention Current: $300\mu A/t_{REF} = 32ms$
- Input and output: TTL compatible
- Refresh: 256 cycles/4ms
- Refresh function: RAS only refresh, \overline{CAS} before \overline{RAS} refresh, Hidden refresh
- High speed page mode capability
- Edge triggered write capability
- Fast CAS output control.

ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} -1V to +7V
 Operating temperature, T_a (Ambient) $0^\circ C$ to $+70^\circ C$
 Storage temperature $-55^\circ C$ to $+125^\circ C$
 Short circuit output current 50mA
 Power dissipation 1W

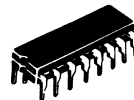
(Top View)

$A_0 \sim A_7$	Address Inputs
\overline{CAS}	Column Address Strobe
Din	Data In
Dout	Data Out
\overline{RAS}	Row Address Strobe
\overline{WE}	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_8 \sim A_{17}$	Refresh Address Inputs

Note) The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM51256LP Series



(DP-16B)

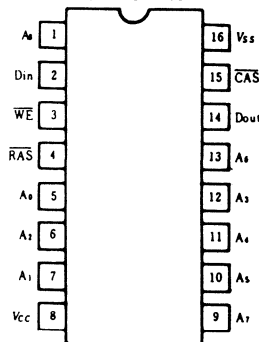
HM51256LCP Series



(CP-18)

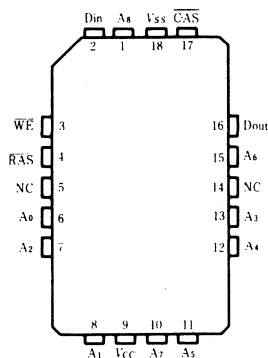
PIN ARRANGEMENT

HM51256LP Series



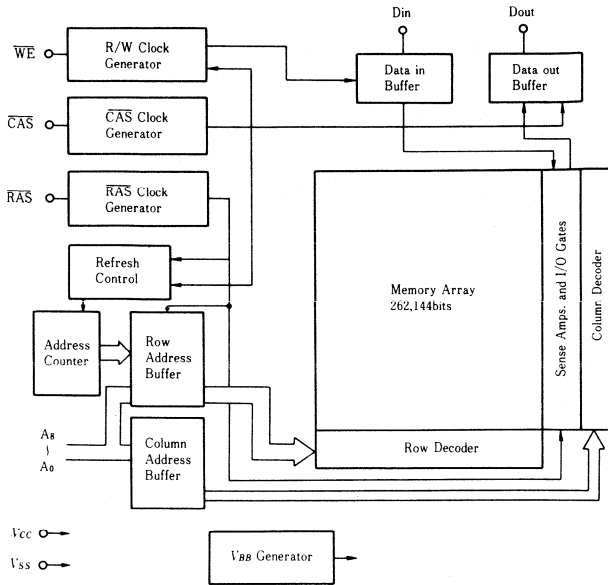
(Top View)

HM51256LCP Series



(Top View)

■BLOCK DIAGRAM



■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min	typ	max	Unit	Note
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Note) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$)

Parameter	Symbol	HM51256LP/LCP-10						HM51256LP/LCP-12		HM51256LP/LCP-15		Unit	Notes
		min	max	min	max	min	max	min	max				
Operating Current (RAS, CAS Cycling: $t_{RC} = \text{min}$)	I_{CC1}	—	60	—	50	—	40	—	40	—	40	mA	1
Standby Current (RAS = V_{IH} , Dout = High Impedance)	I_{CC2}	—	2	—	2	—	2	—	2	—	2	mA	
Refresh Current (RAS only Refresh, $t_{RC} = \text{min}$)	I_{CC3}	—	60	—	50	—	40	—	40	—	40	mA	
Standby Current (RAS = V_{IH} , Dout Enable)	I_{CC4}	—	6	—	6	—	6	—	6	—	6	mA	1
Standby Current (RAS, CAS = $V_{CC} - 0.2V$)	I_{CC5}	—	200	—	200	—	200	—	200	—	200	μA	
Refresh Current (CAS before RAS Refresh, $t_{RC} = \text{min}$)	I_{CC6}	—	55	—	45	—	35	—	35	—	35	mA	
Page Mode Supply Current (RAS = V_{IL} , CAS Cycling, $t_{PC} = \text{min}$)	I_{CC7}	—	60	—	50	—	40	—	40	—	40	mA	1
Input leakage ($0 < V_{in} < 7V$)	I_{LI}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	
Output leakage ($0 < V_{out} < 7V$, Dout = Disable)	I_{LO}	-10	10	-10	10	-10	10	-10	10	-10	10	μA	
Output levels High ($I_{out} = -5\text{mA}$)	V_{OH}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output levels Low ($I_{out} = 4.2\text{mA}$)	V_{OL}	0	0.4	0	0.4	0	0.4	0	0.4	0	0.4	V	

Notes) 1. I_{CC} depends on output loading condition when the device is selected. I_{CC} max is specified at the output open condition.

■ CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^\circ\text{C}$)

Parameter	Symbol	typ	max	Unit	Notes	
Input Capacitance	Address, Data-in	C_{II}	—	5	pF	1
	Clocks	C_{II}	—	7		1, 2
Output Capacitance	Data-out	C_O	—	7		1, 2

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. CAS = V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5V\pm 10\%$, $V_{SS}=0V$)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{TRC}	180	—	210	—	250	—	ns	
RAS Precharge Time	t_{TRP}	70	—	80	—	90	—	ns	
RAS Pulse Width	t_{RAS}	65	10000	75	10000	95	10000	ns	
CAS Pulse Width	t_{CAS}	25	—	30	—	35	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	25	—	30	—	ns	
Column Address Hold Time to $\overline{\text{RAS}}$	t_{AR}	75	—	90	—	110	—	ns	
RAS to CAS Delay Time	t_{RCD}	25	75	25	90	30	115	ns	8
RAS to Column Address Delay Time	t_{RAD}	20	55	20	65	25	80	ns	9
RAS Hold Time	t_{RSH}	25	—	30	—	35	—	ns	
CAS Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
Refresh Period	t_{REF2}	—	32	—	32	—	32	ms	18

● Read Cycle

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from CAS	t_{CAC}	—	25	—	30	—	35	ns	3, 4
Access Time from Address	t_{AA}	—	45	—	55	—	70	ns	3, 5, 14
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	45	—	55	—	70	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	25	0	30	0	35	ns	6

● Write Cycle

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	25	—	30	—	35	—	ns	
Write Command Hold Time to $\overline{\text{RAS}}$	t_{WCR}	80	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WP}	20	—	25	—	30	—	ns	
Write Command to RAS Lead Time	t_{RWL}	25	—	30	—	35	—	ns	
Write Command to CAS Lead Time	t_{CWL}	25	—	30	—	35	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	25	—	30	—	ns	10, 11
Data-in Hold Time to RAS	t_{DHR}	75	—	90	—	110	—	ns	

● Read-Modify-Write Cycle

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWc}	210	—	245	—	290	—	ns	
RAS to WE Delay Time	t_{RWD}	100	—	120	—	150	—	ns	10
CAS to WE Delay Time	t_{CWD}	25	—	30	—	35	—	ns	10
Column Address to WE Delay Time	t_{AWD}	45	—	55	—	70	—	ns	10

● Refresh Cycle

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
CAS Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CHR}	10	—	10	—	10	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	15	—	15	—	15	—	ns	

● High Speed Page Mode Cycle

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
High Speed Page Mode Cycle Time	t_{PC}	55	—	65	—	80	—	ns	19, 21
High Speed Page Mode $\overline{\text{RAS}}$ Pulse Width	t_{RAPC}	65	75000	75	75000	95	75000	ns	20
$\overline{\text{RAS}}$ to Second $\overline{\text{WE}}$ Delay Time	t_{RSW}	105	—	125	—	155	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CP}	15	—	20	—	20	—	ns	
Write Invalid Time	t_{WI}	10	—	15	—	15	—	ns	
Access Time from Column Precharge Time	t_{CAP}	—	50	—	60	—	75	ns	21

● High Speed Page Mode Read-Modify-Write Cycle

Parameter	Symbol	HM5126LP/LCP-10		HM5126LP/LCP-12		HM5126LP/LCP-15		Unit	Notes
		min	max	min	max	min	max		
High Speed Page Mode Cycle Time on Read-Write	t_{RWPC}	95	—	115	—	145	—	ns	12
Access Time from Previous $\overline{\text{WE}}$	t_{PWA}	—	90	—	110	—	140	ns	3, 13
Previous $\overline{\text{WE}}$ to Column Address Delay Time	t_{WAD}	25	45	30	55	35	70	ns	15

Notes: 1. AC measurements assume $t_T = 5\text{ns}$.

2. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.

3. Measured with a load circuit equivalent to 2TTL loads and 100pF.

4. Assumes that $t_{\text{RCD}} \geq t_{\text{RCD}}(\text{max})$, $t_{\text{RAD}} \leq t_{\text{RAD}}(\text{max})$.

5. Assumes that $t_{\text{RCD}} \leq t_{\text{RCD}}(\text{max})$ and $t_{\text{RAD}} \geq t_{\text{RAD}}(\text{max})$.

6. $t_{\text{OFF}}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

7. $V_{\text{IH}}(\text{min})$ and $V_{\text{IL}}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .

8. Operation with the $t_{\text{RCD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RCD}}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{\text{RCD}}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .

9. Operation with the $t_{\text{RAD}}(\text{max})$ limit insures that $t_{\text{RAC}}(\text{max})$ can be met, $t_{\text{RAD}}(\text{max})$ is specified as a Reference point only, if t_{RAD} is greater than the specified $t_{\text{RAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .

10. t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{\text{WCS}} \geq t_{\text{WCS}}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{\text{RWD}} \geq t_{\text{RWD}}(\text{min})$, $t_{\text{CWD}} \geq t_{\text{CWD}}(\text{min})$ and $t_{\text{AWD}} \geq t_{\text{AWD}}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.

11. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read modify write cycles.

12. $t_{\text{RWPC}}(\text{min}) = t_{\text{AWD}}(\text{min}) + t_{\text{WAD}}(\text{max}) + t_T$.

13. Assumes that $t_{\text{WAD}} \leq t_{\text{WAD}}(\text{max})$. If t_{WAD} is greater than the maximum recommended value shown in this table t_{PWA} exceeds the value shown.

14. Assumes that $t_{\text{WAD}} \geq t_{\text{WAD}}(\text{max})$.

15. Operation with the $t_{\text{WAD}}(\text{max})$ limit insures that $t_{\text{PWA}}(\text{max})$ can be met, $t_{\text{WAD}}(\text{max})$ is specified as a reference point only, if t_{WAD} is greater than the specified $t_{\text{WAD}}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .

16. An initial pause of 100 μs is required after power-up then execute at least 8 initialization cycles.

17. At least 8 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh cycles are required before using internal refresh counter.

18. The HM51256L extends the refresh period to 32ms during $\overline{\text{RAS}}$ only refresh operation.

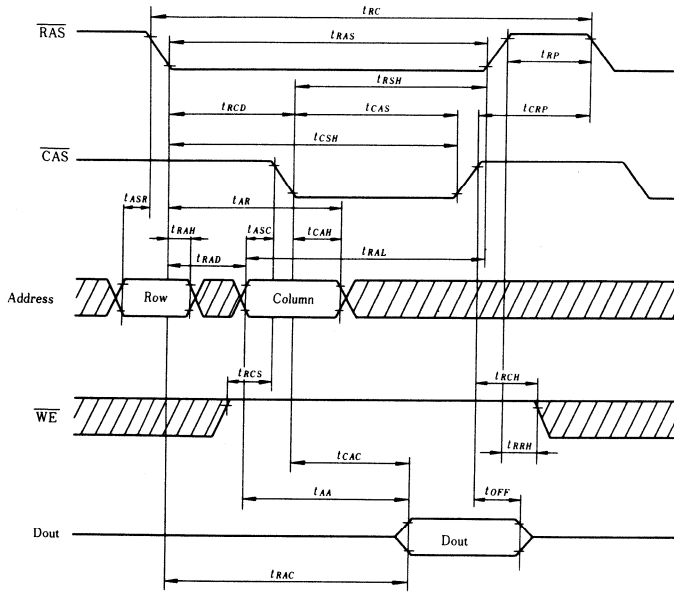
19. Assumes that $t_{\text{ASC}} = t_{\text{CP}} - 5\text{ns}$.

20. t_{RAPC} defines $\overline{\text{RAS}}$ pulse width in High Speed Page mode cycle.

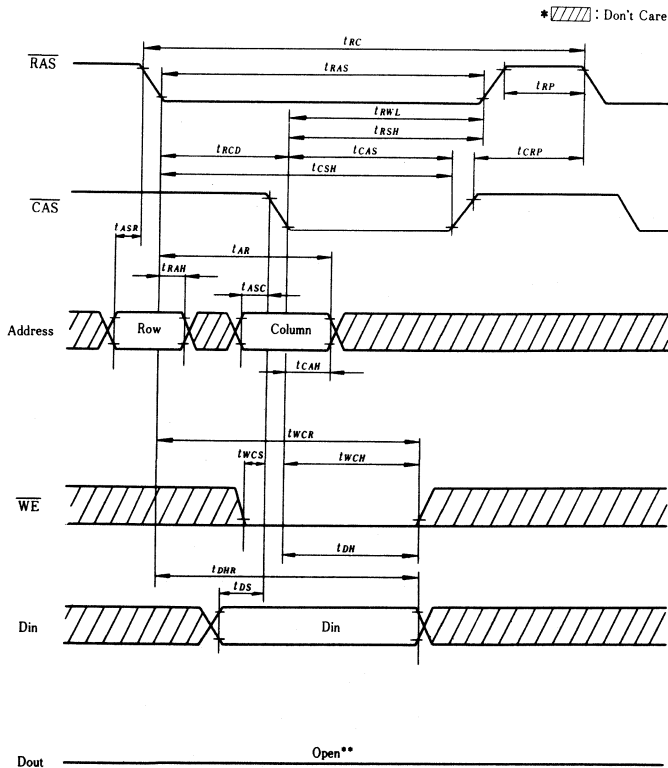
21. Access time is determined by the longer of t_{AA} or t_{CAC} or t_{CAP} .

■ TIMING WAVEFORMS

● Read Cycle

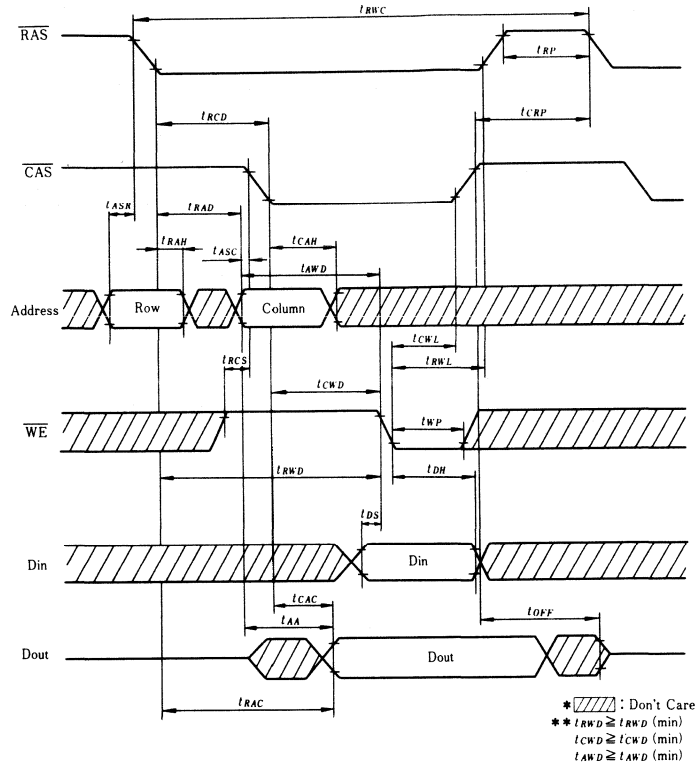


● Write Cycle

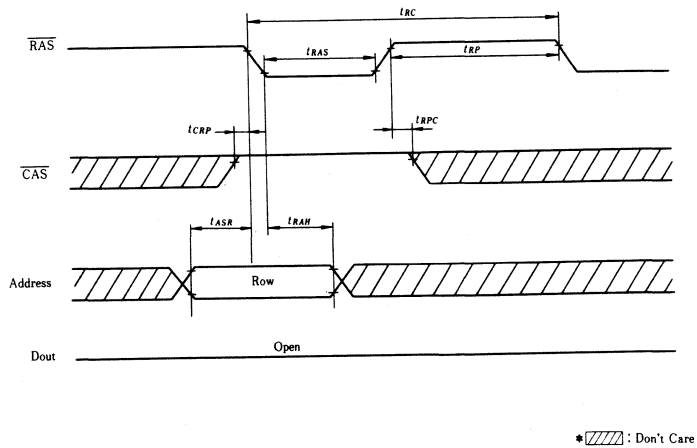


* [hatched box] : Don't Care
 ** $t_{wcs} \geq t_{wcs}(\text{min})$

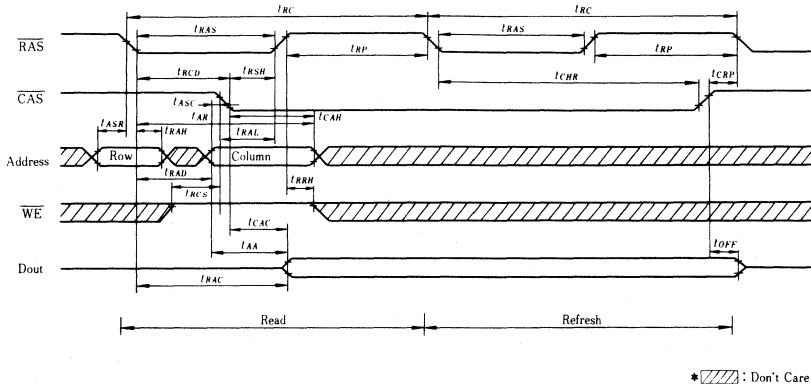
● Read Modify Write Cycle



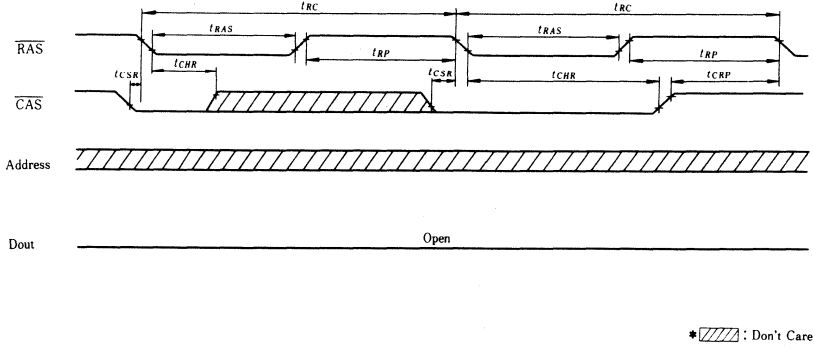
● RAS Only Refresh Cycle



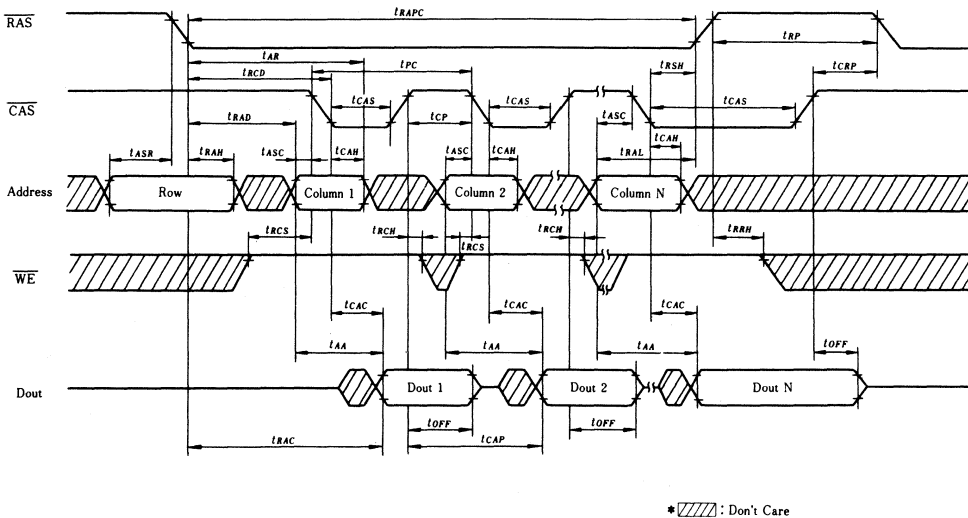
● Hidden Refresh Cycle



● CAS Before RAS Refresh Cycle



● High Speed Page Mode Read Cycle



HM51258P Series, HM51258CP Series

262144-word x 1-bit Static Column Dynamic RAM

The HM51258 is the 262,144 word by 1 bit static column dynamic random access memory utilizing the Hitachi $2\mu\text{m}$ CMOS process.

This device has static column circuit and it is good for high performance main storage or for page access applications.

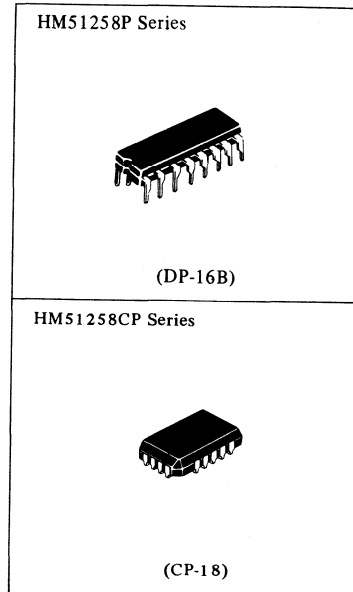
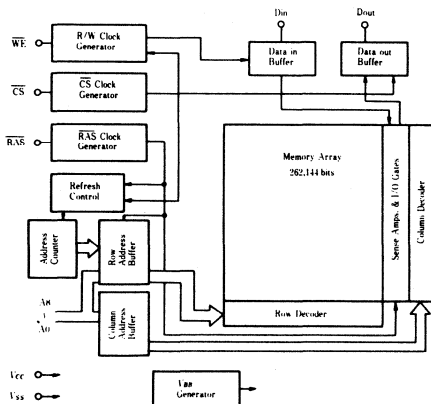
While the row circuitry is still dynamic, and it controls the power consumed in the static circuitry. It realizes very low power dissipation.

Multiplexed address and the 16 pin pinout are compatible with the fully dynamic 256K DRAM HM50256.

■ FEATURES

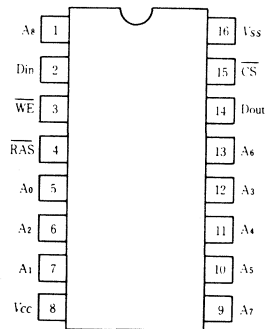
- 262,144 word x 1 bit SCRAM
- Plastic 16 pin DIP & 18 pin PLCC
- Double layer Poly-Si/Polycide Process, high performance CMOS
- Power supply voltage— $5\text{V} \pm 10\%$
- Access time
 - Row access time—85/100/120/150ns
 - Address access time—40/45/55/70ns
- Cycle time
 - Random Read&Write cycle time—155/180/210/250ns
 - Static Column cycle time—45/50/60/75ns
- Lower power
 - Standby — 1mW
 - Active — 385/330/275/220mW
- Input and output—TTL compatible
- Refresh—256 cycles/4ms
- Refresh function— $\overline{\text{RAS}}$ only refresh, $\overline{\text{CS}}$ before $\overline{\text{RAS}}$ refresh, Hidden refresh
- Static column mode capability
- Edge triggered write capability
- Fast $\overline{\text{CS}}$ output control

■ BLOCK DIAGRAM



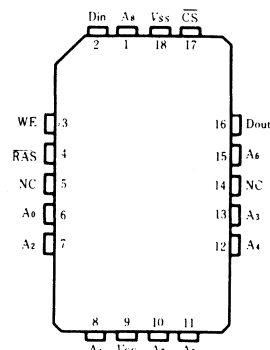
■ PIN ARRANGEMENT

● HM51258P Series



(Top View)

● HM51258CP Series



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Parameter	Symbol	Rating	Unit
Voltage on any pin relative to V_{SS}	V_T	-1.0 to +7.0	V
Supply Voltage relative to V_{SS}	V_{CC}	-1.0 to +7.0	V
Short circuit output current	I_{out}	50	mA
Power dissipation	P_T	1.0	W
Operating temperature	T_{opr}	0 to +70	°C
Storage temperature	T_{stg}	-55 to +125	°C

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input high voltage	V_{IH}	2.4	-	6.5	V
Input low voltage	V_{IL}	-1.0	-	0.8	V

Note) All voltages referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to +70°C)

Parameter	Symbol	Test conditions	HM51258-8		HM51258-10		HM51258-12		HM51258-15		Unit	Note
			min	max	min	max	min	max	min	max		
Operating current	$ICC1$	RAS, CS Cycling, $t_{RC}=\text{min}$.	-	70	-	60	-	50	-	40	mA	1
Standby current	$ICC2$	RAS= V_{IH} , Dout=High Impedance	-	2	-	2	-	2	-	2	mA	
Refresh current	$ICC3$	RAS only Refresh, $t_{RC}=\text{min}$	-	70	-	60	-	50	-	40	mA	
Standby current	$ICC4$	RAS= V_{IH} , Dout Enable	-	6	-	6	-	6	-	6	mA	1
Refresh current	$ICC5$	CS before RAS Refresh, $t_{RC}=\text{min}$	-	60	-	55	-	45	-	35	mA	
Operating current	$ICC6$	Static Column Mode, t_{RSC} , $t_{WSC}=\text{min}$	-	70	-	60	-	50	-	40	mA	1
Input leakage	I_{LI}	$V_{in}=0$ to 7V	-10	10	-10	10	-10	10	-10	10	μA	
Output leakage	I_{LO}	$V_{out}=0$ to 7V	-10	10	-10	10	-10	10	-10	10	μA	
Output high voltage	V_{OH}	$I_{out}=-5\text{mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
Output low voltage	V_{OL}	$I_{out}=4.2\text{mA}$	0	0.4	0	0.4	0	0.4	0	0.4	V	

Note) 1. ICC depends on output loading condition when the device is selected.
 ICC max is specified at the output open condition.

■ CAPACITANCE ($V_{CC}=5V \pm 10\%$, $T_a=25^\circ\text{C}$)

Parameter	Symbol	typ	max	Unit	Note	
Input capacitance	Address, Data-In	C_{I1}	-	5	pF	1
	Clock	C_{I2}	-	7	pF	1
Output capacitance	Data-Out	C_O	-	7	pF	1, 2

Note) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. CS= V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ($T_a=0$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$)

● Read, Write, Read-Modify-Write and Refresh Cycles (Common Parameter)

Parameter	Symbol	HM51258-8		HM51358-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Random Read or Write Cycle Time	t_{RC}	155	—	180	—	210	—	250	—	ns	
RAS Precharge Time	t_{RP}	60	—	70	—	80	—	90	—	ns	
RAS Pulse Width	t_{RAS}	55	10000	65	10000	75	10000	95	10000	ns	
CS Pulse Width	t_{CS}	25	—	25	—	30	—	35	—	ns	
RAS to CS Delay Time	t_{RCD}	20	60	25	75	25	90	30	115	ns	8
RAS to Column Address Delay Time	t_{RAD}	15	45	20	55	20	65	25	80	ns	9
RAS Hold Time	t_{RSH}	20	—	25	—	30	—	35	—	ns	
CS Hold Time	t_{CSH}	85	—	100	—	120	—	150	—	ns	
CS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	10	—	ns	
Row Address Set-Up Time	t_{ASR}	0	—	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	10	—	15	—	15	—	20	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	4	—	4	—	4	—	4	ms	

● Read Cycle

Access Time from RAS	t_{RAC}	—	85	—	100	—	120	—	150	ns	2, 3
Access Time from CS	t_{CAC}	—	25	—	25	—	30	—	35	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	45	—	55	—	70	ns	3,5,14
Column Address Hold Time to RAS on Read	t_{AR}	85	—	100	—	120	—	150	—	ns	
Read Command Set-Up Time	t_{RCS}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to CS	t_{RCH}	0	—	0	—	0	—	0	—	ns	
Read Command Hold Time to RAS	t_{RRH}	10	—	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	40	—	45	—	55	—	70	—	ns	
RAS to Column Address Hold Time	t_{AH}	10	—	15	—	15	—	20	—	ns	16
Output Hold Time from Address	t_{OH}	5	—	5	—	5	—	5	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	20	0	25	0	30	0	35	ns	6

● Write Cycle

Column Address Set-Up Time	t_{ASC}	0	—	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	15	—	20	—	25	—	30	—	ns	
Column Address Hold Time to RAS on Write	t_{AWR}	60	—	75	—	90	—	110	—	ns	
Write Command Set-Up Time	t_{WCS}	0	—	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	35	—	ns	
Write Command Hold Time to RAS	t_{WCR}	65	—	80	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WCP}	15	—	20	—	25	—	30	—	ns	
Write Command to RAS Lead Time	t_{RWL}	20	—	25	—	30	—	35	—	ns	
Write Command to CS Lead Time	t_{CWL}	20	—	25	—	30	—	35	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	15	—	20	—	25	—	30	—	ns	10, 11
Data-in Hold Time to RAS	t_{DHR}	60	—	75	—	90	—	110	—	ns	

(to be continued)

● Read-Modify-Write Cycle

Parameter	Symbol	HM5158-8		HM5158-10		HM51258-12		HM51258-15		Unit	Notes
		min	max	min	max	min	max	min	max		
Read-Write Cycle Time	t_{RWC}	180	–	210	–	245	–	290	–	ns	
RAS to \overline{WE} Delay Time	t_{RWD}	85	–	100	–	120	–	150	–	ns	10
\overline{CS} to \overline{WE} Delay Time	t_{CWD}	20	–	25	–	30	–	35	–	ns	10
Column Address to \overline{WE} Delay Time	t_{AWD}	40	–	45	–	55	–	70	–	ns	10
Output Hold Time from \overline{WE}	t_{OHW}	25	–	25	–	25	–	25	–	ns	

● Refresh Cycle

\overline{CS} Set-up Time (\overline{CS} before \overline{RAS} Refresh)	t_{CSR}	10	–	10	–	10	–	10	–	ns	
\overline{CS} Hold Time (\overline{CS} before \overline{RAS} Refresh)	t_{CHR}	10	–	10	–	10	–	10	–	ns	
RAS Precharge to \overline{CS} Hold Time	t_{RPC}	15	–	15	–	15	–	15	–	ns	

● SC Mode Cycle

SC Mode Cycle Time on Read	t_{RSC}	45	–	50	–	60	–	75	–	ns	
SC Mode Cycle Time on Write	t_{WSC}	45	–	50	–	60	–	75	–	ns	
RAS to Second \overline{WE} Delay Time	t_{RSW}	90	–	105	–	125	–	155	–	ns	
SC Mode \overline{RAS} Pulse Width	t_{RASC}	55	75000	65	75000	75	75000	95	75000	ns	
\overline{CS} Precharge Time	t_{CP}	10	–	10	–	15	–	15	–	ns	
Write Invalid Time	t_{WI}	10	–	10	–	15	–	15	–	ns	

● SC Mode Read-Modify-Write and Mixed Cycle

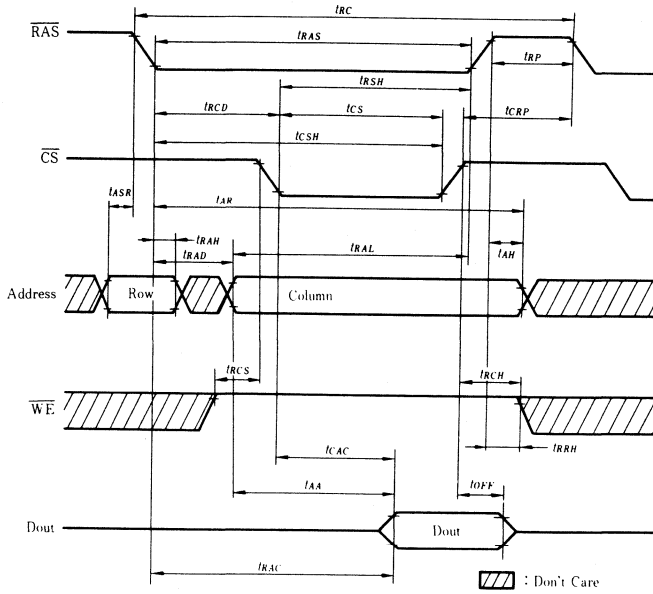
SC Mode Cycle Time on Read-Write	t_{RWSC}	85	–	95	–	115	–	145	–	ns	12
Access Time from Previous \overline{WE}	t_{PWA}	–	80	–	90	–	110	–	140	ns	3, 13
Previous \overline{WE} to Column Address Delay Time	t_{WAD}	20	40	25	45	30	55	35	70	ns	15
Column Address Hold Time to Previous \overline{WE}	t_{PWH}	80	–	90	–	110	–	140	–	ns	

Notes: 1. AC measurements assume $t_T = 5\text{ns}$.

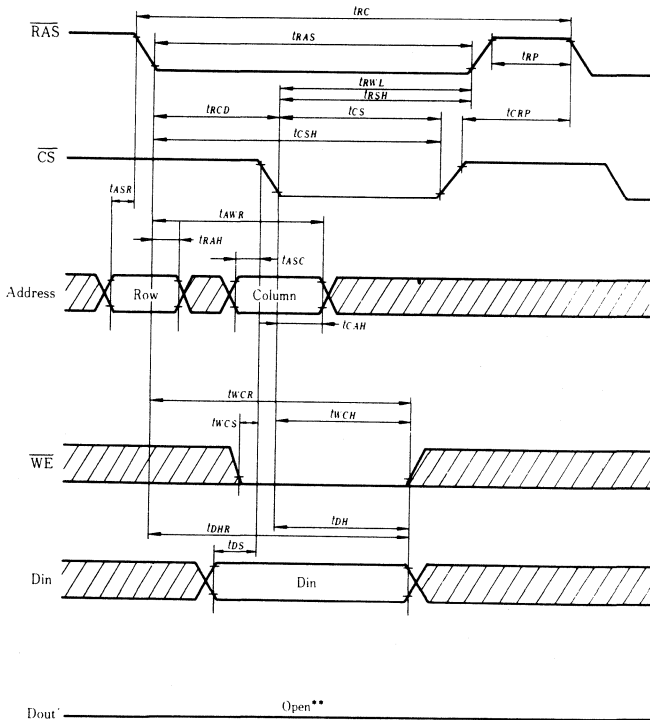
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
- Measured with a load circuit equivalent to 2TTL loads and 100pF.
- Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$, $t_{RAD} \leq t_{RAD}(\text{max})$.
- Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \geq t_{RAD}(\text{max})$.
- $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
- $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
- Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
- Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a reference point only; if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
- t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
- These parameters are referenced to \overline{CS} leading edge in early write cycles and to \overline{WE} leading edge in delayed write or read-modify-write cycles.
- $t_{RWSC}(\text{min}) = t_{AWD}(\text{min}) + t_{WAD}(\text{max}) + t_T$
- Assumes that $t_{WAD} \leq t_{WAD}(\text{max})$. If t_{WAD} is greater than the maximum recommended value shown in this table, t_{PWA} exceeds the value shown.
- Assumes that $t_{WAD} \geq t_{WAD}(\text{max})$.
- Operation with the $t_{WAD}(\text{max})$ limit insures that $t_{PWA}(\text{max})$ can be met, $t_{WAD}(\text{max})$ is specified as a reference point only, if t_{WAD} is greater than the specified $t_{WAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
- t_{AH} defines the time at which the column address hold.
- An initial pause of 100 μs is required after power-up then execute at least 8 initialization cycles.
- At least, 8 \overline{CS} before \overline{RAS} refresh cycle are required before using internal refresh counter.

■ TIMING WAVEFORMS

● Read Cycle

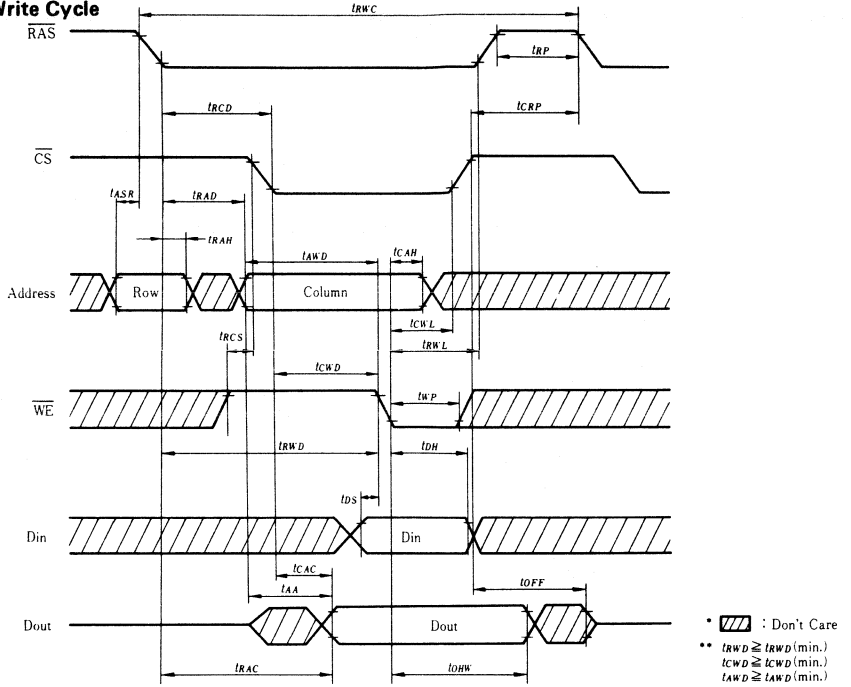


● Write Cycle

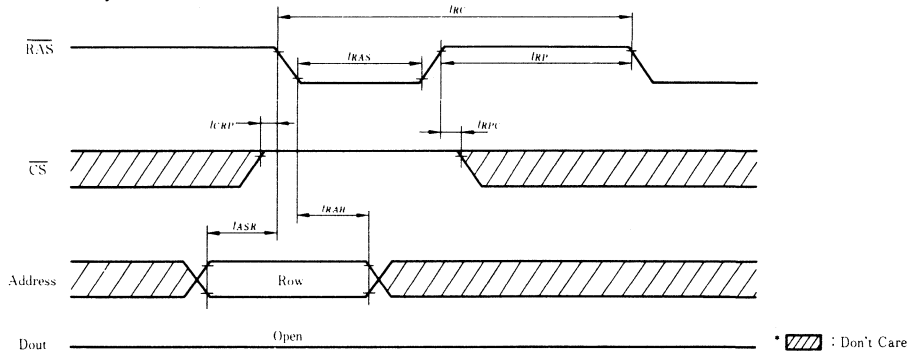


• [Hatched Box] : Don't Care
 •• $t_{WCS} \geq t_{WCS \min}$

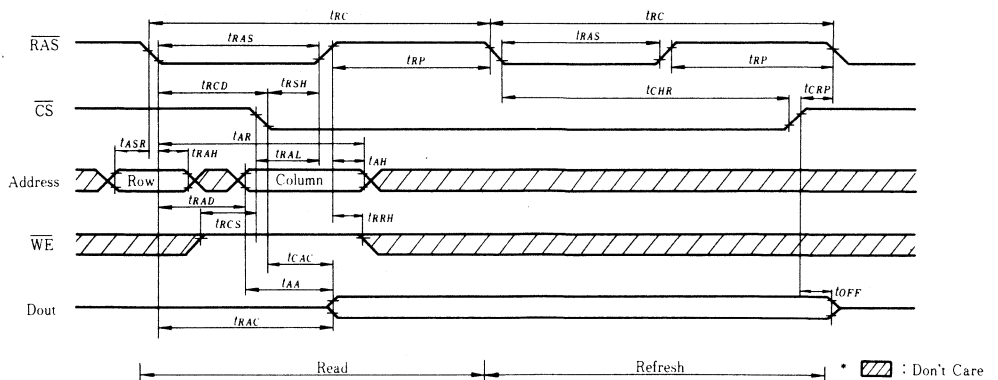
● Read-Modify-Write Cycle



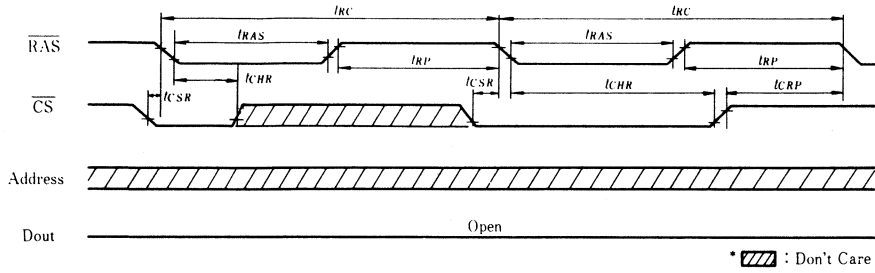
● RAS Only Refresh Cycle



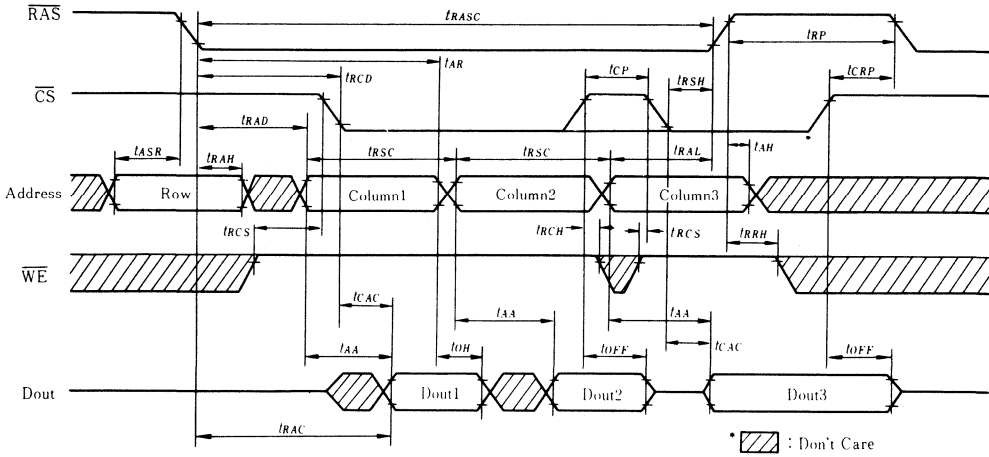
● Hidden Refresh Cycle



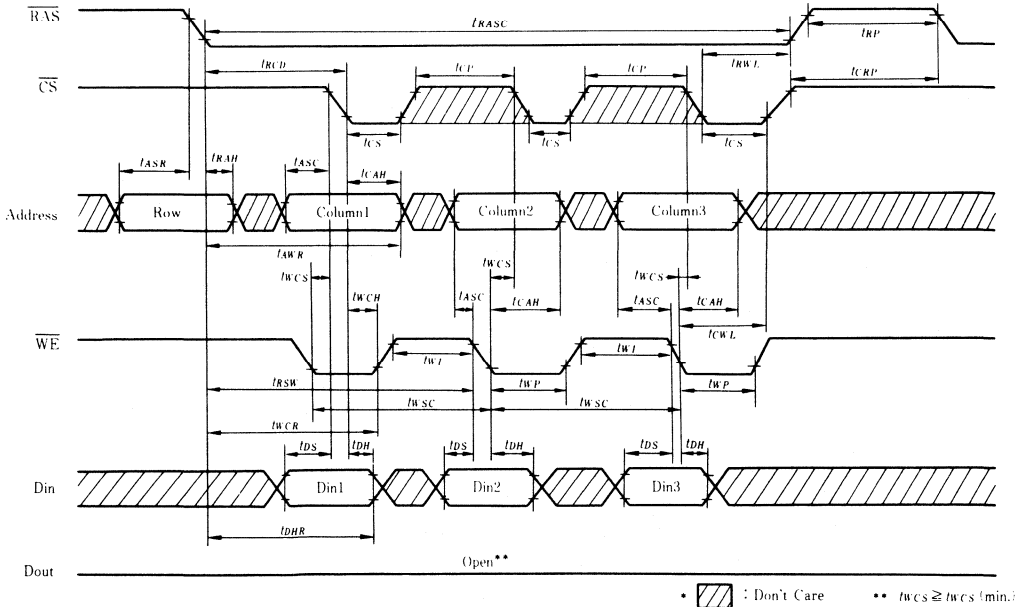
● **$\overline{\text{CS}}$ before $\overline{\text{RAS}}$ Refresh Cycle**



● **Static Column Mode Read Cycle**



● **Static Column Mode Write Cycle**



HM511000 Series, HM511000P Series

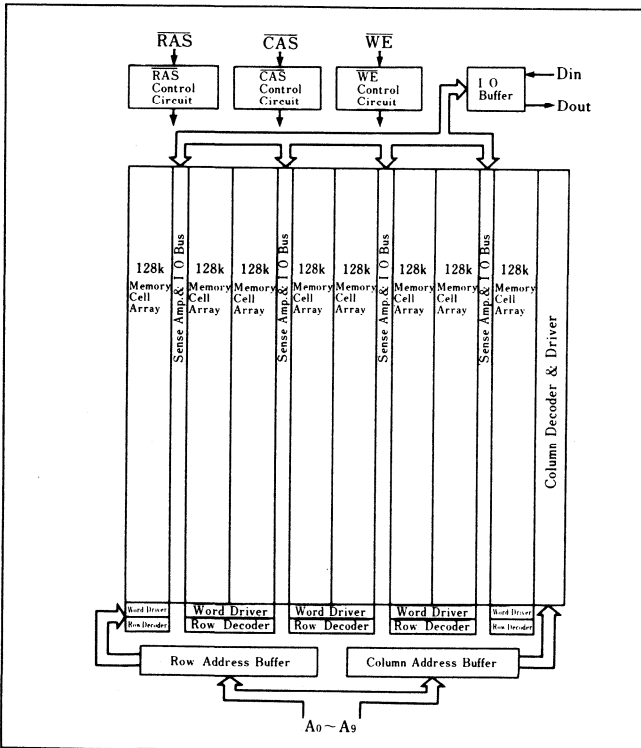
Preliminary

1048576-word X 1-bit Dynamic Random Access Memory

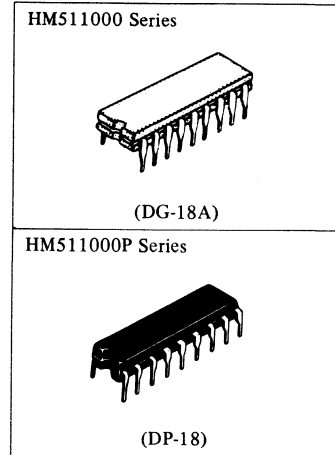
■ FEATURES

- High Speed: Access Time 100/120/150ns (max.)
- Low Power: 300mW (active), 10mW (standby)
- High speed page mode capability
- 512 refresh cycles . . . (8ms)
- 3 variations of refresh: RAS only refresh
CAS before RAS refresh
Hidden refresh

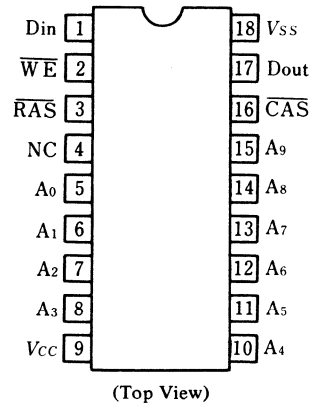
■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.



■ PIN ARRANGEMENT



$A_0 \sim A_9$	Address Inputs
\overline{CAS}	Column Address Strobe
Din	Data In
Dout	Data Out
\overline{RAS}	Row Address Strobe
\overline{WE}	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_8$	Refresh Address Inputs

■ **ABSOLUTE MAXIMUM RATINGS**

Voltage on any pin relative to V_{SS} -1V to +7V
 Operating temperature, T_a (Ambient) 0 to +70°C
 Storage temperature (Plastic) -55 to +125°C
 Storage Temperature Cedip -65 to +150°C
 Power dissipation 1W
 Short circuit output current 50mA

■ **RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to 70°C)**

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	-	6.5	V	1
Input Low voltage	V_{IL}	-2.0	-	0.8	V	1

Notes) 1. All voltages referenced to V_{SS}

■ **DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to +70°C)**

Parameter	Symbol	Test Condition	HM511000/P-10		HM511000/P-12		HM511000/P-15		Unit	Note
			min.	max.	min.	max.	min.	max.		
Operating Current	I_{CC1}	RAS, CAS Cycling: $t_{RC}=\text{min.}$	-	60	-	50	-	40	mA	1
Standby Current	I_{CC2}	RAS, CAS= V_{IH} , TTL Interface	-	2	-	2	-	2	mA	
		Dout=High Impedance CMOS Interface	-	1	-	1	-	1		
Refresh Current	I_{CC3}	RAS only Refresh, $t_{RC}=\text{min.}$	-	50	-	40	-	35	mA	
Standby Current	I_{CC5}	RAS= V_{IH} , CAS= V_{IL} Dout Enable	-	5	-	5	-	5	mA	1
Refresh Current	I_{CC6}	CAS before RAS Refresh, $t_{RC}=\text{min.}$	-	50	-	40	-	35	mA	
Page Mode Supply Current	I_{CC7}	RAS= V_{IL} , CAS Cycling, $t_{PC}=\text{min.}$	-	50	-	45	-	40	mA	
Input Leakage	I_{LI}	$V_{in}=0$ to +7V	-10	10	-10	10	-10	10	μ A	
Output Leakage	I_{LO}	$V_{out}=0$ to +7V, Dout is disabled	-10	10	-10	10	-10	10	μ A	
Output Levels	V_{OH}	$I_{out}=-5\text{mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
	V_{OL}	$I_{out}=4.2\text{mA}$	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ **CAPACITANCE ($V_{CC}=5V \pm 10\%$, $T_a=25^\circ\text{C}$)**

Parameter	Symbol	typ.	max.	Unit	Notes	
Input Capacitance	Address, Data-in	C_{I1}	-	5	pF	1
	Clocks	C_{I2}	-	7		1, 2
Output Capacitance	Data-out	C_o	-	7		

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 2. CAS= V_{IH} to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
 ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^\circ\text{C}$)^{1),10),11)}

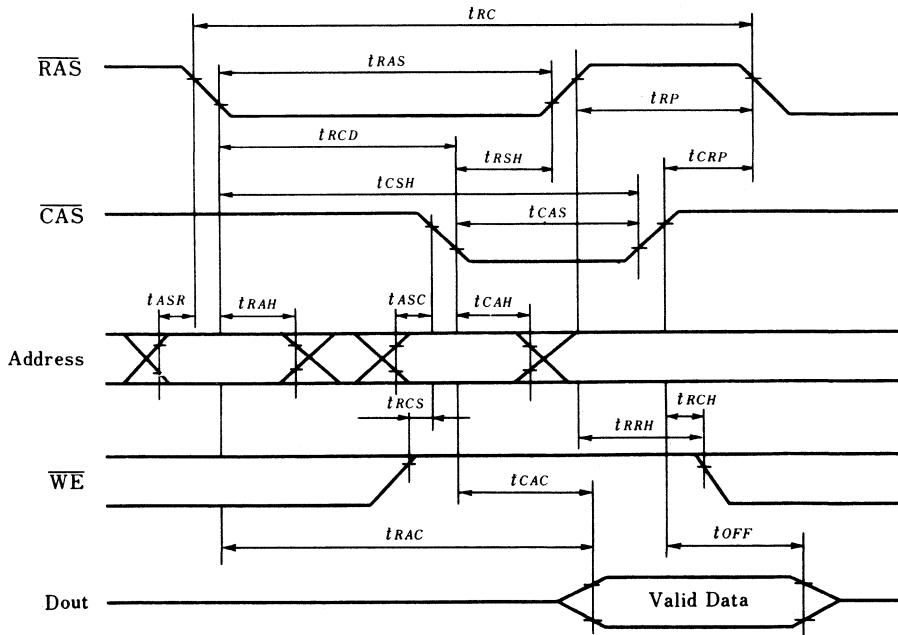
Parameter	Symbol	HM511000/P-10		HM511000/P-12		HM511000/P-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	50	—	60	—	75	ns	2, 3
Output Buffer Turn-off Delay	t_{OFF}	—	25	—	30	—	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Setup Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Setup Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Setup Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Setup Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Setup Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
Read-Write Cycle Time	t_{RWC}	230	—	265	—	310	—	ns	
Read Modify Write Cycle Time	t_{RWS}	140	—	165	—	200	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay	t_{RWD}	100	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t_{CWD}	40	—	50	—	65	—	ns	8
$\overline{\text{CAS}}$ Setup Time	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
Page Mode Read or Write Cycle	t_{PC}	70	—	85	—	105	—	ns	
$\overline{\text{CAS}}$ Precharge Time, Page Cycle	t_{CP}	10	—	15	—	20	—	ns	
Page Mode Read Modify Write Cycle	t_{PCM}	100	—	120	—	145	—	ns	
Page Mode $\overline{\text{CAS}}$ Pulse Width (Read Modify Write Cycle)	t_{CRW}	80	—	95	—	115	—	ns	

Notes)

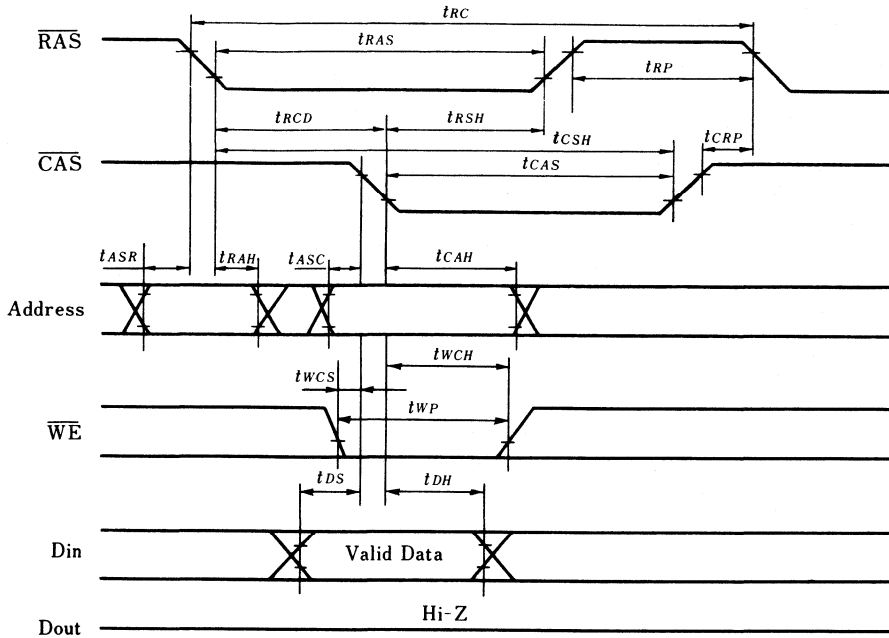
1. AC measurements assume $t_T = 5\text{ns}$.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.

■ TIMING WAVEFORMS

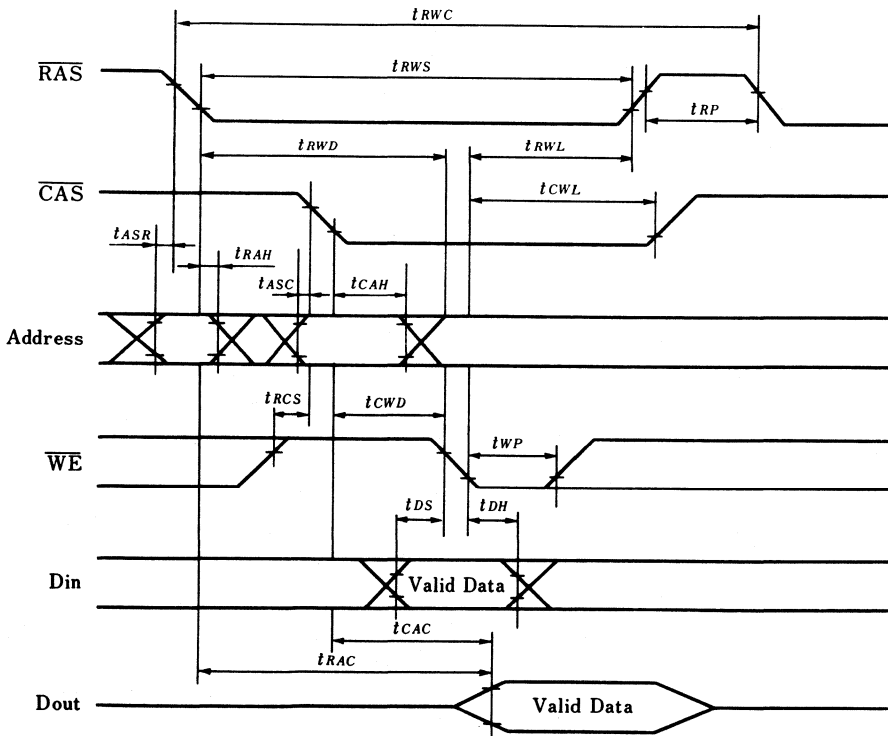
● Read Cycle



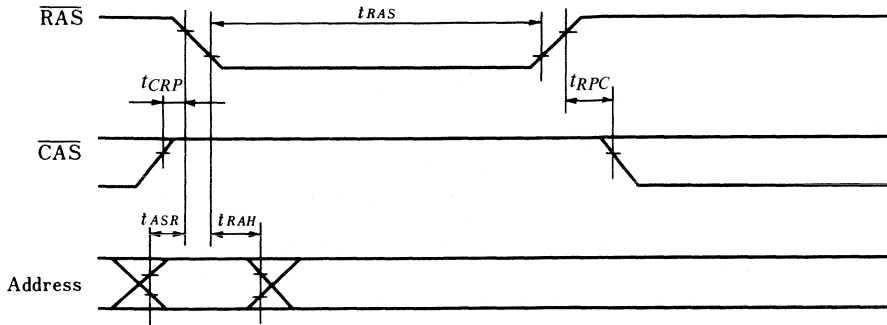
• Write Cycle (Early Write)



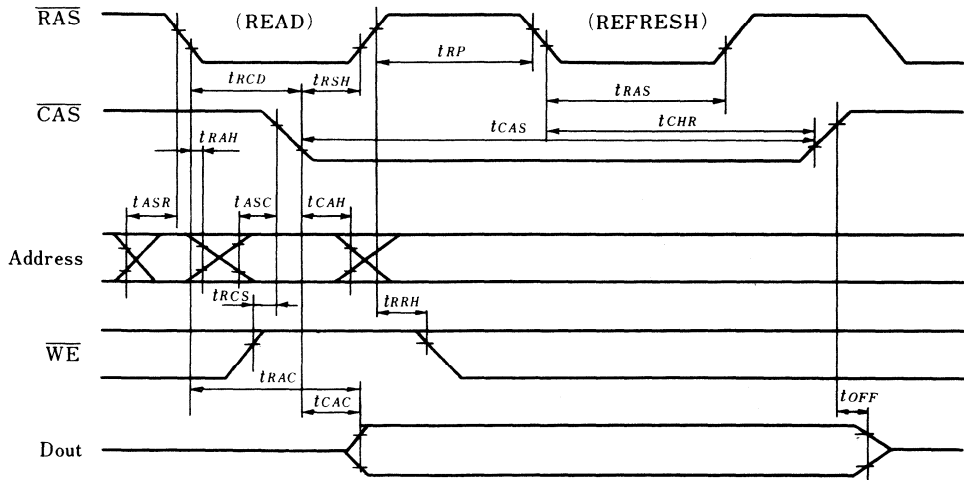
• Read-Modify-Write Cycle



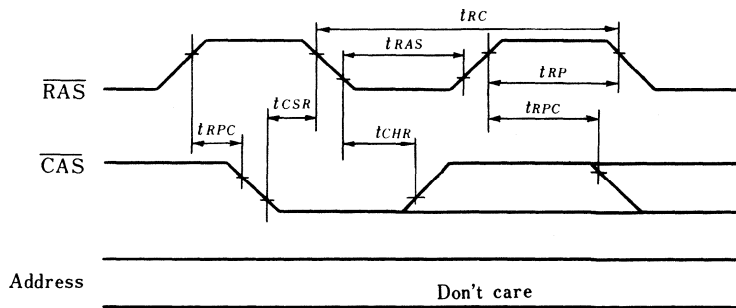
• $\overline{\text{RAS}}$ Only Refresh Cycle



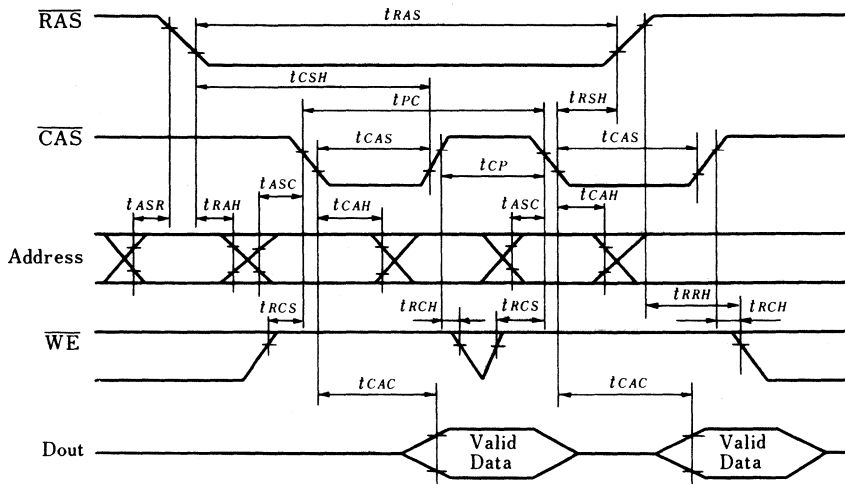
• Hidden Refresh Cycle



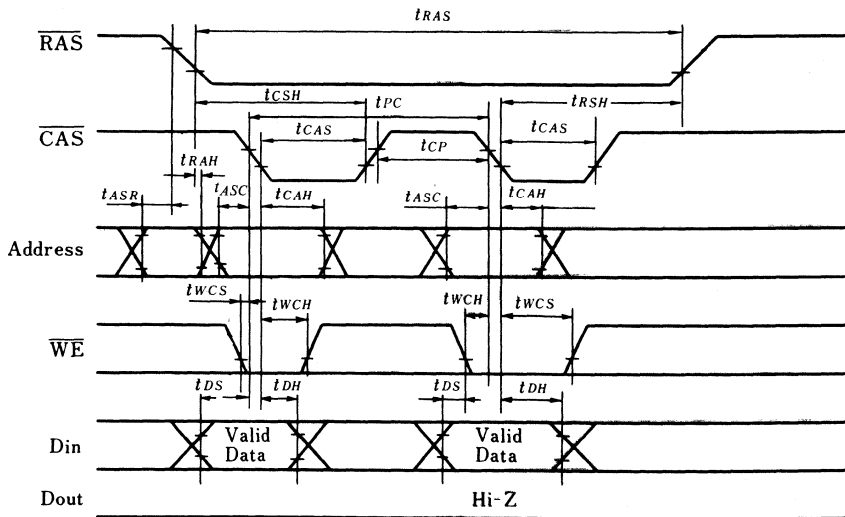
• $\overline{\text{CAS}}$ Before $\overline{\text{RAS}}$ Refresh Cycle



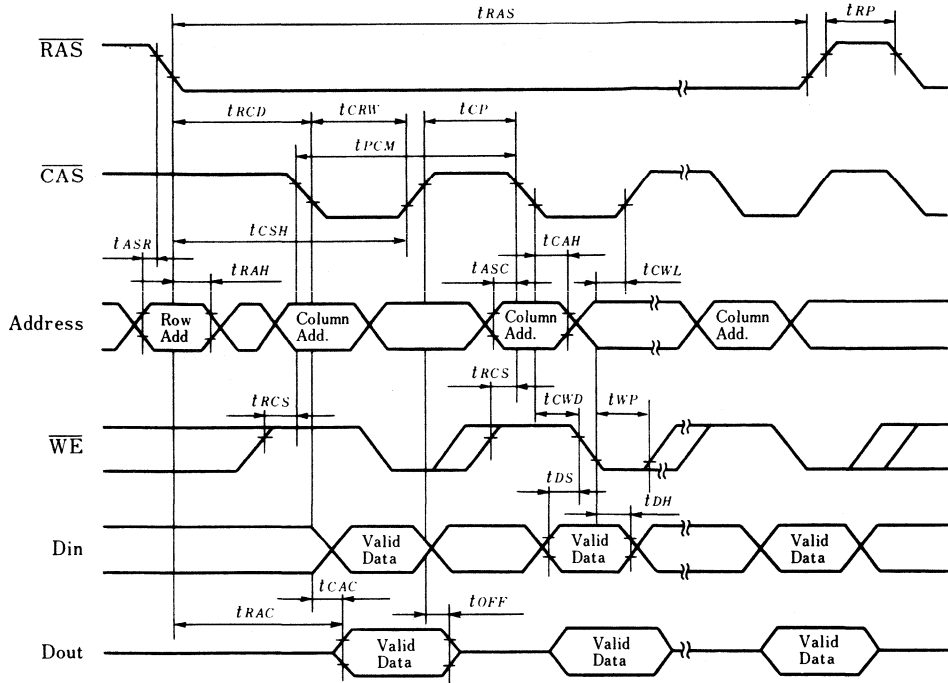
• Page Mode Read Cycle



• Page Mode Write Cycle



• Page Mode Read Modify Write Cycle



HM511001 Series, HM511001P Series

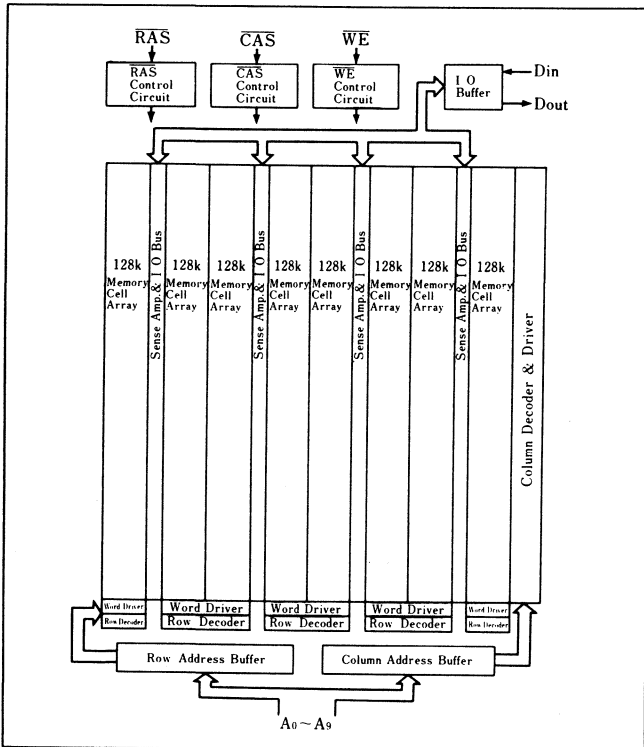
Preliminary

1048576-word X 1-bit Dynamic Random Access Memory

■ FEATURES

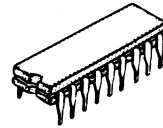
- High Speed: Access Time 100/120/150ns (max.)
- CMOS Low Power: 300mW (active), 10mW (standby)
- Nibble mode capability
- 512 refresh cycles . . . (8ms)
- 3 variations of refresh: $\overline{\text{RAS}}$ only refresh
CAS before $\overline{\text{RAS}}$ refresh
Hidden refresh

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM511001 Series



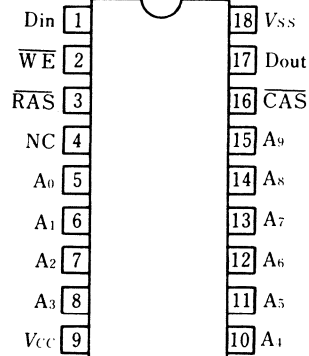
(DG-18A)

HM511001P Series



(DP-18)

■ PIN ARRANGEMENT



(Top View)

$A_0 \sim A_9$	Address Inputs
CAS	Column Address Strobe
Din	Data In
Dout	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_8$	Refresh Address Inputs

■ ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} -1V to +7V
 Operating temperature, T_a (Ambient) 0 to +70°C
 Storage Temperature (Ambient) -65 to +150°C
 Power dissipation 1W
 Short circuit output current 50mA

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High voltage	V_{IH}	2.4	–	6.5	V	1
Input Low voltage	V_{IL}	-2.0	–	0.8	V	1

Notes) 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERIS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to +70°C)

Parameter	Symbol	Test Condition	HM511001-10		HM511001-12		HM511001-15,		Unit	Note
			min.	max.	min.	max.	min.	max.		
Operating Current	I_{CC1}	\overline{RAS} , \overline{CAS} Cycling: $t_{RC} = \text{min.}$	–	60	–	50	–	40	mA	1
Standby Current	I_{CC2}	\overline{RAS} , $\overline{CAS} = V_{IH}$, TTL Interface	–	2	–	2	–	2	mA	
		Dout=High Impedance CMOS Interface	–	1	–	1	–	1	mA	
Refresh Current	I_{CC3}	\overline{RAS} only Refresh, $t_{RC} = \text{min.}$	–	50	–	40	–	35	mA	
Standby Current	I_{CC5}	$\overline{RAS} = V_{IH}$, $\overline{CAS} = V_{IL}$ Dout Enable	–	5	–	5	–	5	mA	1
Refresh Current	I_{CC6}	\overline{CAS} before \overline{RAS} Refresh, $t_{RC} = \text{min.}$	–	50	–	40	–	35	mA	
Nibble Mode Supply Current	I_{CC8}	$\overline{RAS} = V_{IL}$, \overline{CAS} Cycling, $t_{NC} = \text{min.}$	–	50	–	45	–	40	mA	
Input Leakage	I_{LI}	$V_{in} = 0$ to +7V	-10	10	-10	10	-10	10	μA	
Output Leakage	I_{LO}	$V_{out} = 0$ to 7V, Dout is disabled	-10	10	-10	10	-10	10	μA	
Output Levels	V_{OH}	$I_{out} = -5\text{mA}$	2.4	V_{CC}	2.4	V_{CC}	2.4	V_{CC}	V	
	V_{OL}	$I_{out} = 4.2\text{mA}$	0	0.4	0	0.4	0	0.4	V	

Note) 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max. is specified at the output open condition.

■ CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^\circ\text{C}$)

Parameter		Symbol	typ.	max.	Unit	Notes
Input Capacitance	Address, Data-in	C_{I1}	–	5	pF	1
	Clocks	C_{I2}	–	7		1, 2
Output Capacitance	Data-out	C_o	–	7		

Notes) 1. Capacitance measured with Boonton Meter or effective capacitance measuring method.

2. $\overline{CAS} = V_{IH}$ to disable Dout.

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS
 ($V_{CC}=5V \pm 10\%$, $V_{SS} = 0V$, $T_a = 0$ to $+70^\circ C$)^{1),10),11)}

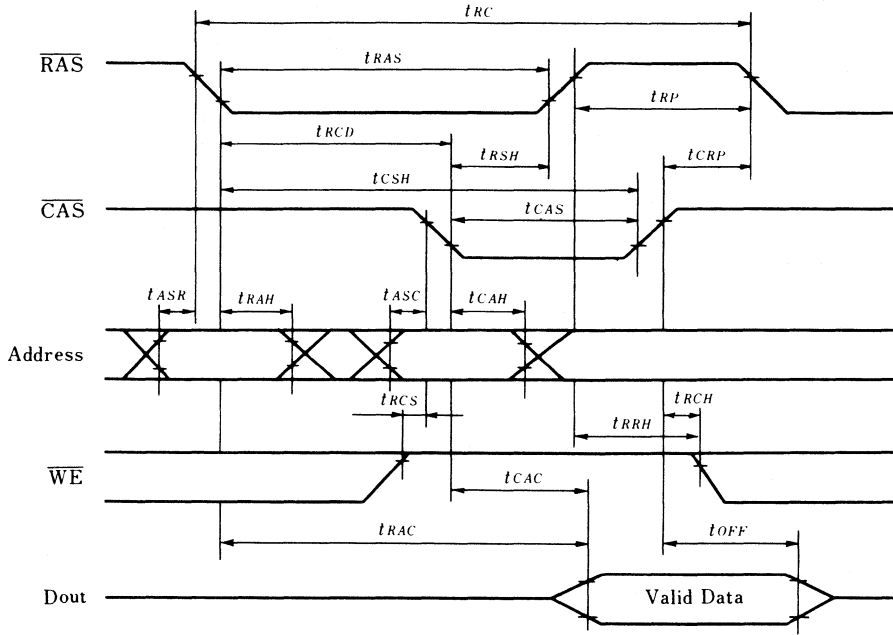
Parameter	Symbol	HM511001-10		HM511001-12		HM511001-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from \overline{RAS}	t_{RAC}	–	100	–	120	–	150	ns	2, 3
Access Time from \overline{CAS}	t_{CAC}	–	50	–	60	–	75	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	–	25	–	30	–	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	190	–	220	–	260	–	ns	
RAS Precharge Time	t_{RP}	80	–	90	–	100	–	ns	
RAS Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
\overline{CAS} Pulse Width	t_{CAS}	50	10000	60	10000	75	10000	ns	
RAS to \overline{CAS} Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
RAS Hold Time	t_{RSH}	50	–	60	–	75	–	ns	
\overline{CAS} Hold Time	t_{CSH}	100	–	120	–	150	–	ns	
\overline{CAS} to RAS Precharge Time	t_{CRP}	10	–	10	–	10	–	ns	
Row Address Setup Time	t_{ASR}	0	–	0	–	0	–	ns	
Row Address Hold Time	t_{RAH}	15	–	15	–	20	–	ns	
Column Address Setup Time	t_{ASC}	0	–	0	–	0	–	ns	
Column Address Hold Time	t_{CAH}	20	–	20	–	25	–	ns	
Write Command Setup Time	t_{WCS}	0	–	0	–	0	–	ns	8
Write Command Hold Time	t_{WCH}	25	–	25	–	30	–	ns	
Write Command Pulse Width	t_{WP}	15	–	20	–	25	–	ns	
Write Command to \overline{RAS} Lead Time	t_{RWL}	35	–	40	–	45	–	ns	
Write Command to \overline{CAS} Lead Time	t_{CWL}	35	–	40	–	45	–	ns	
Data-in Setup Time	t_{DS}	0	–	0	–	0	–	ns	9
Data-in Hold Time	t_{DH}	25	–	25	–	30	–	ns	8, 9
Read Command Setup Time	t_{RCS}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to \overline{CAS}	t_{RCH}	0	–	0	–	0	–	ns	
Read Command Hold Time referenced to \overline{RAS}	t_{RRH}	10	–	10	–	10	–	ns	
Refresh Period	t_{REF}	–	8	–	8	–	8	ms	
Read-Write Cycle Time	t_{RWC}	230	–	265	–	310	–	ns	
Read Modify Write Cycle Time	t_{RWS}	140	–	165	–	200	–	ns	
\overline{RAS} to \overline{WE} Delay	t_{RWD}	100	–	120	–	150	–	ns	
\overline{CAS} to \overline{WE} Delay	t_{CWD}	40	–	50	–	65	–	ns	8
\overline{CAS} Setup Time	t_{CSR}	10	–	10	–	10	–	ns	
\overline{CAS} Hold Time (\overline{CAS} before \overline{RAS} Refresh)	t_{CHR}	20	–	25	–	30	–	ns	
RAS Precharge to \overline{CAS} Hold Time	t_{RPC}	10	–	10	–	10	–	ns	
Nibble Mode Access Time	t_{NAC}	–	30	–	35	–	40	ns	
Nibble Mode Cycle Time	t_{NC}	50	–	55	–	65	–	ns	
Nibble Mode \overline{CAS} Precharge Time	t_{NCP}	10	–	10	–	15	–	ns	
Nibble Mode \overline{CAS} Pulse Width	t_{NCA}	30	–	35	–	40	–	ns	
Nibble Mode RAS Hold Time	t_{NRSH}	40	–	50	–	65	–	ns	

Notes)

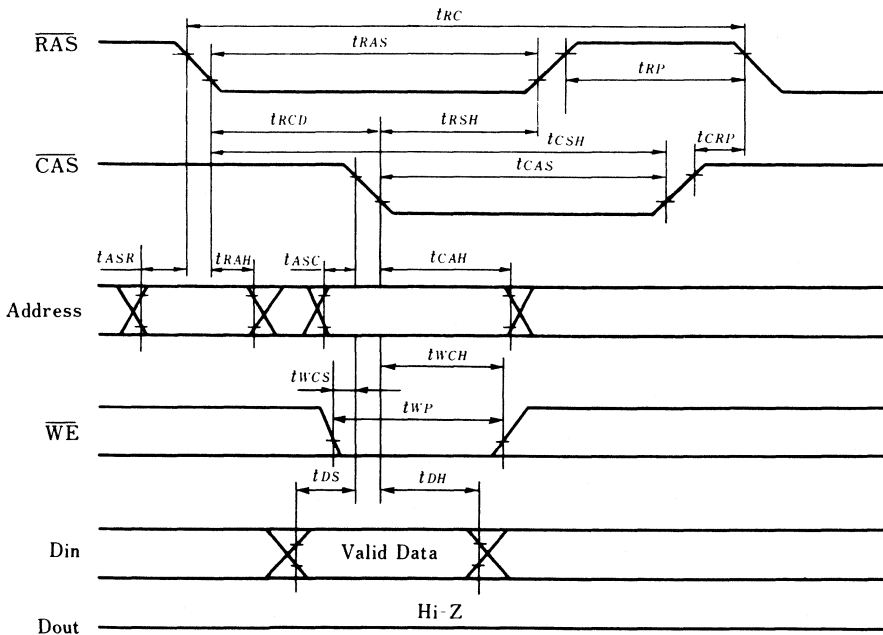
1. AC measurements assume $t_T = 5\text{ns}$.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
10. An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.

■ TIMING WAVEFORMS

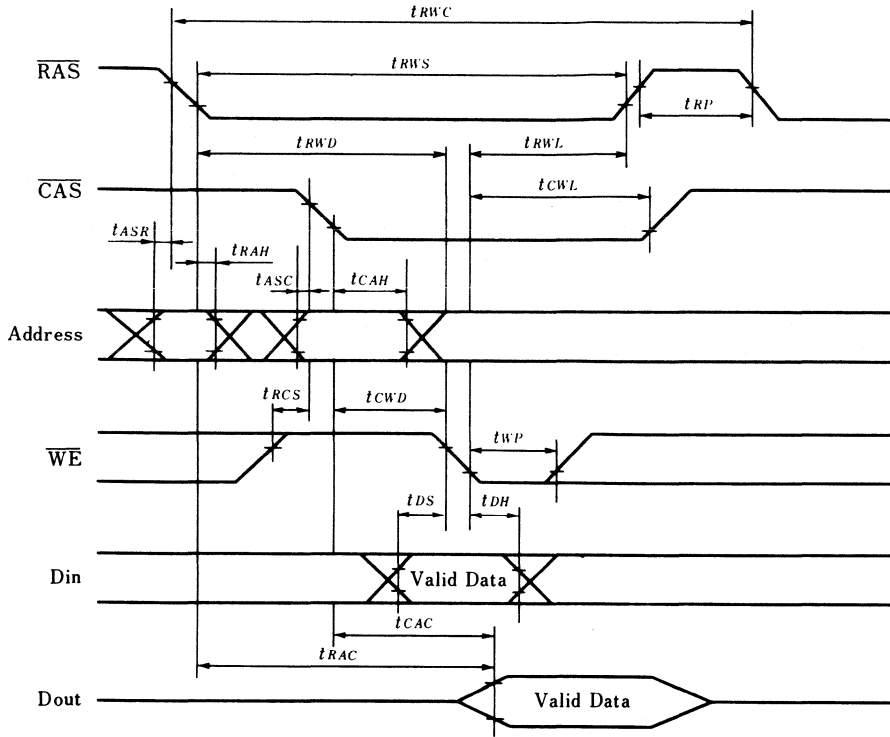
● Read Cycle



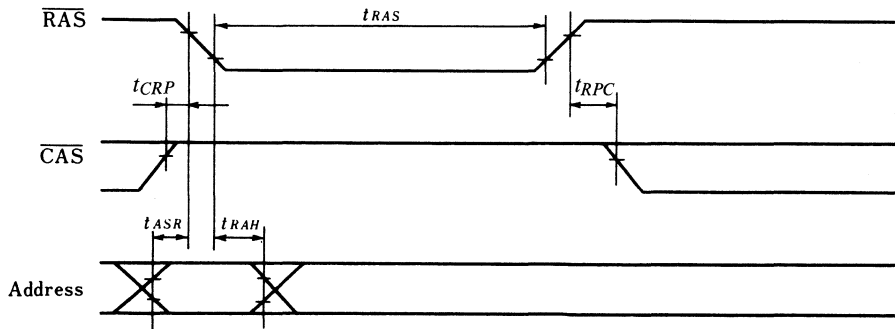
● Write Cycle (Early Write)



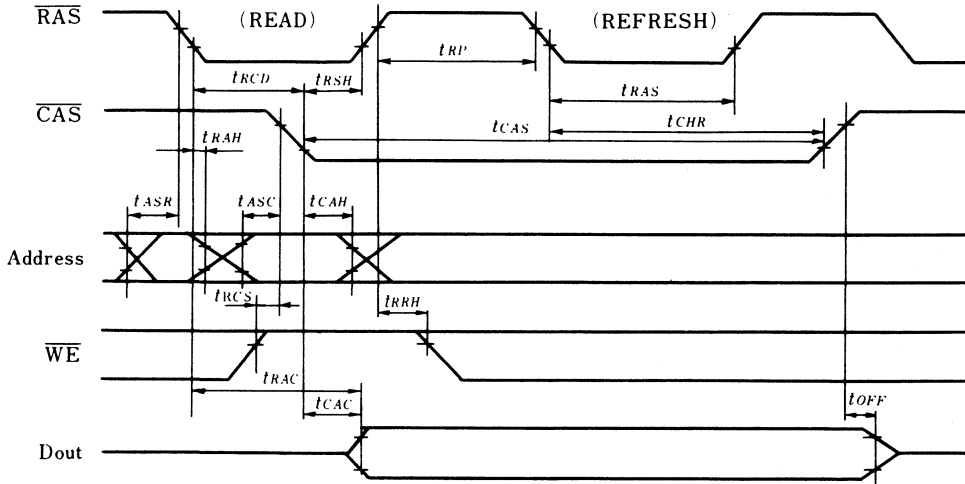
• Read-Modify-Write Cycle



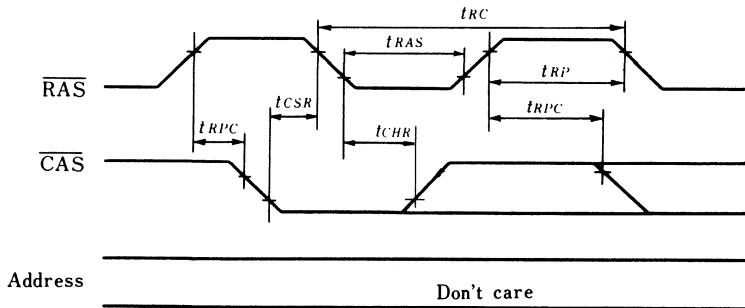
• $\overline{\text{RAS}}$ Only Refresh Cycle



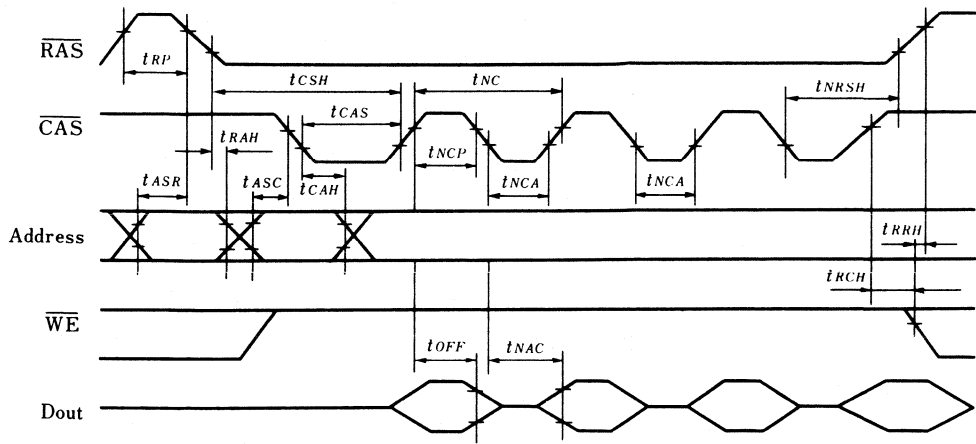
• Hidden Refresh Cycle



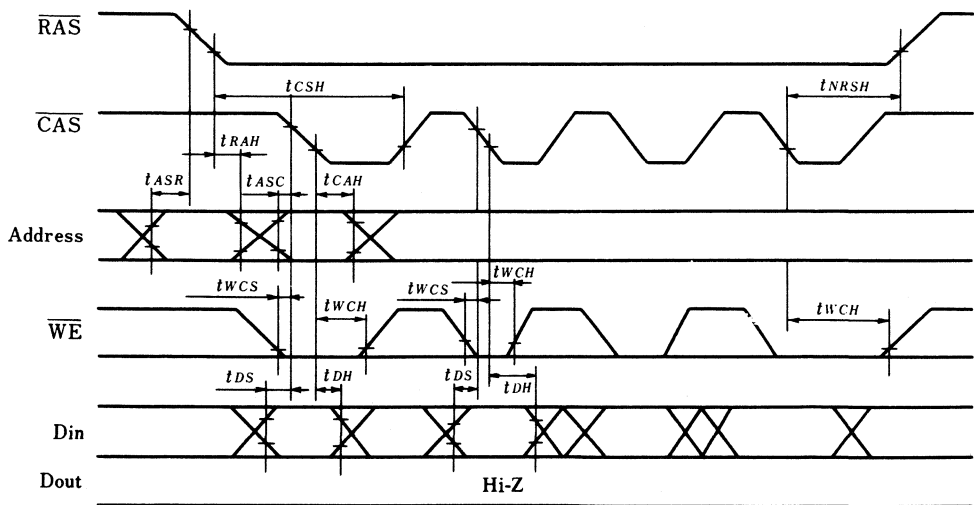
• \overline{CAS} Before \overline{RAS} Refresh Cycle



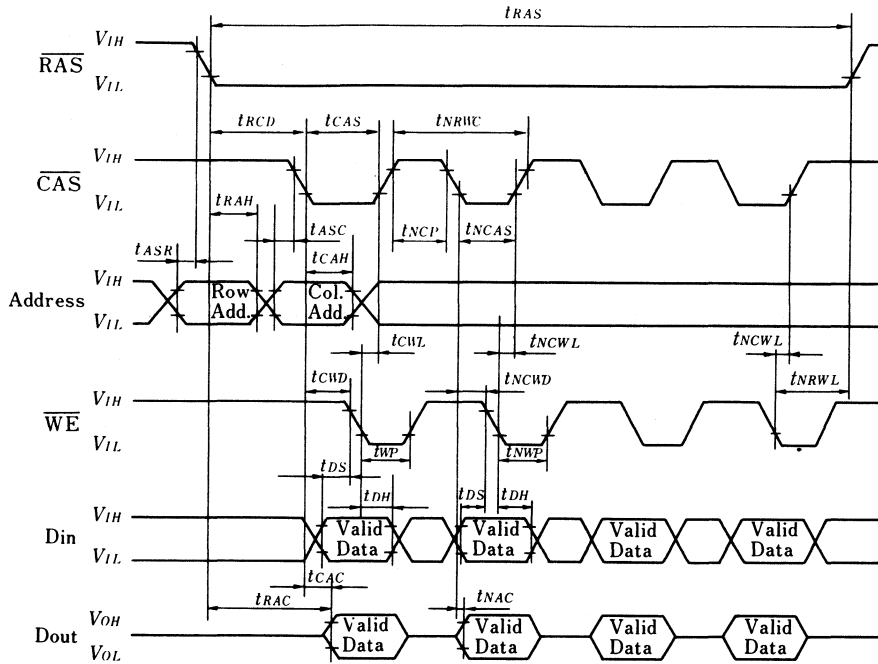
• Nibble Mode Read Cycle



• Nibble Mode Write Cycle



• Nibble Mode Read Modify Write Cycle



HM511002 Series, HM511002P Series

Preliminary

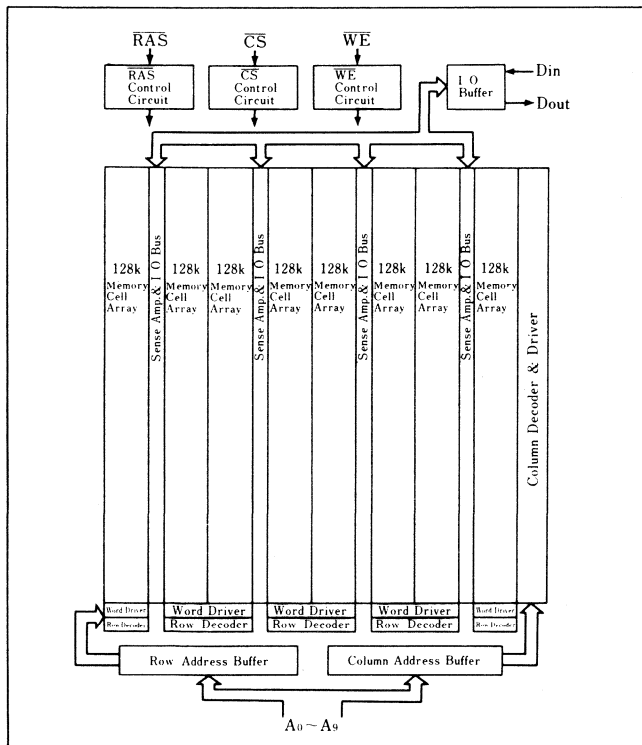
1048576-word x 1-bit Dynamic Random Access Memory

FEATURES

- Single 5V ($\pm 10\%$)
- High speed: Access Time 100ns/120ns/150ns
- CMOS Low Power: 300mW active, 10mW standby
- Static Column mode
- 512 refresh cycles – (8ms)
- 3 variations of refresh

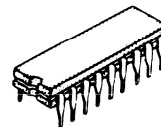
RAS only refresh
CS before RAS refresh
Hidden refresh

BLOCK DIAGRAM



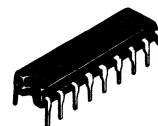
Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

HM511002 Series



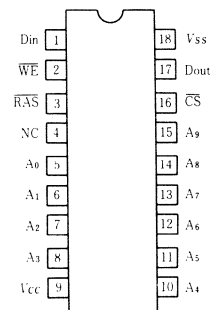
(DG-18A)

HM511002P Series



(DP-18B)

PIN ARRANGEMENT



(Top View)

A0 – A9	Address Inputs
CS	Chip Select
D _{in}	Data In
D _{out}	Data Out
RAS	Row Address Strobe
WE	Read/Write Input
V _{CC}	Power (+5V)
V _{SS}	Ground
A0 – A8	Refresh Address Inputs

■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} : -1V to +7V
 Operating temperature, T_a (Ambient): 0°C to +70°C
 Storage temperature (Ambient):
 -65°C to +150°C (Cerdip)
 -55°C to +125°C (Plastic)
 Power dissipation: 1W
 Short circuit output current: 50mA

■RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Parameter	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input High Voltage	V_{IH}	2.4	-	6.5	V
Input Low Voltage	V_{IL}	-2.0	-	0.8	V

Notes: All voltages referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to +70°C, $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	min	max	Unit	Notes	
Operating current	I_{CC1}	-	40	mA	1	
			50			
			60			
Standby current	I_{CC2}	-	2	mA	TTL Interface	
			1		CMOS Interface	
Refresh current	I_{CC3}	-	35	mA	RAS only Refresh	
			40			
			50			
Standby current (D_{out} Enable, $\overline{RAS} = V_{IH}$, $CS = V_{IL}$)	I_{CC5}	-	5	mA	1	
Refresh current	I_{CC6}	-	35	mA	CS before RAS Refresh	
			40			
			50			
Operating current	I_{CC9}	-	T.B.D.	mA	Static Column mode	
						$t_{RCs}, t_{wCS} = 65ns$
						$t_{RCs}, t_{wCS} = 55ns$
Input leakage $0 < V_{in} < 7V$	I_{LI}	-10	10	μA		
Output leakage $0 < V_{out} < 7V$	I_{LO}	-10	10	μA	D_{out} is disabled	
Output levels High	I_{OH}	2.4	V_{CC}	V		
						$I_{out} = -5mA$
Low	I_{OL}	0	0.4	V		
					$I_{out} = 4.2mA$	

■AC ELECTRICAL CHARACTERISTICS

Symbol	Parameter	typ.	max.	Unit	Notes
C_{11}	Address, Data-in	-	5	pF	2
C_{12}	Clocks, Data-out	-	7	pF	2, 3

Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 3. $CS = V_{IH}$ to disable D_{out} .

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 10\%$)

Parameter	Symbol	HM511002-10		HM511002-12		HM511002-15		Unit	Notes
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
RAS Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
RAS Pulse Width	t_{RAS}	100	10000	120	10000	150	10000	ns	
$\overline{\text{CS}}$ Pulse Width	t_{CS}	20	—	25	—	30	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CS}}$ Delay Time	t_{RCD}	25	80	25	95	30	120	ns	8
$\overline{\text{RAS}}$ to Column Address Delay Time	t_{RAD}	20	60	20	70	25	85	ns	9
Read RAS Hold Time	t_{RRSH}	20	—	25	—	30	—	ns	
Write RAS Hold Time	t_{WRSH}	50	—	60	—	75	—	ns	
$\overline{\text{CS}}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{\text{CS}}$ to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	7
Refresh Period	t_{REF}	—	8	—	8	—	8	ms	
Access Time from RAS	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{\text{CS}}$	t_{CAC}	—	20	—	25	—	30	ns	3, 4
Access Time from Address	t_{AA}	—	40	—	50	—	65	ns	3, 5, 14
Column Address Hold Time to $\overline{\text{RAS}}$ on Read	t_{AR}	100	—	120	—	150	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{CS}}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	ns	
Column Address to RAS Lead Time	t_{RAL}	40	—	50	—	65	—	ns	
$\overline{\text{RAS}}$ to Column Address Hold Time	t_{AH}	15	—	15	—	20	—	ns	16
Output Hold Time from Address	t_{OH}	5	—	5	—	5	—	ns	
Output Buffer Turn-off Time	t_{OFF}	0	25	0	30	0	35	ns	6
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Column Address Hold Time to $\overline{\text{RAS}}$ on Write	t_{AWR}	80	—	90	—	110	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	10
Write Command Hold Time	t_{WCH}	20	—	25	—	30	—	ns	
Write Command Hold Time to $\overline{\text{RAS}}$	t_{WCR}	80	—	95	—	115	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{\text{CS}}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	11
Data-in Hold Time	t_{DH}	20	—	25	—	30	—	ns	10, 11
Data-in Hold Time to $\overline{\text{RAS}}$	t_{DHR}	80	—	90	—	110	—	ns	
Read-Write Cycle Time	t_{RWC}	215	—	250	—	295	—	ns	
$\overline{\text{RAS}}$ to $\overline{\text{WE}}$ Delay Time	t_{RWD}	100	—	120	—	150	—	ns	10
$\overline{\text{CS}}$ to $\overline{\text{WE}}$ Delay Time	t_{CWD}	20	—	25	—	30	—	ns	10
Column Address to $\overline{\text{WE}}$ Delay Time	t_{AWD}	40	—	50	—	65	—	ns	10
Output Hold Time from $\overline{\text{WE}}$	t_{OHW}	35	—	40	—	45	—	ns	
$\overline{\text{CS}}$ Set-up Time ($\overline{\text{CS}}$ before $\overline{\text{RAS}}$ Refresh)	t_{CSR}	10	—	10	—	10	—	ns	

(to be continued)

Parameter	Symbol	HM511002-10		HM511002-12		HM511002-15		Unit	Notes
		min.	max.	min.	max.	min.	max.		
CS Hold Time (CS before RAS Refresh)	t_{CHR}	20	—	25	—	30	—	ns	
RAS precharge to CS Hold Time	t_{RPC}	10	—	10	—	10	—	ns	

● SC Mode Cycle ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 10\%$)

Parameter	Symbol	HM511002-10		HM511002-12		HM511002-15		Unit	Notes
		min.	max.	min.	max.	min.	max.		
SC Mode Cycle Time on Read	t_{RSC}	45	—	55	—	70	—	ns	
SC Mode Cycle Time on Write	t_{WSC}	45	—	55	—	70	—	ns	
SC Mode RAS Pulse Width	t_{RASC}	60	140000	70	140000	90	140000	ns	
RAS to Second WE Delay Time	t_{RSW}	105	—	125	—	155	—	ns	
CS Precharge Time	t_{CP}	10	—	15	—	15	—	ns	
Write Invalid Time	t_{WI}	10	—	15	—	15	—	ns	

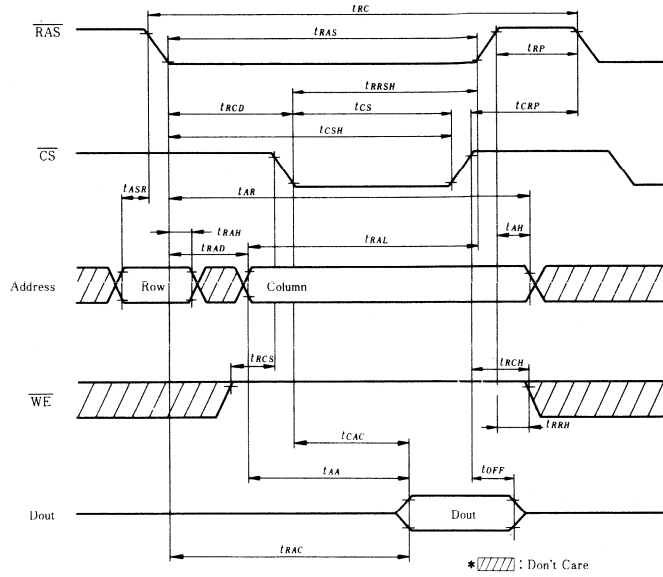
● SC Mode Read-Modify-Write and Mixed Cycle ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 10\%$)

Parameter	Symbol	HM511002-10		HM511002-12		HM511002-15		Unit	Notes
		min.	max.	min.	max.	min.	max.		
SC Mode Cycle Time on Read-Write	t_{RWSC}	85	—	105	—	135	—	ns	12
Access Time from Previous WE	t_{PWA}	—	80	—	100	—	130	ns	3, 13
Previous WE to Column Address Delay Time	t_{WAD}	25	40	25	50	30	65	ns	15
Column Address Hold Time to Previous WE	t_{PWH}	80	—	100	—	130	—	ns	

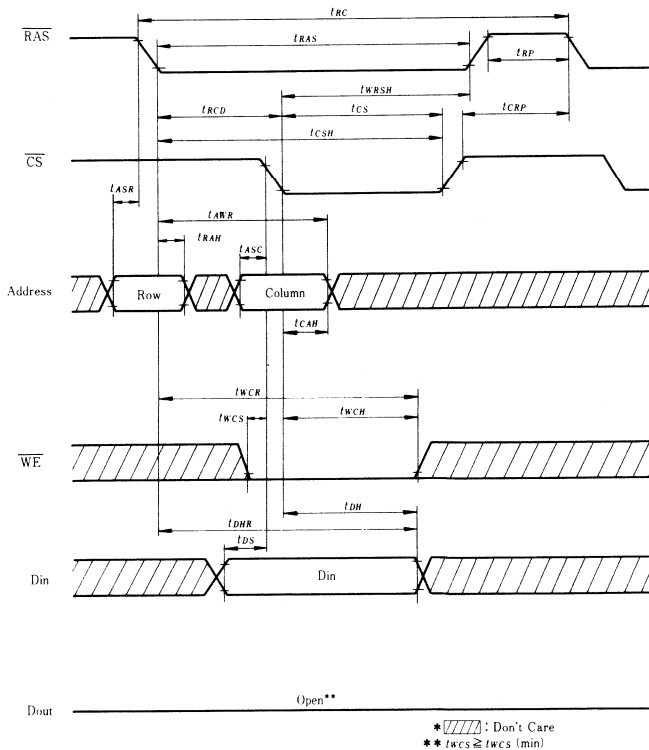
- Notes:
- AC measurements assume $t_T = 5\text{ns}$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$. If t_{RCD} or t_{RAD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2TTL loads and 100pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$, $t_{RAD} \leq t_{RAD}(\text{max})$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$ and $t_{RAD} \leq t_{RAD}(\text{max})$.
 - $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
 - Operation with the $t_{RAD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RAD}(\text{max})$ is specified as a Reference point only, if t_{RAD} is greater than the specified $t_{RAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 - t_{WCS} , t_{RWD} , t_{CWD} and t_{AWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{RWD} \geq t_{RWD}(\text{min})$, $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{AWD} \geq t_{AWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
 - These parameters are referenced to $\overline{\text{CS}}$ leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 - $t_{RWSC}(\text{min}) = t_{AWD}(\text{min}) + t_{WAD}(\text{max}) + t_T$.
 - Assumes that $t_{WAD} \leq t_{WAD}(\text{max})$. If t_{WAD} is greater than the maximum recommended value shown in this table t_{PWA} exceeds the value shown.
 - Assumes that $t_{WAD} \geq t_{WAD}(\text{max})$.
 - Operation with the $t_{WAD}(\text{max})$ limit insures that $t_{PWA}(\text{max})$ can be met, $t_{WAD}(\text{max})$ is specified as a Reference point only, if t_{WAD} is greater than the specified $t_{WAD}(\text{max})$ limit, then access time is controlled exclusively by t_{AA} .
 - t_{AH} defines the time at which the column address hold.
 - An initial pause of $100\mu\text{s}$ is required after power-up then execute at least 8 initialization cycles.
 - At least, 8 CS before RAS refresh cycle are required before using internal refresh counter.

TIMING WAVEFORMS

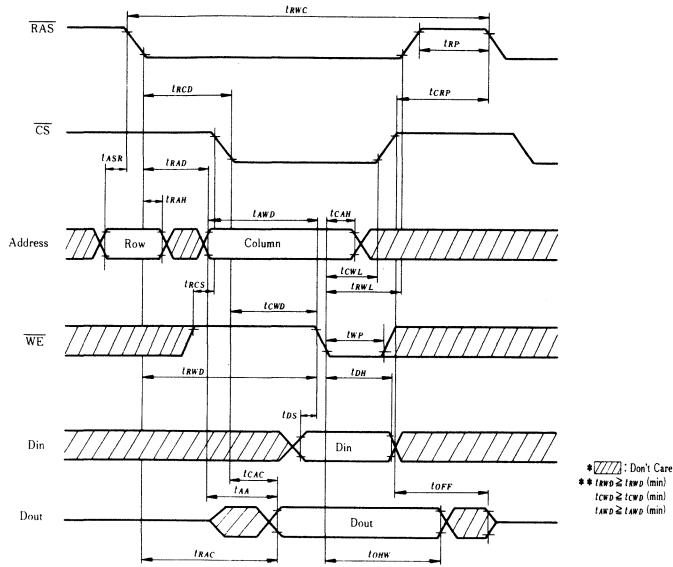
● Read Cycle



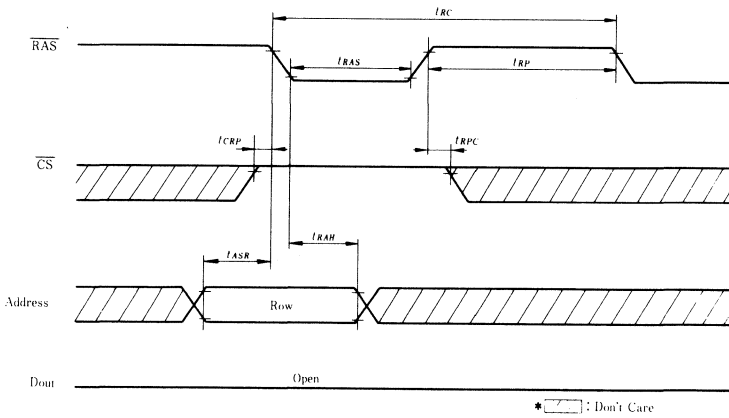
● Write Cycle



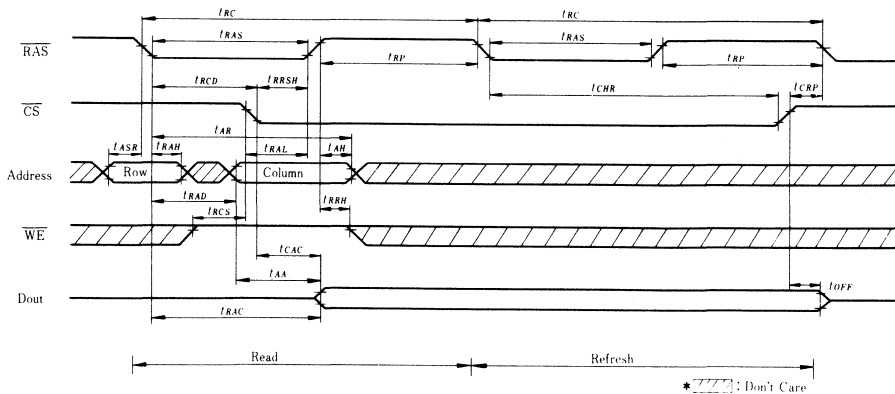
● Read Modify Write Cycle



● RAS Only Refresh Cycle



● Hidden Refresh Cycle



MULTI-PORT DYNAMIC RAM

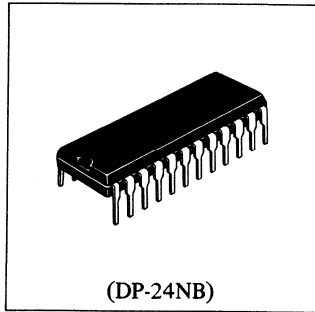
HM53461P Series

Preliminary

65,536-word x 4 bit Multi Port Dynamic Random Access Memory

The HM53461P is a 262, 144 bit multi port memory equipped with a 64k word x 4 bit Dynamic RAM port and a 256 word x 4 bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024 bit data register through a 256 word x 4 bit serial read or write access control. In the read data transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved.

Utilizing the Hitachi 2 μ m CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible. The package is a 400mil 24-pin dual-in-line plastic package.

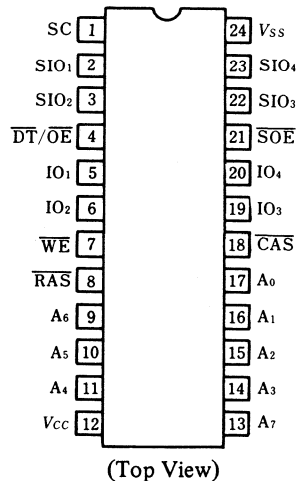


(DP-24NB)

■ FEATURES

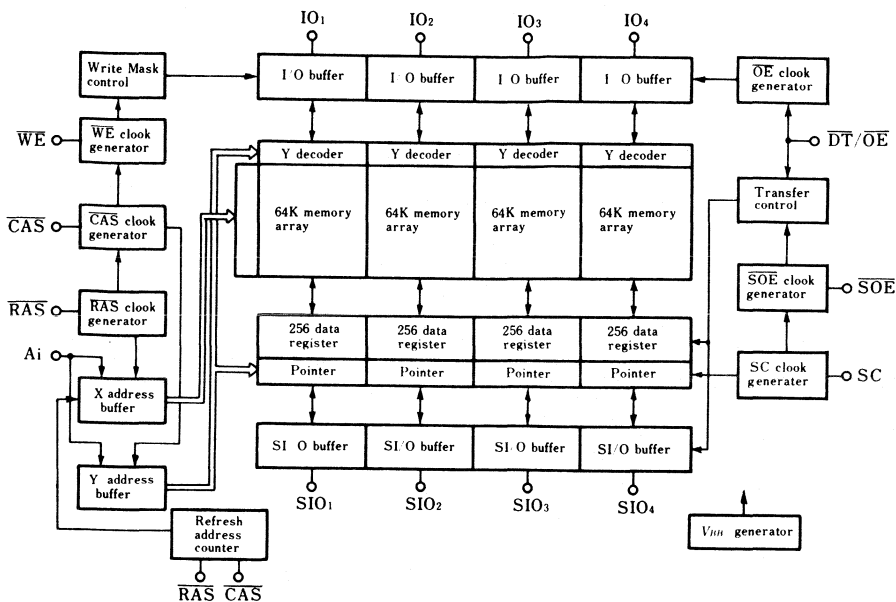
- Multi port organization
(RAM; 64k word x 4 bit and SAM; 256 word x 4 bit)
- 400mil 24-pin dual-in line plastic package
- Double layer polysilicon/polycide n-well CMOS process
- Single 5V ($\pm 10\%$)
- Low power Active RAM; 380mW max.
SAM; 220mW max.
Standby 40mW max.
- Access Time RAM; 100ns/120ns/150ns
SAM; 40ns/ 40ns/ 60ns
- Cycle Time Random read or write cycle time (RAM) 190ns/
220ns/260ns
Serial read or write cycle time (SAM) 40ns/40ns/
60ns
- TTL compatible
- 256 refresh cycles 4ms
- Refresh function $\overline{\text{RAS}}$ only refresh
 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
Hidden refresh
- Data transfer operation (RAM \leftrightarrow SAM)
- Fast serial access operation asynchronous from RAM port
except data transfer cycle
- Real time read transfer capability
- Write mask mode capability

■ PIN ARRANGEMENT



Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} -1V to +7V
- Operating temperature, T_a (Ambient) 0°C to +70°C
- Storage temperature -55°C to +125°C
- Short circuit output current 50mA
- Power dissipation 1W

A ₀ ~A ₄	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
D _{in}	Data In
D _{out}	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
$\overline{\text{WE}}$	Read/Write Input
V _{CC}	Power (+5V)
V _{SS}	Ground
A ₀ ~A ₇	Refresh Address Inputs

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	—	6.5	V
Input Low voltage	V_{IL}	-1.0	—	0.8	V

Note: All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

RAM PORT	Symbol	SAM PORT		HM53461P -10	HM53461P -12	HM53461P -15	Unit
		Standby	Active				
Operating current $\overline{\text{RAS}}$, $\overline{\text{CAS}}$ cycling $t_{RC} = \text{min.}$	I_{CC1}	○	X	70	60	50	mA
	I_{CC7}	X	○	110	100	80	mA
Standby current $\overline{\text{RAS}}$, $\overline{\text{CAS}} = V_{IH}$	I_{CC2}	○	X	7	7	7	mA
	I_{CC8}	X	○	40	40	30	mA
$\overline{\text{RAS}}$ only refresh current $\text{CAS} = V_{IH}$, $\overline{\text{RAS}}$ cycling $t_{RC} = \text{min.}$	I_{CC3}	○	X	60	50	40	mA
	I_{CC9}	X	○	100	90	70	mA
Page mode current $\overline{\text{RAS}} = V_{IL}$, CAS cycling $t_{PC} = \text{min.}$	I_{CC4}	○	X	50	40	35	mA
	I_{CC10}	X	○	90	80	65	mA
CBR refresh current $\overline{\text{RAS}}$ cycling $t_{RC} = \text{min.}$	I_{CC5}	○	X	60	50	40	mA
	I_{CC11}	X	○	100	90	70	mA
Data transfer current $\overline{\text{RAS}}$, CAS cycling $t_{RC} = \text{min.}$	I_{CC6}	○	X	75	65	55	mA
	I_{CC12}	X	○	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{IL}	-10	10	μA
Output leakage	I_{OL}	-10	10	μA
Output high voltage $I_{OH} = -2\text{mA}$	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 4.2\text{mA}$	V_{OL}	—	0.4	V

■ INPUT/OUTPUT CAPACITANCE

Symbol	Parameter	typ.	max.	Unit
Address	CI1	—	5	pF
Clocks	CI2	—	5	pF
I/O, SI/O	CI3	—	7	pF

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{SS}=0\text{V}$)^{1), 10), 11)}

Parameter	Symbol	HM53461P-10		HM53461P-12		HM53461P-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
Read Modify Write Cycle Time	t_{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t_{PC}	70	—	85	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{\text{CAS}}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	100	30000	120	30000	150	30000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	50	30000	60	30000	75	30000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{\text{RAS}}$ Pulse Width (Read Modify Write Cycle)	t_{RWS}	170	—	200	—	245	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{\text{CAS}}$ Set-up Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time ($\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{\text{OE}}$	t_{OAC}	—	25	—	30	—	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{\text{OE}}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{\text{OE}}$ Hold Time referenced to $\overline{\text{WE}}$	t_{OEH}	10	—	15	—	20	—	ns	
Data-in to $\overline{\text{CAS}}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{\text{OE}}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Delay Time	t_{ORD}	25	—	30	—	40	—	ns	

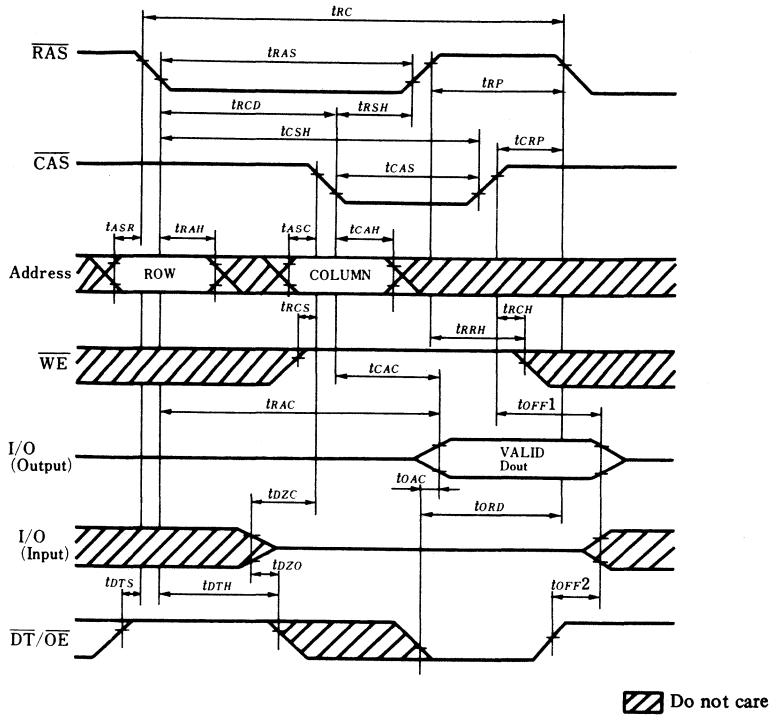
(to be continued)

Parameter	Symbol	HM53461P-10		HM53461P-12		HM53461P-15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Serial Clock Cycle Time	t_{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access Time from \overline{SOE}	t_{SEA}	—	25	—	30	—	40	ns	10
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from \overline{SOE}	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Set-up Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
\overline{DT} to \overline{RAS} Set-up Time	t_{DTS}	0	—	0	—	0	—	ns	
\overline{DT} to \overline{RAS} Hold Time(Read Data Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
\overline{DT} to \overline{RAS} Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
\overline{DT} to \overline{CAS} Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to \overline{DT} Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to \overline{DT} Hold Time	t_{SDH}	20	—	25	—	30	—	ns	
\overline{DT} to \overline{RAS} Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
\overline{WE} to \overline{RAS} Set-up Time	t_{WS}	0	—	0	—	0	—	ns	
\overline{WE} to \overline{RAS} Hold Time	t_{WH}	15	—	15	—	20	—	ms	
I/O to \overline{RAS} Set-up Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to \overline{RAS} Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn off Delay from \overline{RAS}	t_{SRZ}	10	50	10	60	10	75	ns	
\overline{SC} to \overline{RAS} Set-up Time	t_{SRS}	30	—	40	—	45	—	ns	
\overline{RAS} to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from \overline{RAS}	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to \overline{DT} Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
\overline{SOE} to \overline{RAS} Set-up Time	t_{ES}	0	—	0	—	0	—	ns	
\overline{SOE} to \overline{RAS} Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Read Enable Set-up Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	40	—	60	—	ns	
Serial Write Disable Set-up Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	40	—	60	—	ns	
\overline{DT} to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

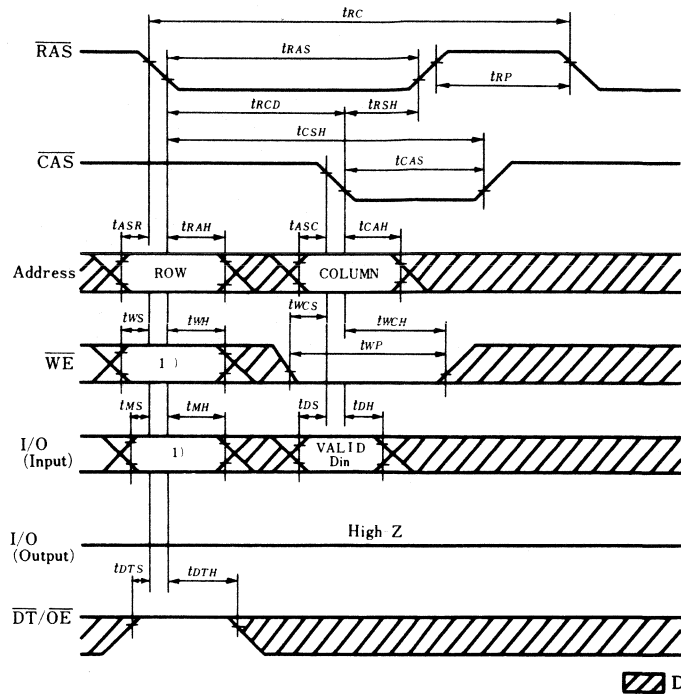
Notes)

1. AC measurements assume $t_T=5\text{ns}$.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycle and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50pF.
11. An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.

■ WAVE FORMS
● READ CYCLE

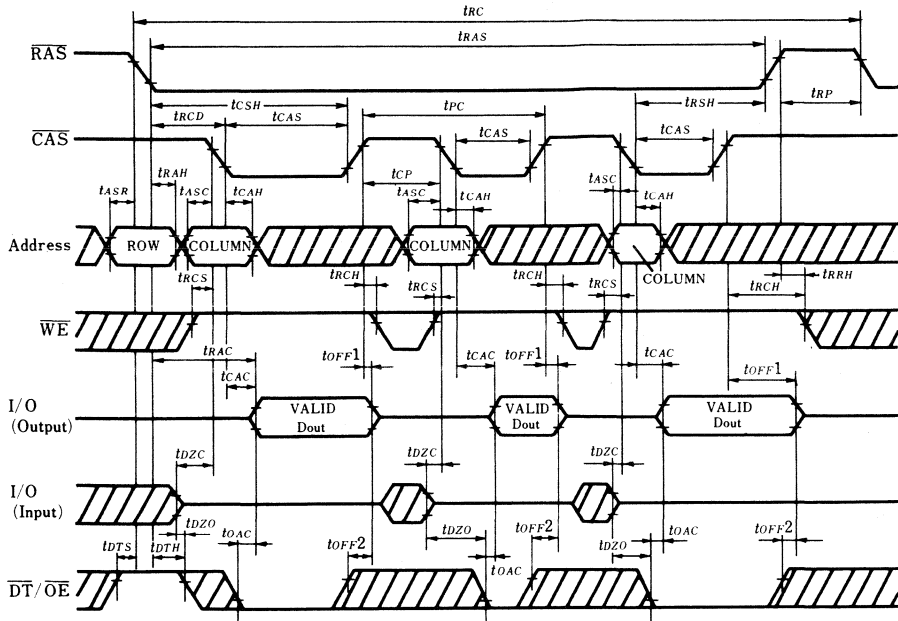


● EARLY WRITE CYCLE



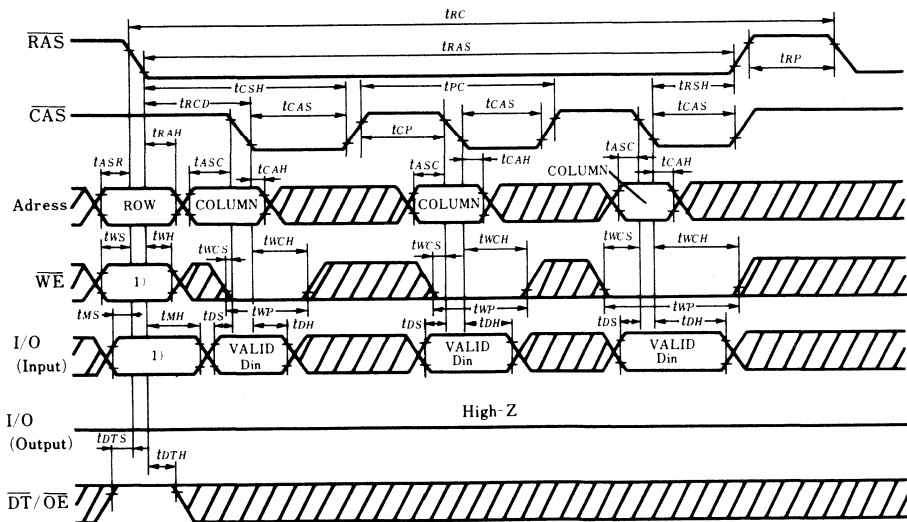
Note 1) When \overline{WE} is "H" level, the all data on the I/O can be written into the cell.
 When \overline{WE} is "L" level, the data on the I/O are not written except for when I/O is 'high' at the falling edge of \overline{RAS} .

● PAGE MODE READ CYCLE



▨ Do not care

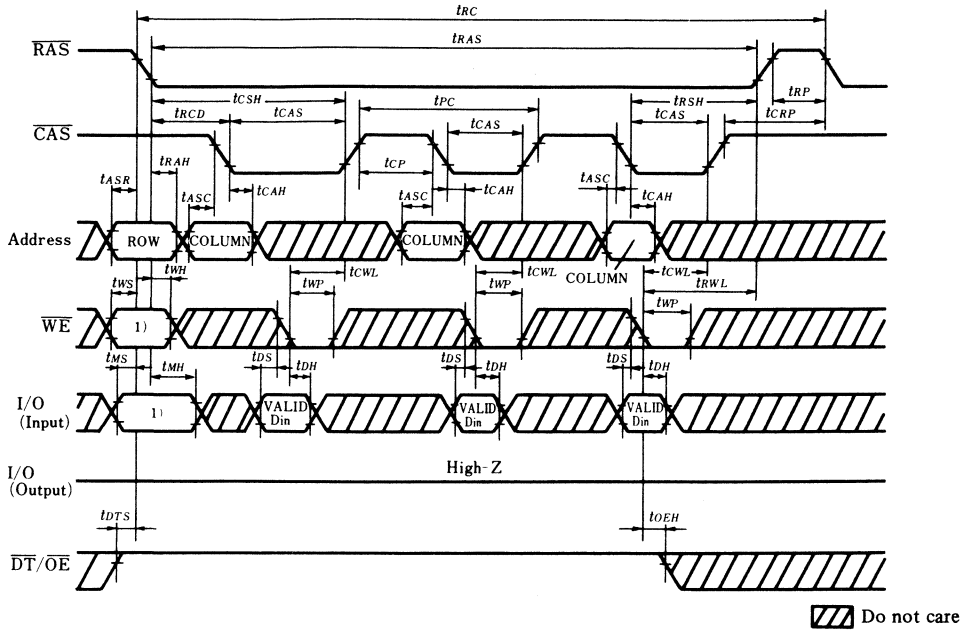
● PAGE MODE WRITE CYCLE (Early Write)



▨ Do not care

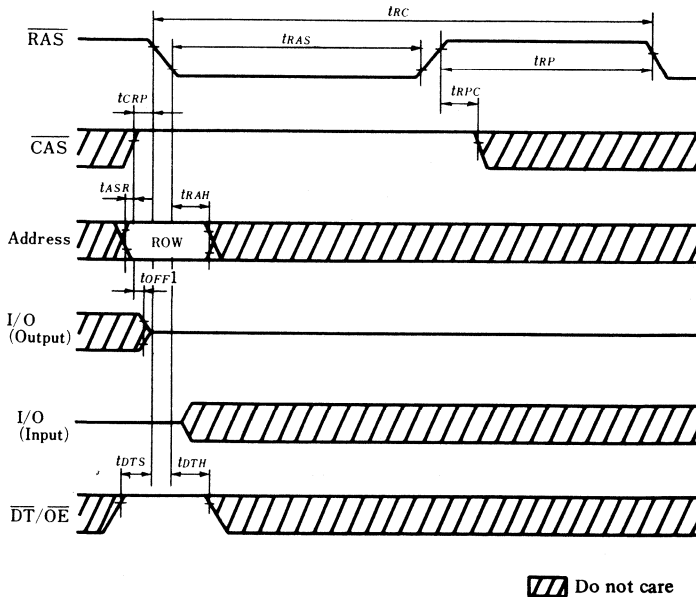
Note 1) When \overline{WE} is "H" level, all the data on I/O1-4 can be written into the memory cell.
 When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of \overline{RAS} .

● PAGE MODE WRITE CYCLE (Delayed Write)

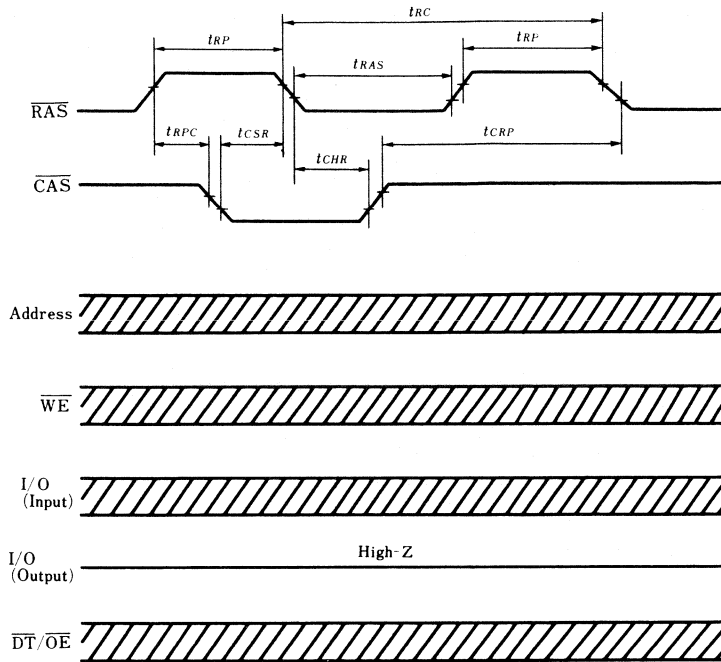


Note 1) When \overline{WE} is "H" level, all the data on I/O1-4 can be written into the memory cell.
 When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O="H" at the falling edge of \overline{RAS} .

● \overline{RAS} ONLY REFRESH CYCLE

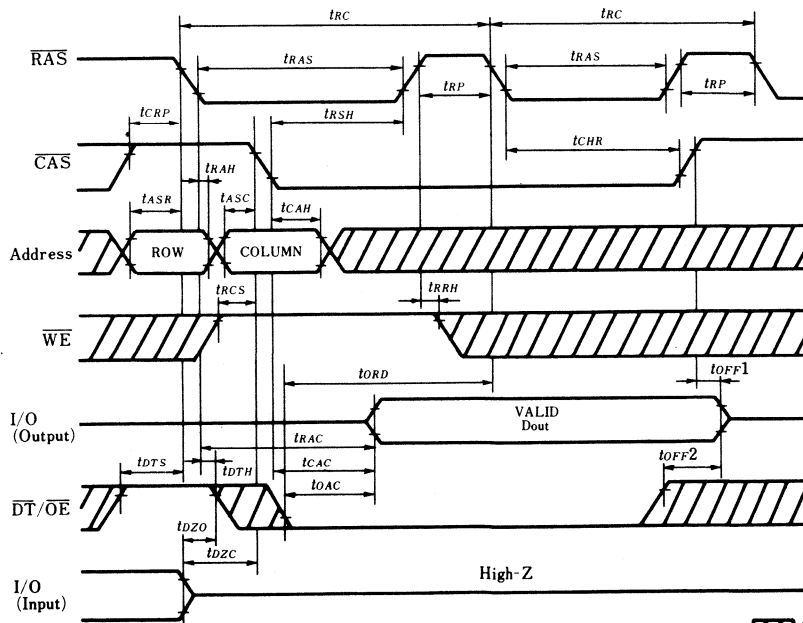


● **CAS BEFORE RAS REFRESH**



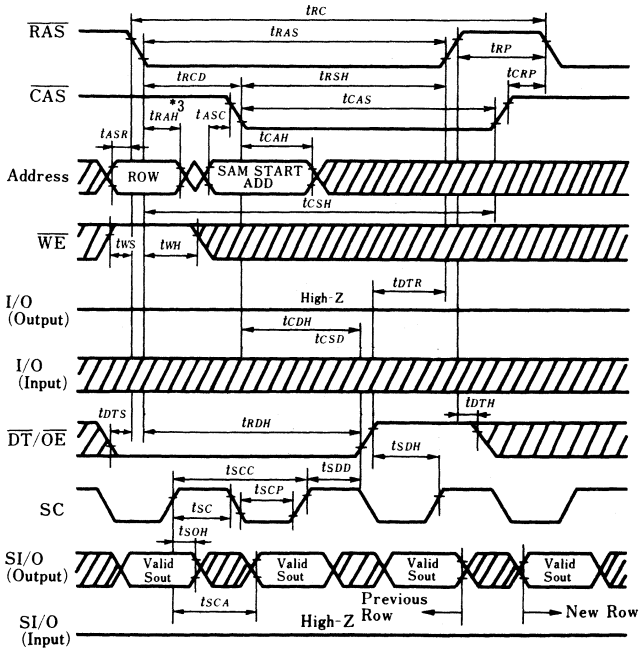
Do not care

● **HIDDEN REFRESH CYCLE**



Do not care

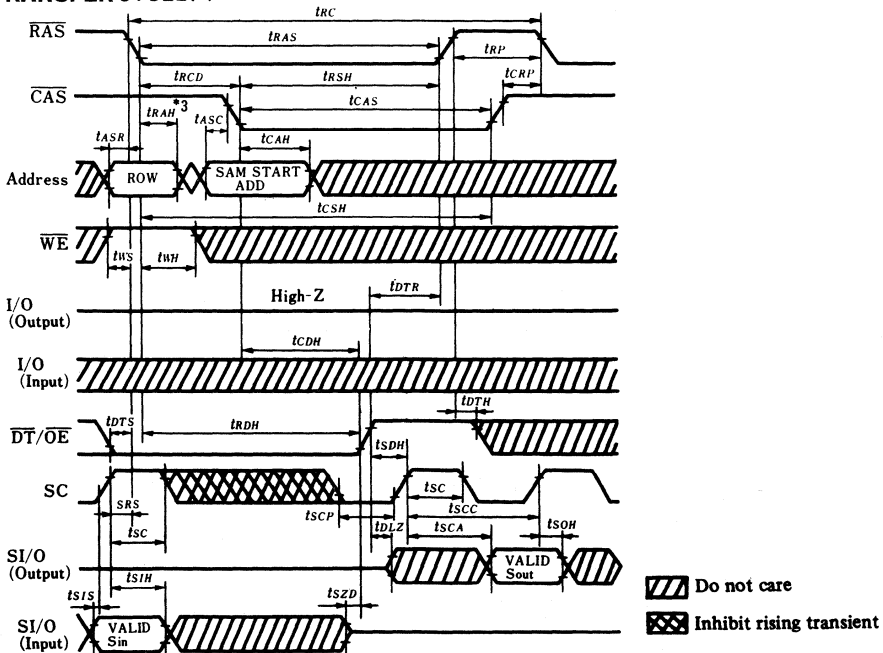
● READ DATA TRANSFER CYCLE (1)*1 *2



Note

- *1) In the case that the previous data transfer cycle was read data transfer. ▨ Do not care
- *2) Assume that SOE is "L" level.
- *3) CAS and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

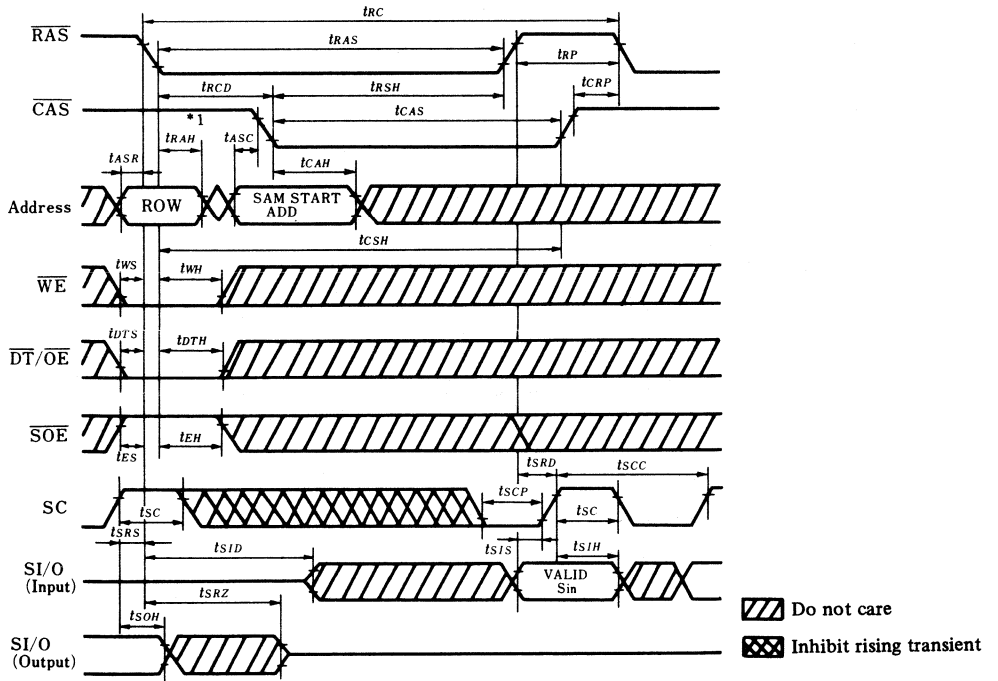
● READ DATA TRANSFER CYCLE (2)*1 *2



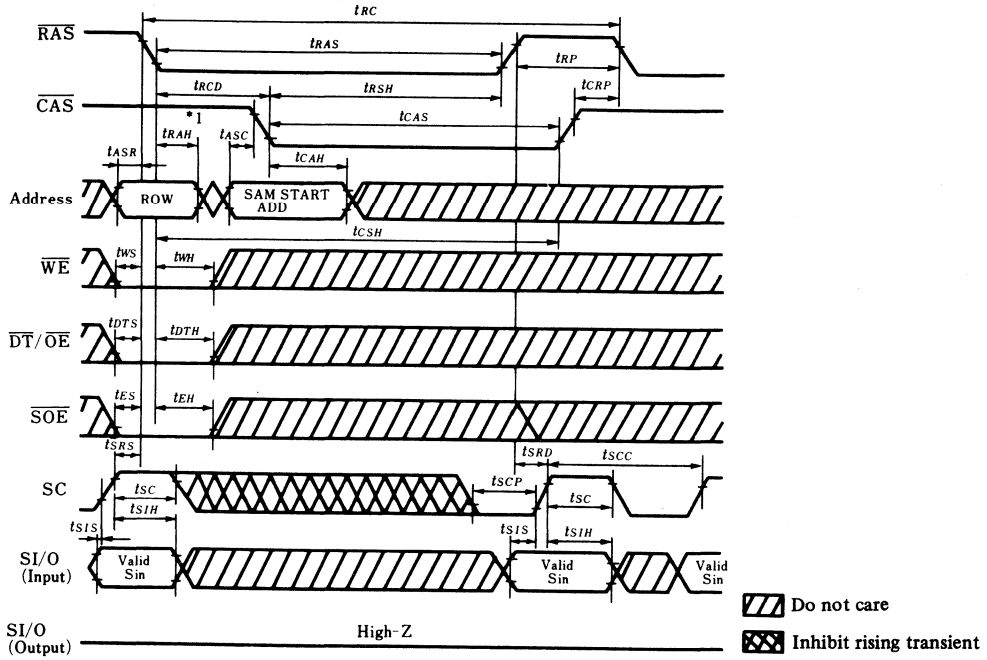
Note 1)

- *1) In the case that the previous data transfer cycle was write data transfer or pseudo data transfer.
- *2) Assume that SOE is "L" level,
- *3) CAS and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

● PSEUDO DATA TRANSFER CYCLE



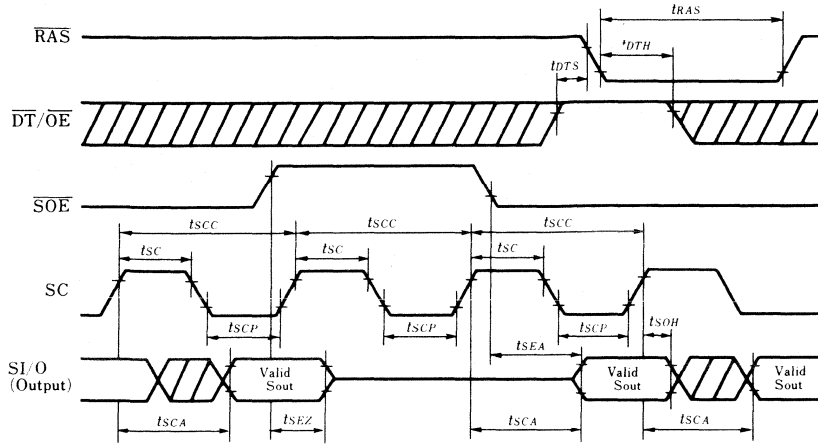
● WRITE DATA TRANSFER CYCLE



Note 1)

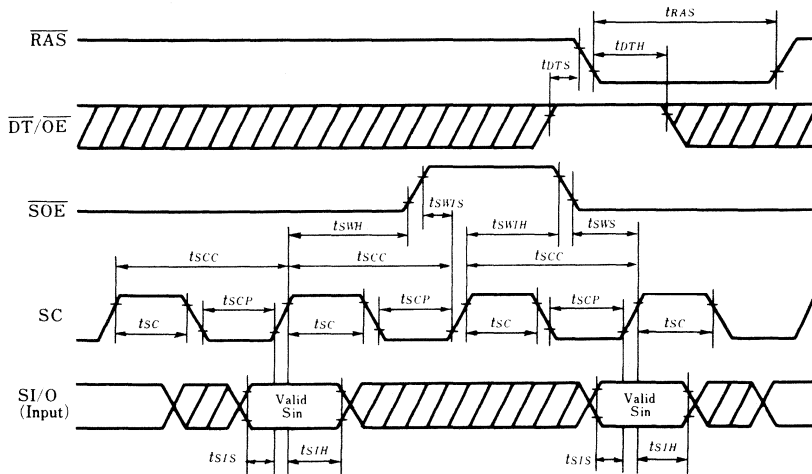
CAS and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

● SERIAL READ CYCLE



▨ Do not care

● SERIAL WRITE CYCLE



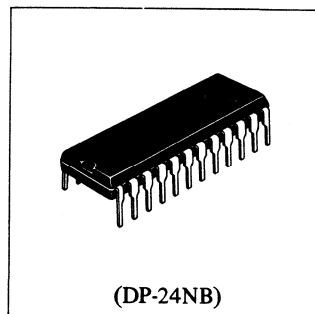
▨ Do not care

HM53462P Series

Preliminary

65,536 – word x 4 bits Multi Port DRAM (with Logic operation mode)

The HM53462P is a 262,144 bit multi port memory equipped with a 64k word x 4 bit Dynamic RAM port and a 256 word x 4 bit Serial Access Memory (SAM) port. The SAM port is connected to an internal 1,024 bit data register through a 256 word x 4 bit serial read or write access control. In the read data transfer cycle, the memory cell data is transferred from a selected word line of the RAM port to the data register. The RAM port has a write mask capability in addition to the conventional operation mode. Write bit selection out of 4 data bit can be achieved. Utilizing the Hitachi 2 μ m CMOS process, fast serial access operation and low power dissipation are realized. All inputs and outputs, including clocks, are TTL compatible. The package is a 400 mil 24-pin dual-in-line plastic package.

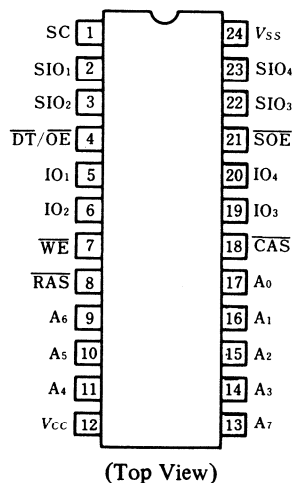


■ FEATURES

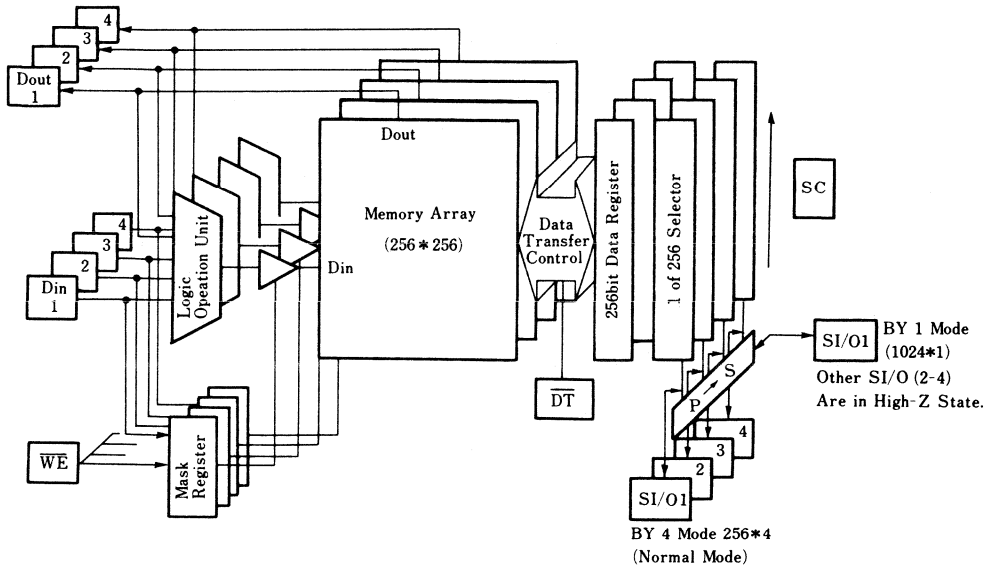
- Multi port organization
(RAM; 64k word x 4 bit and SAM; 256 word x 4 bit)
- 400 mil 24-pin dual-in-line plastic package
- Double layer polysilicon/polyicide n-well CMOS process
- Single 5V ($\pm 10\%$)
- Low power Active RAM; 380 mW max.
SAM; 220 mW max.
Standby 40 mW max.
- Access Time RAM; 100ns/120ns/150ns
SAM; 40ns/ 40ns/ 60ns
- Cycle Time Random read or write cycle time (RAM)
190ns/220ns/260ns
Serial read or write cycle time (SAM)
40ns/ 40ns/ 60ns
- TTL compatible
- 256 refresh cycles . . . 4ms
- Refresh function $\overline{\text{RAS}}$ only refresh
 $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
Hidden refresh
- Bidirectional data transfer operation (RAM \leftrightarrow SAM)
- Fast serial access operation asynchronous from RAM port except data transfer cycle
- Real time read transfer capability
- Write mask mode capability
- Logic operation capability between Din and Dout
- SAM organization can be changed to 1024 x 1

Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifica

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} -1V to +7V
- Operating temperature, T_a (Ambient) 0°C to $+70^{\circ}\text{C}$
- Storage temperature -55°C to $+125^{\circ}\text{C}$
- Short circuit output current 50mA
- Power dissipation 1W

$A_0 \sim A_4$	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobe
Din	Data In
Dout	Data Out
$\overline{\text{RAS}}$	Row Address Strobe
WE	Read/Write Input
V_{CC}	Power (+5V)
V_{SS}	Ground
$A_0 \sim A_7$	Refresh Address Inputs

Note) The specifications of this device are subject to change without notice.
 Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ INPUT/OUTPUT CAPACITANCE

Parameter	Symbol	typ.	max.	Unit
Address	C_{11}	—	5	pF
Clocks	C_{12}	—	5	pF
I/O, SI/O	C_{13}	—	7	pF

RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	min.	typ.	max.	Unit
Supply voltage	V_{CC}	4.5	5.0	5.5	V
Input High voltage	V_{IH}	2.4	—	6.5	V
Input Low voltage	V_{IL}	-1.0	—	0.8	V

Notes: All voltages referenced to V_{SS} .

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

RAM PORT	Symbol	SAM PORT		HM53462P -10	HM53462P -12	HM53462P -15	Unit
		Standby	Active				
Operating current RAS, CAS cycling $t_{RC} = \text{min.}$	I_{CC1}	○	×	70	60	50	mA
	I_{CC7}	×	○	110	100	80	mA
Standby current RAS, CAS = V_{IH}	I_{CC2}	○	×	7	7	7	mA
	I_{CC8}	×	○	40	40	30	mA
RAS only refresh current CAS = V_{IH} , RAS cycling $t_{RC} = \text{min.}$	I_{CC3}	○	×	60	50	40	mA
	I_{CC9}	×	○	100	90	70	mA
Page mode current RAS = V_{IL} , CAS cycling $t_{PC} = \text{min.}$	I_{CC4}	○	×	50	40	35	mA
	I_{CC10}	×	○	90	80	65	mA
CBR refresh current RAS cycling $t_{RC} = \text{min.}$	I_{CC5}	○	×	60	50	40	mA
	I_{CC11}	×	○	100	90	70	mA
Data transfer current RAS, CAS cycling $t_{RC} = \text{min.}$	I_{CC6}	○	×	75	65	55	mA
	I_{CC12}	×	○	115	105	85	mA

Parameter	Symbol	min.	max.	Unit
Input leakage	I_{IL}	-10	10	μA
Output leakage	I_{OL}	-10	10	μA
Output high voltage $I_{OH} = -2$ mA	V_{OH}	2.4	—	V
Output low voltage $I_{OL} = 4.2$ mA	V_{OL}	—	0.4	V

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)^{1), 10), 11)}

Parameter	Symbol	HM53462P -10		HM53462P -12		HM53462P -15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Random Read or Write Cycle Time	t_{RC}	190	—	220	—	260	—	ns	
Read Modify Write Cycle Time	t_{RWC}	260	—	300	—	355	—	ns	
Page Mode Cycle Time	t_{PC}	70	—	85	—	105	—	ns	
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	100	—	120	—	150	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	50	—	60	—	75	ns	3, 4
Output Buffer Turn Off Delay referenced to $\overline{\text{CAS}}$	t_{OFF1}	0	25	0	30	0	40	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	80	—	90	—	100	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	100	30000	120	30000	150	30000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	50	30000	60	30000	75	30000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	25	50	25	60	30	75	ns	7
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	50	—	60	—	75	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	100	—	120	—	150	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	20	—	20	—	25	—	ns	
Write Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	25	—	25	—	30	—	ns	
Write Command Pulse Width	t_{WP}	15	—	20	—	25	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	35	—	40	—	45	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	35	—	40	—	45	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	25	—	25	—	30	—	ns	8, 9
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{\text{RAS}}$	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
$\overline{\text{RAS}}$ Pulse Width (Read Modify Write Cycle)	t_{RWS}	170	—	200	—	245	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{WE}}$ Delay	t_{CWD}	85	—	100	—	125	—	ns	8
$\overline{\text{CAS}}$ Set-up Time (CAS before $\overline{\text{RAS}}$ refresh)	t_{CSR}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Hold Time (CAS before $\overline{\text{RAS}}$ refresh)	t_{CHR}	20	—	25	—	30	—	ns	
$\overline{\text{RAS}}$ Precharge to $\overline{\text{CAS}}$ Hold Time	t_{RPC}	10	—	10	—	10	—	ns	
$\overline{\text{CAS}}$ Precharge Time	t_{CP}	10	—	15	—	20	—	ns	
Access Time from $\overline{\text{OE}}$	t_{OAC}	—	25	—	30	—	40	ns	
Output Buffer Turn-off Delay referenced to $\overline{\text{OE}}$	t_{OFF2}	0	25	0	30	0	40	ns	
$\overline{\text{OE}}$ to Data-in Delay Time	t_{ODD}	25	—	30	—	40	—	ns	
$\overline{\text{OE}}$ Hold Time referenced to $\overline{\text{WE}}$	t_{OEH}	10	—	15	—	20	—	ns	
Data-in to $\overline{\text{CAS}}$ Delay Time	t_{DZC}	0	—	0	—	0	—	ns	
Data-in to $\overline{\text{OE}}$ Delay Time	t_{DZO}	0	—	0	—	0	—	ns	
$\overline{\text{OE}}$ to $\overline{\text{RAS}}$ Delay Time	t_{ORD}	25	—	30	—	40	—	ns	

(to be continued)

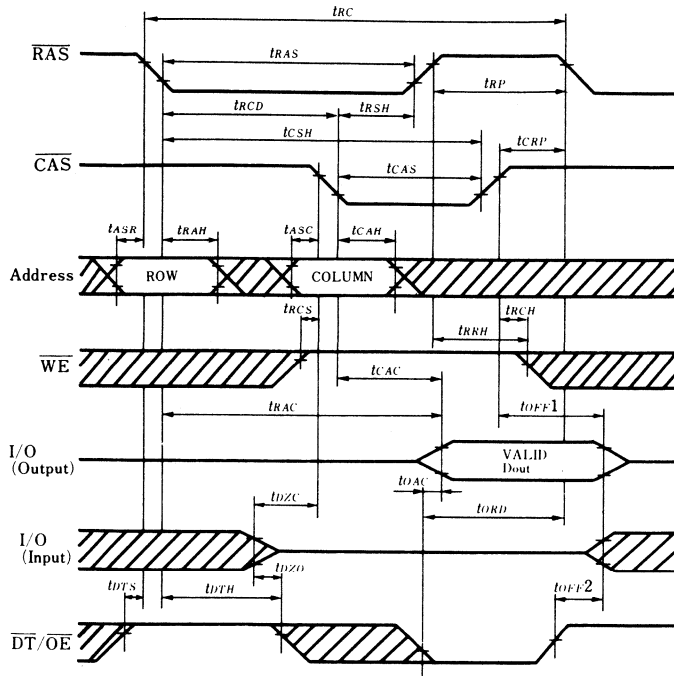
■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$) (1), 10), 11)

Parameter	Symbol	HM53462P -10		HM53462P -12		HM53462P -15		Unit	Note
		min.	max.	min.	max.	min.	max.		
Serial Clock Cycle Time	t_{SCC}	40	—	40	—	60	—	ns	
Access Time from SC	t_{SCA}	—	40	—	40	—	60	ns	10
Access Time from SOE	t_{SEA}	—	25	—	30	—	40	ns	10
SC Pulse Width	t_{SC}	10	—	10	—	10	—	ns	
SC Precharge Width	t_{SCP}	10	—	10	—	10	—	ns	
Serial Data-out Hold Time after SC High	t_{SOH}	10	—	10	—	10	—	ns	
Serial Output Buffer Turn-off Delay from SOE	t_{SEZ}	0	25	0	25	0	30	ns	
Serial Data-in Set-up Time	t_{SIS}	0	—	0	—	0	—	ns	
Serial Data-in Hold Time	t_{SIH}	15	—	20	—	25	—	ns	
$\overline{\text{DT}}$ to RAS Set-up Time	t_{DTS}	0	—	0	—	0	—	ns	
$\overline{\text{DT}}$ to RAS Hold Time (Read Data Transfer Cycle)	t_{RDH}	80	—	90	—	110	—	ns	
$\overline{\text{DT}}$ to RAS Hold Time	t_{DTH}	15	—	15	—	20	—	ns	
$\overline{\text{DT}}$ to $\overline{\text{CAS}}$ Hold Time	t_{CDH}	20	—	30	—	45	—	ns	
Last SC to $\overline{\text{DT}}$ Delay Time	t_{SDD}	5	—	5	—	10	—	ns	
First SC to $\overline{\text{DT}}$ Hold Time	t_{SDH}	20	—	25	—	30	—	ns	
$\overline{\text{DT}}$ to RAS Delay Time	t_{DTR}	10	—	10	—	10	—	ns	
$\overline{\text{WE}}$ to RAS Set-up Time	t_{WS}	0	—	0	—	0	—	ns	
$\overline{\text{WE}}$ to RAS Hold Time	t_{WH}	15	—	15	—	20	—	ns	
I/O to RAS Set-up Time	t_{MS}	0	—	0	—	0	—	ns	
I/O to RAS Hold Time	t_{MH}	15	—	15	—	20	—	ns	
Serial Output Buffer Turn off Delay from RAS	t_{SRZ}	10	50	10	60	10	75	ns	
SC to $\overline{\text{RAS}}$ Set-up Time	t_{SRS}	30	—	40	—	45	—	ns	
RAS to SC Delay Time	t_{SRD}	25	—	30	—	35	—	ns	
Serial Data Input Delay Time from RAS	t_{SID}	50	—	60	—	75	—	ns	
Serial Data Input to $\overline{\text{DT}}$ Delay Time	t_{SZD}	0	—	0	—	0	—	ns	
SOE to RAS Set-up Time	t_{ES}	0	—	0	—	0	—	ns	
SOE to RAS Hold Time	t_{EH}	15	—	15	—	20	—	ns	
Serial Read Enable Set-up Time	t_{SWS}	0	—	0	—	0	—	ns	
Serial Write Enable Hold Time	t_{SWH}	30	—	40	—	60	—	ns	
Serial Write Disable Set-up Time	t_{SWIS}	0	—	0	—	0	—	ns	
Serial Write Disable Hold Time	t_{SWIH}	30	—	40	—	60	—	ns	
$\overline{\text{DT}}$ to Sout in Low-Z Delay Time	t_{DLZ}	5	—	10	—	10	—	ns	

Notes)

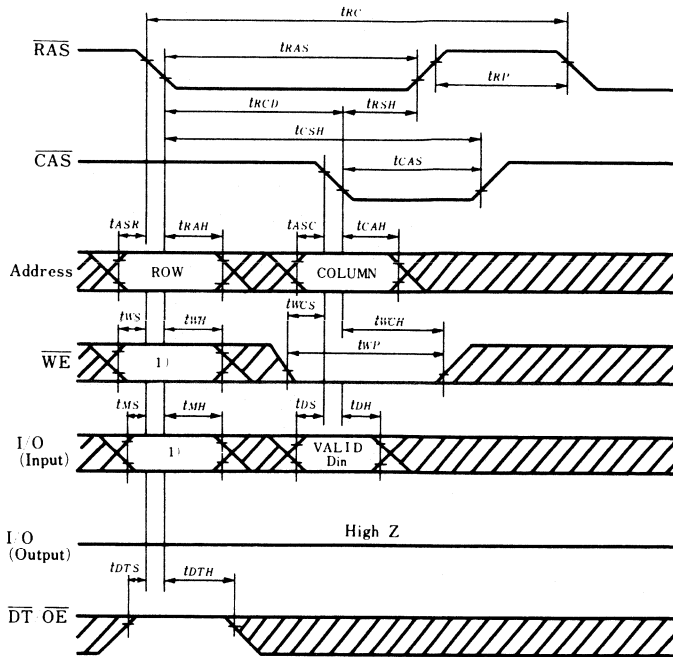
1. AC measurements assume $t_T = 5\text{ ns}$.
2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
3. Measured with a load circuit equivalent to 2TTL loads and 100 pF.
4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met, $t_{RCD}(\text{max})$ is specified as a reference point only, if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, then access time is controlled exclusively by t_{CAC} .
8. t_{WCS} and t_{CWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only: if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data out pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$, the cycle is a read/write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied, the condition of the data out (at access time) is indeterminate.
9. These parameters are referenced to $\overline{\text{CAS}}$ leading edge in early write cycle and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
10. Measured with a load circuit equivalent to 2TTL and 50 pF.
11. An initial pause of 100 μs is required after power-up. Then execute at least 8 Logic Reset Cycles as initialization cycles.


■ WAVE FORMS
● READ CYCLE



▨ Do not care

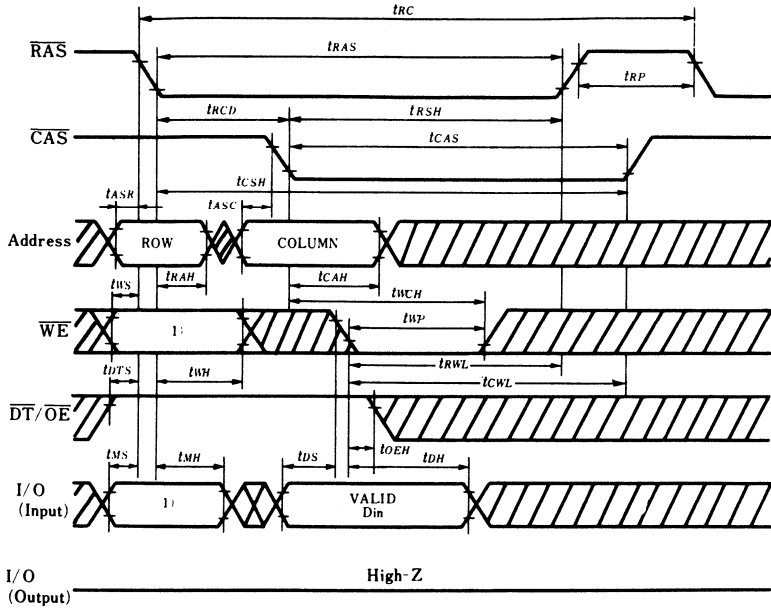
● EARLY WRITE CYCLE



 Do not care

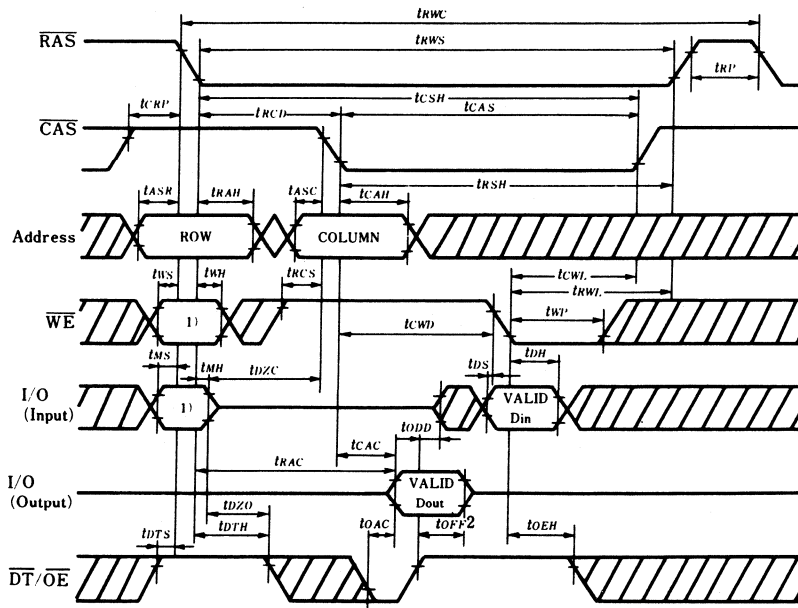
NOTE 1) When \overline{WE} is "H" level, the all data on the I/O can be written into the cell. When \overline{WE} is "L" level, the data on the I/O are not written except for when I/O is "H" level at the falling edge of RAS.

● DELAYED WRITE CYCLE



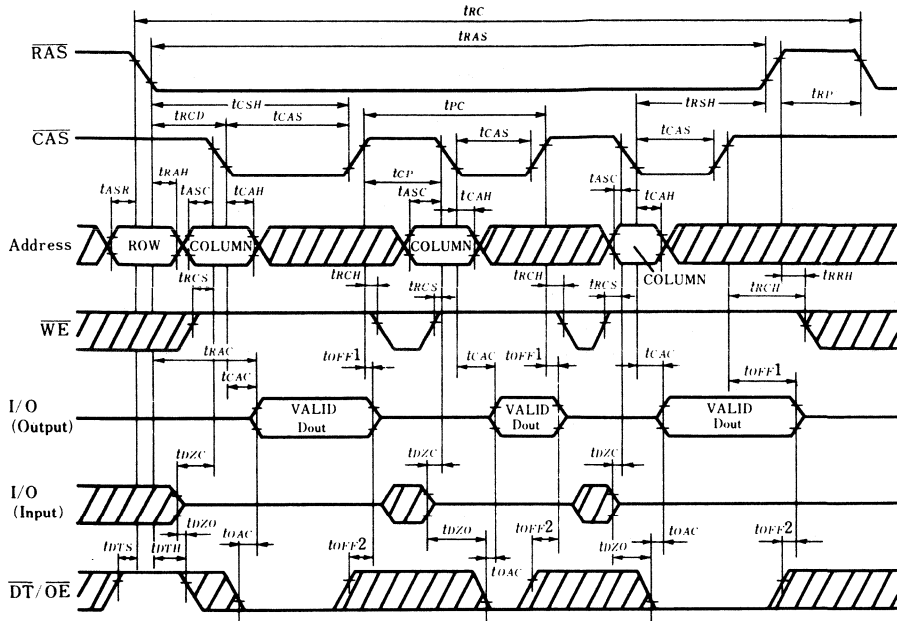
NOTE 1) When \overline{WE} is "H" level, all the data on I/O 1-4 can be written into the memory cell. ▨ Do not care
 When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of \overline{RAS} .

● READ MODIFY WRITE CYCLE



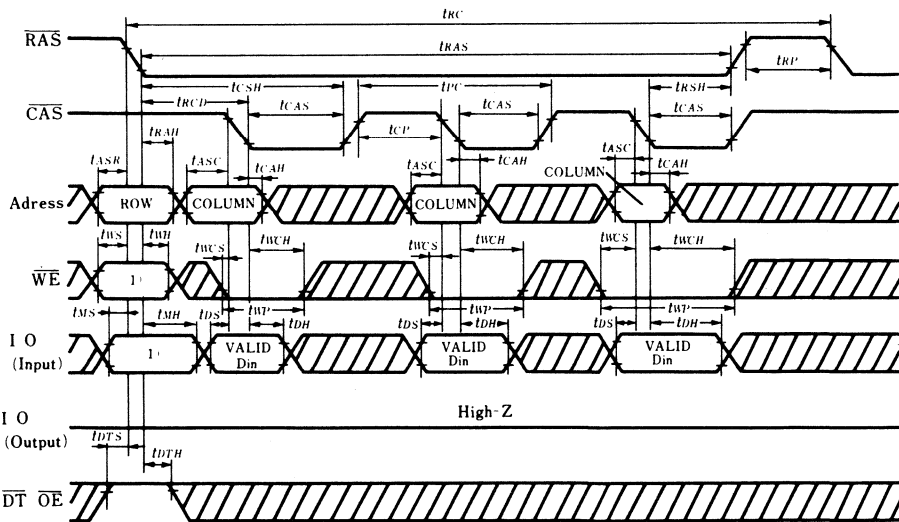
NOTE 1) When \overline{WE} is "H" level, all the data on I/O 1-4 can be written into the memory cell. ▨ Do not care
 When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of \overline{RAS} .

● PAGE MODE READ CYCLE



▨ Do not care

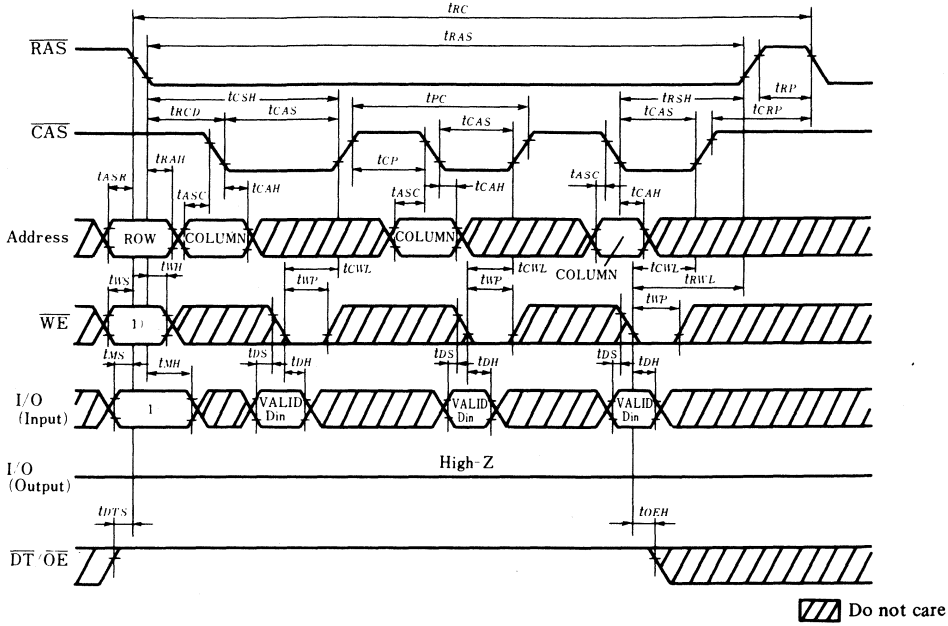
● PAGE MODE WRITE CYCLE (Early Write)



▨ Do not care

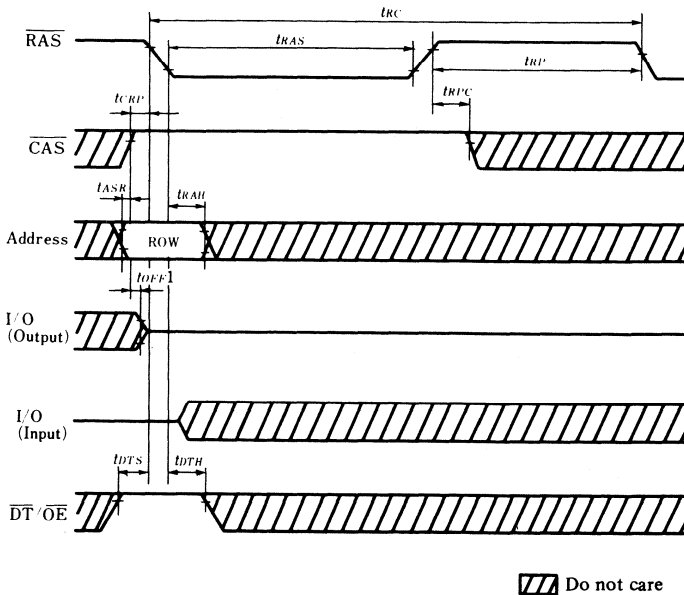
NOTE 1) When \overline{WE} is "H" level, all the data on I/O 1-4 can be written into the memory cell.
When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of RAS.

● PAGE MODE WRITE CYCLE (Delayed Write)

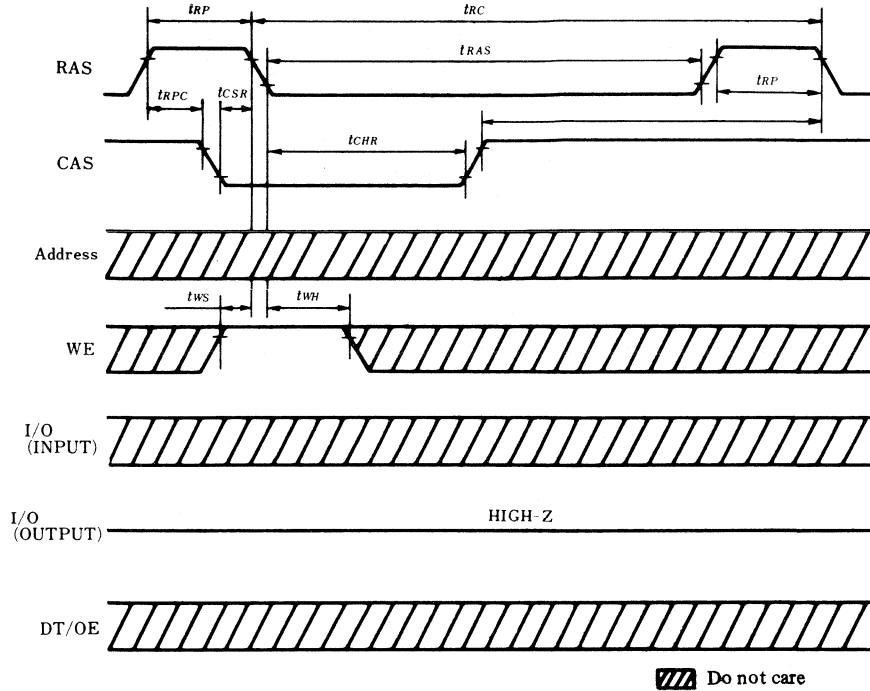


NOTE 1) When \overline{WE} is "H" level, all the data on I/O 1-4 can be written into the memory cell.
 When \overline{WE} is "L" level, the data on I/Os are not written except for when I/O = "H" at the falling edge of \overline{RAS} .

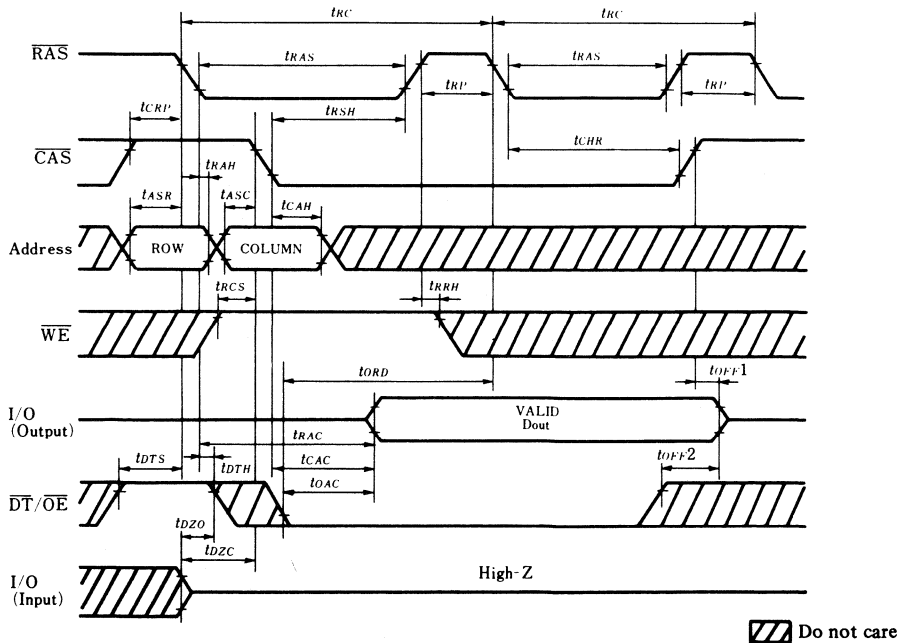
● \overline{RAS} ONLY REFRESH CYCLE



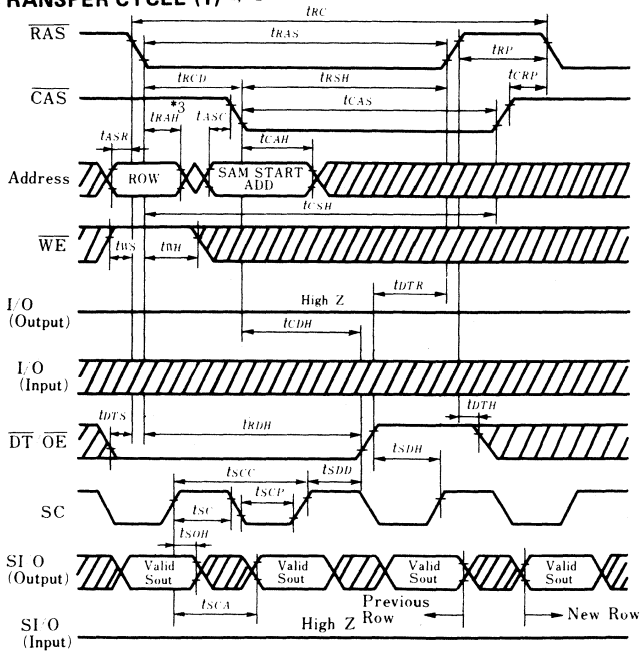
● **CAS BEFORE RAS REFRESH CYCLE**



● **HIDDEN REFRESH CYCLE**



● READ DATA TRANSFER CYCLE (1)*1,*2

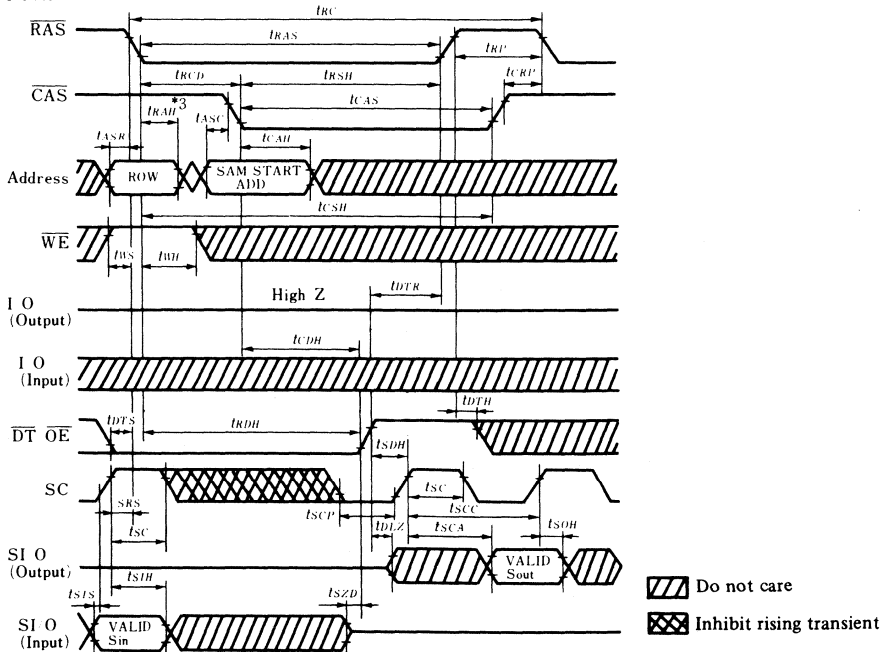


NOTE *1) In the case that the previous data transfer cycle was read data transfer. Do not care

*2) Assume that SOE is "Low".

*3) CAS and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

● READ DATA TRANSFER CYCLE (2)*1,*2



Do not care

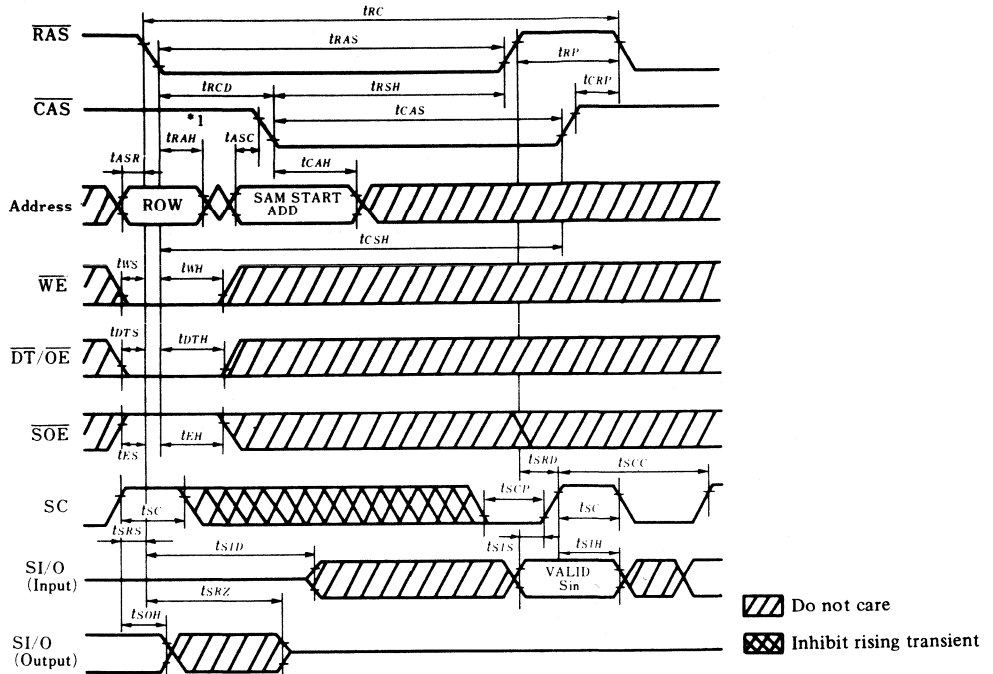
Inhibit rising transient

NOTE *1) In the case that the previous data transfer cycle was read data transfer.

*2) Assume that SOE is "Low".

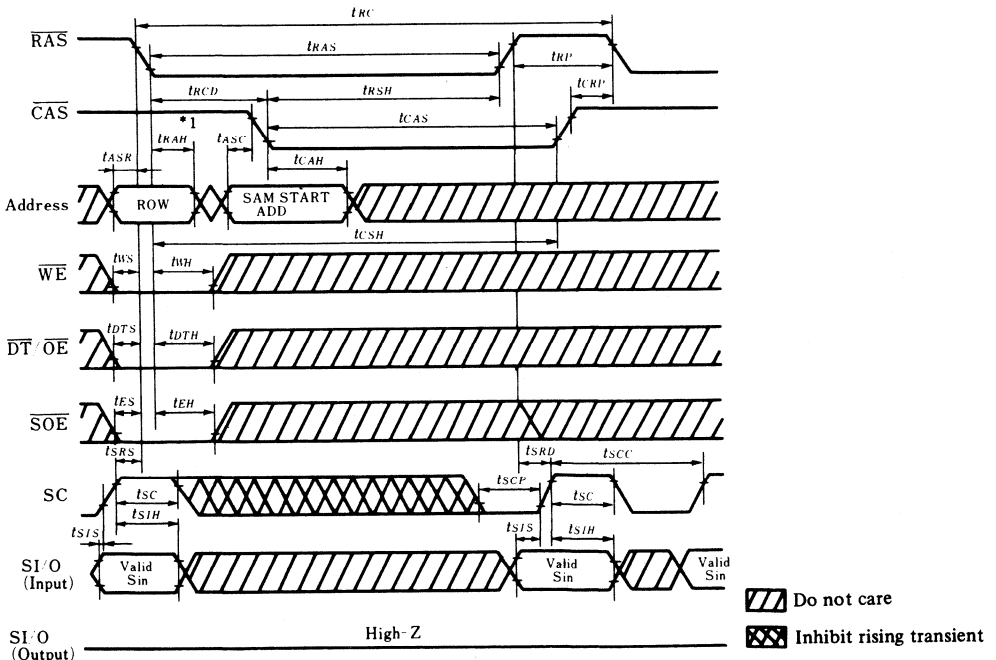
*3) CAS and SAM start Address need not be supplied every cycle, only when it is desired to change to a new SAM start Address.

● PSEUDO DATA TRANSFER CYCLE



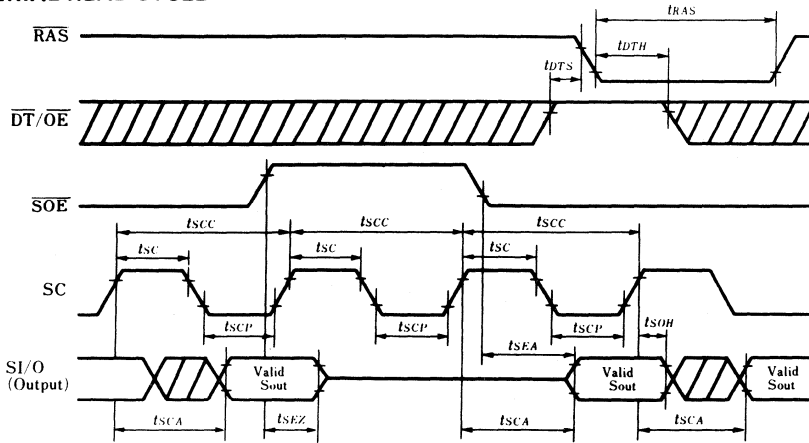
*1) \overline{CAS} and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

● WRITE DATA TRANSFER CYCLE



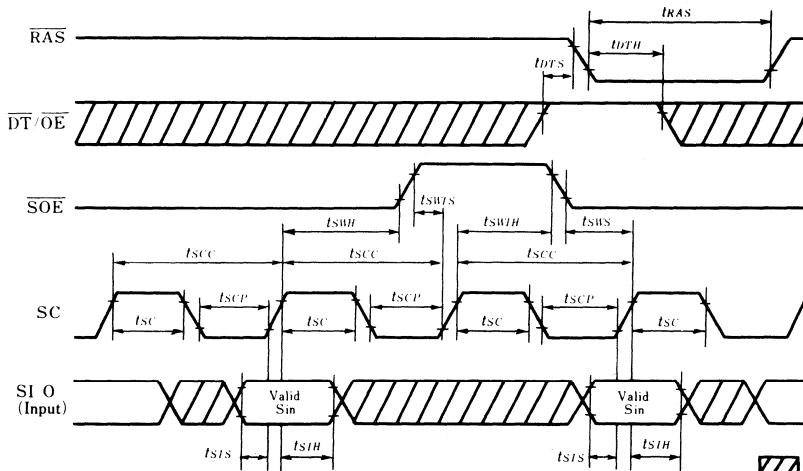
*1) \overline{CAS} and SAM start address need not be supplied every cycle, only when it is desired to change to a new SAM start address.

● SERIAL READ CYCLE



● SERIAL WRITE CYCLE

Do not care



Do not care

■ ELECTRICAL AC CHARACTERISTICS (Logic operation mode)

Parameter	Symbol	HM53462P -10		HM53462P -12		HM53462P -15		Unit
		min.	max.	min.	max.	min.	max.	
Write cycle time	t_{FRC}	230	-	265	-	310	-	ns
RAS pulse width in write cycle	t_{RFS}	140	-	165	-	200	-	ns
CAS pulse width in write cycle	t_{CFS}	80	-	95	-	105	-	ns
CAS hold time in write cycle	t_{FCSH}	140	-	165	-	200	-	ns
RAS hold time in write cycle	t_{FRSH}	80	-	95	-	105	-	ns
Page mode cycle time (Write cycle)	t_{FPC}	100	-	120	-	135	-	ns

■ LOGIC CODE (FC0 ~ 3 are AX0 ~ AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$D_i \cdot M_i$
0	0	1	0	AND2	$\overline{D_i} \cdot M_i$
0	0	1	1	X4 → X1	-
0	1	0	0	AND3	$D_i \cdot \overline{M_i}$
0	1	0	1	THROUGH	D_i
0	1	1	0	EOR	$\overline{D_i} \cdot M_i + D_i \cdot \overline{M_i}$
0	1	1	1	OR1	$D_i + M_i$
1	0	0	0	NOR	$\overline{D_i} \cdot \overline{M_i}$
1	0	0	1	ENOR	$D_i \cdot M_i + \overline{D_i} \cdot \overline{M_i}$
1	0	1	0	INV1	$\overline{D_i}$
1	0	1	1	OR2	$\overline{D_i} + M_i$
1	1	0	0	INV2	$\overline{M_i}$
1	1	0	1	OR3	$D_i + \overline{M_i}$
1	1	1	0	NAND	$\overline{D_i} + \overline{M_i}$
1	1	1	1	1	ONE

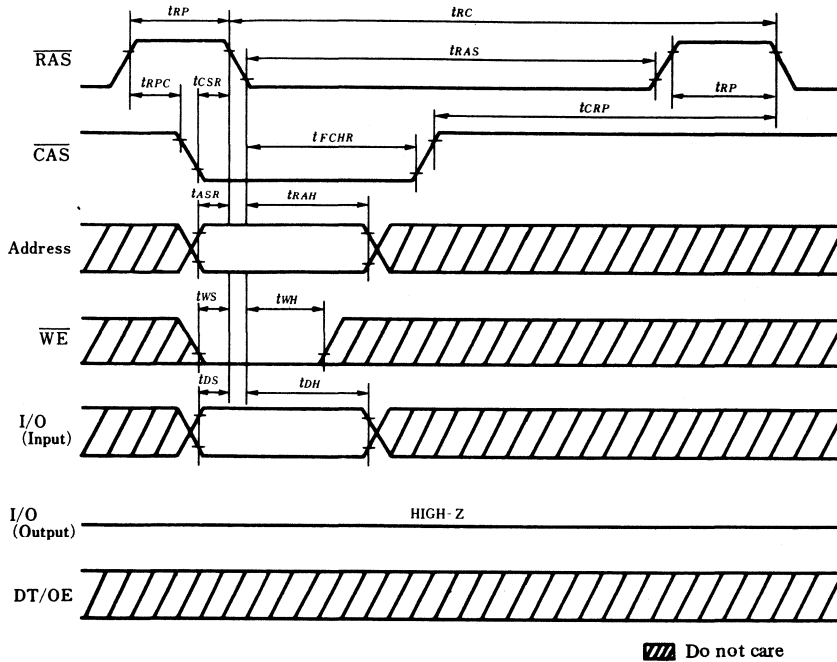
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

D_i : External Data-in

M_i : The data of the memory cell

● LOGIC OPERATION SET/RESET CYCLE (With $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh)



▨ Do not care

*1) Logic code A0-A3 (A4-A7: don't care)

*2) Write mask data

DESCRIPTION

1. LOGIC OPERATION MODE

HM53462P has an internal logic operation unit which makes a process of graphics simple. The logic is determined in "Logic operation set/reset cycle", and the operation is executed in every write cycle succeeding to the logic operation set/reset cycle. In this mode the internal read-modify-write operation is executed and the cell data is converted into the new data given by the logic operation between Din and the old cell data.

2. LOGIC OPERATION SET/RESET CYCLE

A logic operation set/reset cycle is performed by bringing $\overline{\text{CAS}}$ and $\overline{\text{WE}}$ low when $\overline{\text{RAS}}$ falls (Fig. 1). The logic code and the bits to be masked are determined respectively by Ax0-3 state and I/O1-4 state at the falling edge of $\overline{\text{RAS}}$. Furthermore, in this cycle $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh operation is executed, too. In the case of executing the conventional CAS before $\overline{\text{RAS}}$ refresh operation, $\overline{\text{WE}}$ must be high when $\overline{\text{RAS}}$ falls.

2.1. Logic code

The logic code is shown in Table 1. When power is turned on, the logic code is initialized to "THROUGH". If the logic code is $(\text{Ax3}, \text{Ax2}, \text{Ax1}, \text{Ax0}) = (0, 0, 1, 1)$, the SAM organization is changed to $1,024 \times 1$ using the internal parallel to serial converter (Fig. 2). In the case that the SAM organization is changed to $1,024 \times 1$, one data transfer cycle is needed to initialize the SAM selector. Once the SAM organization is changed to 1024×1 , this code is maintained unless power is turned off.

2.2. Write mask

HM35462P has two kinds of mask registers (register 1, 2). The register 1 is set by bringing $\overline{\text{WE}}$ low at the falling edge of $\overline{\text{RAS}}$ during the write cycle, and the mask data is available only in this cycle. The register 2 is set by level of I/O in the logic operation set/reset cycle, and the mask data is available until the next logic operation set/reset cycle. If the register 1 is set during the current logic operation mode, the mask data of the register 1 is preferred (that of the register 2 is ignored) and the logic becomes "THROUGH" only in this cycle (Fig. 3).

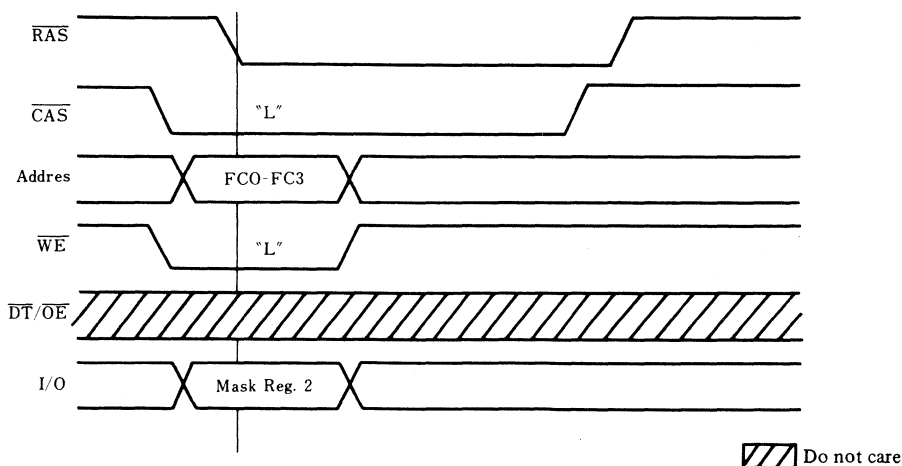


Fig. 1 LOGIC OPERATION SET/RESET CYCLE

Table 1. LOGIC CODE (FC0 ~ 3 are AX0 ~ AX3 in Logic Operation Set Cycle)

FC3	FC2	FC1	FC0	LOGIC	
				Symbol	Write Data
0	0	0	0	0	Zero
0	0	0	1	AND1	$D_i \cdot M_i$
0	0	1	0	AND2	$\overline{D_i} \cdot M_i$
0	0	1	1	X4 → X1	—
0	1	0	0	AND3	$D_i \cdot \overline{M_i}$
0	1	0	1	THROUGH	D_i
0	1	1	0	EOR	$\overline{D_i} \cdot M_i + D_i \cdot \overline{M_i}$
0	1	1	1	OR1	$D_i + M_i$
1	0	0	0	NOR	$\overline{D_i} \cdot \overline{M_i}$
1	0	0	1	ENOR	$D_i \cdot M_i + D_i \cdot \overline{M_i}$
1	0	1	0	INV1	$\overline{D_i}$
1	0	1	1	OR2	$\overline{D_i} + M_i$
1	1	0	0	INV2	$\overline{M_i}$
1	1	0	1	OR3	$D_i + \overline{M_i}$
1	1	1	0	NAND	$\overline{D_i} + \overline{M_i}$
1	1	1	1	1	ONE

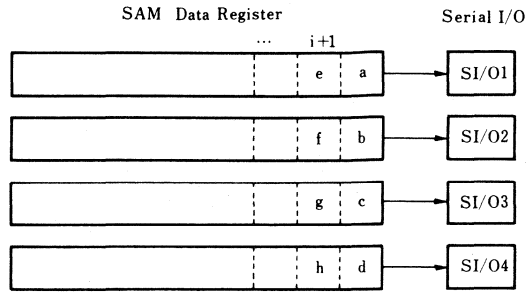
→ SAM organization changes to 1024 x 1

→ Logic operation mode reset

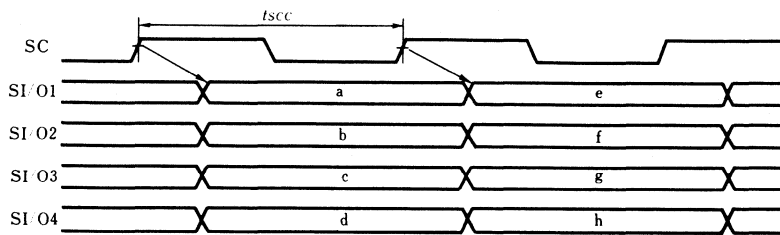
Di : External Data-in

Mi : The data of the memory cell

Fig. 2 THE SHIFT WAY OF SAM DATA



1) By 4 mode (SAM organization: 256 × 4)



2) By 1 mode (SAM organization: 1024 × 1)

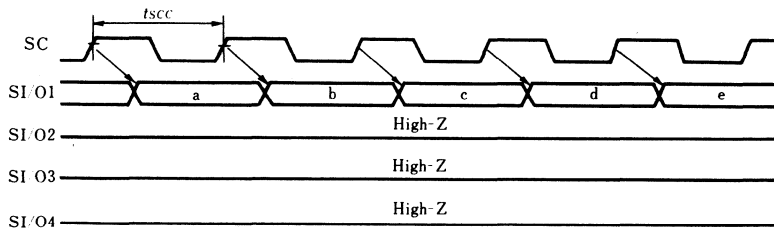
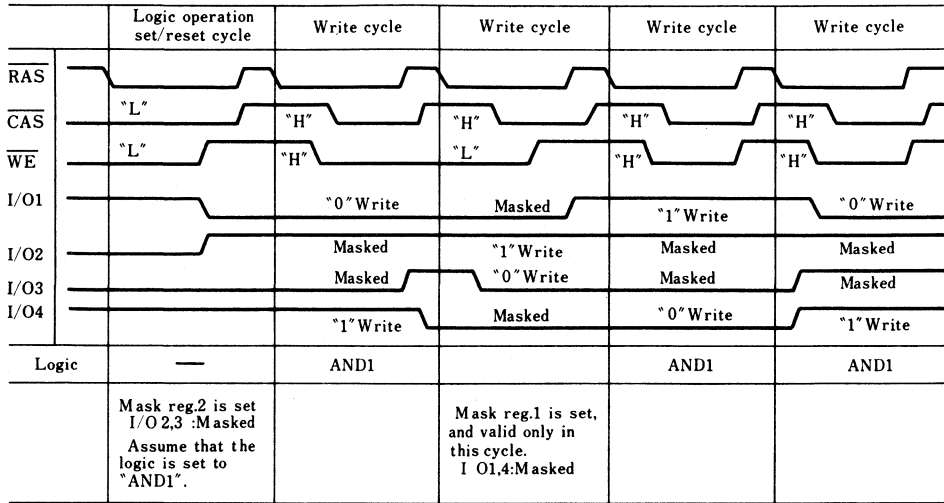


Fig. 3 EXAMPLE OF LOGIC OPERATION MODE



MOS DYNAMIC RAM MODULE

HB561003A/B Series

262,144 x 9 bit Dynamic Random Access Memory Module

The HB561003A/B is a 2.25M dynamic random-access memory module organized as 262,144 x 9 bits [bit nine (PD, PQ) is generally used for parity and is controlled by \overline{PCAS}] in a 30-pin single-in-line package comparing nine HM50256CP, 262,144 x 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on a substrate together with decoupling capacitors.

■ FEATURES

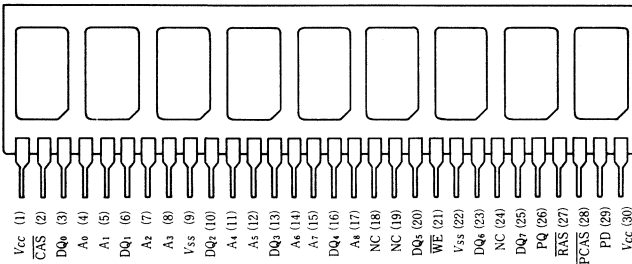
- 262,144 words x 9 bits Organization
- Industry standard 30-pin Single Inline Package Memory Module
- Single 5V ($\pm 10\%$)
- Utilizes nine 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561003A/B operates as nine HM50256CP as shown in the functional block diagram.
- Low Power; Operating: 2,160mW typ. ($t_{RC} = 260ns$)
Standby: 135 mW typ.

- High speed:

	Access Time from RAS (max)	Access Time from CAS (max)	Read or Write Cycle (min)
HB561003A/B-12	120ns	70ns	220ns
HB561003A/B-15	150ns	75ns	260ns
HB561003A/B-20	200ns	100ns	330ns

- Page mode capability
- TTL compatible
- 256 refresh cycles/4ms
- 3 variations of refresh
 - \overline{RAS} only refresh
 - CAS before \overline{RAS} refresh
 - Hidden refresh
- Operating Ambient Air Temperature: 0°C to +70°C

■ PIN ARRANGEMENT



* HB561003B's pin arrangement is same as HB561003A.

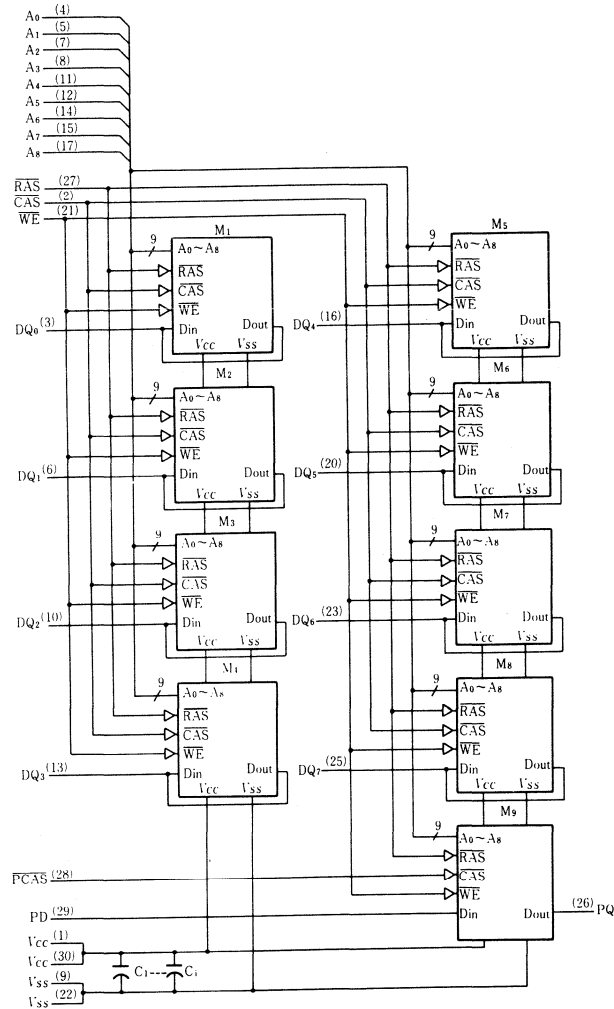
(Side View)

- Common \overline{CAS} control for eight common Data-In and Data-Out lines.
- Separate \overline{CAS} control for one separate pair of Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operations to prevent contention on Din and Dout.

PIN NOMENCLATURE

A0~A8	Address Inputs
\overline{CAS} , \overline{PCAS}	Column Address Strobes
DQ0~DQ7	Data In/Data Out
PD	Data In
NC	No Connection
PQ	Data Out
\overline{RAS}	Row Address Strobes
WE	Write Enable
V_{CC}	+5V Supply
V_{SS}	Ground

■FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} : -1V to +7V
- Operating temperature, T_a (Ambient): 0°C to +70°C
- Storage temperature (Ambient): -55°C to +125°C
- Power dissipation: 9W
- Short circuit output current: 50mA

■RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to +70°C)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	-	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	-	0.8	V	1

Notes: 1. All voltages referenced to V_{SS}

■ DC ELECTRICAL CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)

Parameter		Symbol	min.	max.	Unit	Notes
Operating current	$t_{RC} = 330\text{ns}$	I_{CC1}	-	495	mA	1
	$t_{RC} = 260\text{ns}$			630		
	$t_{RC} = 220\text{ns}$			747		
Standby current		I_{CC2}	-	40	mA	
Refresh current	$t_{RC} = 330\text{ns}$	I_{CC3}	-	378	mA	$\overline{\text{RAS}}$ only Refresh
	$t_{RC} = 260\text{ns}$			477		
	$t_{RC} = 220\text{ns}$			558		
Standby current	(D_{out} Enable)	I_{CC5}	-	90	mA	1
Refresh current	$t_{RC} = 330\text{ns}$	I_{CC6}	-	405	mA	$\overline{\text{CAS}}$ before RAS Refresh
	$t_{RC} = 260\text{ns}$			522		
	$t_{RC} = 220\text{ns}$			621		
Input leakage	$0 < V_{in} < 7\text{V}$	I_{LI}	-10	10	μA	
Output leakage	$0 < V_{out} < 7\text{V}$	I_{LO}	-10	10	μA	D_{out} is disabled
Output levels	High ($I_{out} = -5\text{mA}$)	V_{OH}	2.4	V_{CC}	V	
	Low ($I_{out} = 4.2\text{mA}$)	V_{OL}	0	0.4	V	

■ CAPACITANCE ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 25^\circ\text{C}$)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	-	60	pF	2
Clocks	C_{I2}	-	75	pF	2,3
DQ	$C_{I/O}$	-	17	pF	2,3
PQ	C_o	-	12	pF	2,3
PD	C_{I3}	-	10	pF	2

- Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 3. $\text{CAS} = V_{IH}$ to disable D_{out} .

■ ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$)^{1), 9), 10)}

Parameter	Symbol	HB561003A/B-12		HB561003A/B-15		HB561003A/B-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	-	120	-	150	-	200	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	-	70	-	75	-	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	-	30	-	40	-	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	-	260	-	330	-	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	90	-	100	-	120	-	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	70	10000	75	10000	100	10000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	35	50	35	75	35	100	ns	7
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	70	-	75	-	100	-	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	-	150	-	200	-	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	10	-	10	-	10	-	ns	
Row Address Set-up Time	t_{ASR}	0	-	0	-	0	-	ns	
Row Address Hold Time	t_{RAH}	15	-	15	-	20	-	ns	
Column Address Set-up Time	t_{ASC}	0	-	0	-	0	-	ns	
Column Address Hold Time	t_{CAH}	25	-	25	-	30	-	ns	
Column Address Hold Time referenced to $\overline{\text{RAS}}$	t_{AR}	75	-	100	-	130	-	ns	
Read Command Set-up Time	t_{WCS}	0	-	0	-	0	-	ns	8
Write Command Hold Time	t_{WCH}	45	-	45	-	55	-	ns	
Write Command Hold Time referenced to $\overline{\text{RAS}}$	t_{WCR}	95	-	120	-	155	-	ns	
Write Command Pulse Width	t_{WCP}	45	-	45	-	55	-	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	45	-	45	-	55	-	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	45	-	45	-	55	-	ns	
Data-in Set-up Time	t_{DS}	0	-	0	-	0	-	ns	8

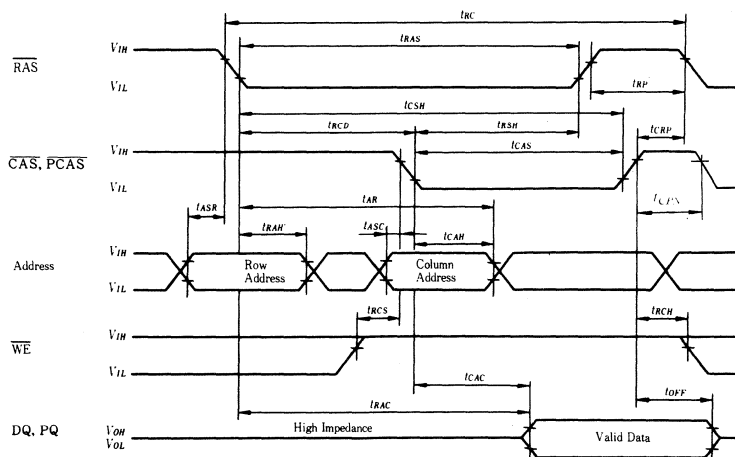
(to be continued)

Parameter	Symbol	HB561003A/B-12		HB561003A/B-15		HB561003A/B-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Data-in Hold Time	t_{DH}	45	—	45	—	55	—	ns	
Data-in Hold Time Referenced to \overline{RAS}	t_{DHR}	95	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to \overline{CAS}	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time Referenced to \overline{RAS}	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
\overline{CAS} Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
\overline{CAS} Set-up Time	t_{CSR}	10	—	10	—	10	—	ns	
\overline{CAS} Hold Time (\overline{CAS} before \overline{RAS})	t_{CHR}	120	—	150	—	200	—	ns	
\overline{RAS} Precharge to \overline{RAS} Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

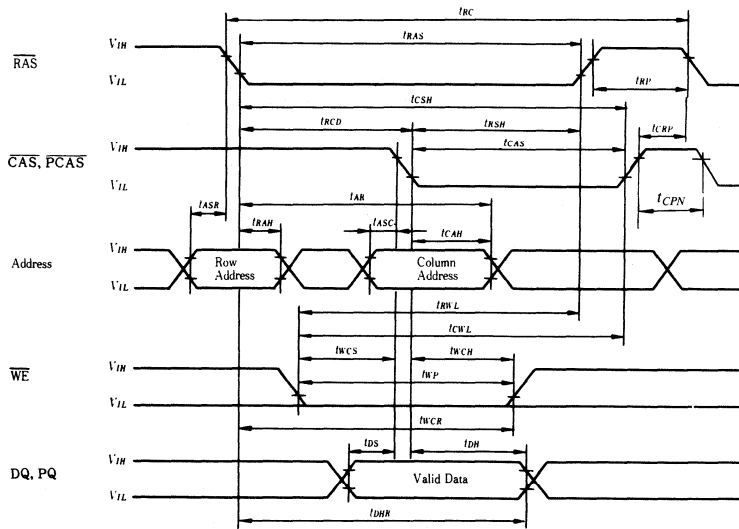
- Notes:
- AC measurements assume $t_T = 5ns$.
 - Assumes that $t_{RCD} \leq t_{RCD} (max)$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2TTL loads and 100pF.
 - Assumes that $t_{RCD} \geq t_{RCD} (max)$.
 - $t_{OFF} (max)$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
 - $V_{IH} (min)$ and $V_{IL} (max)$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD} (max)$ limit insures that $t_{RAC} (max)$ can be met. $t_{RCD} (max)$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD} (max)$ limit, access time is controlled exclusively by t_{CAC} .
 - An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.
 - At least 8 \overline{CAS} before \overline{RAS} refresh cycles are required before using internal refresh counter.

■ WAVE FORMS

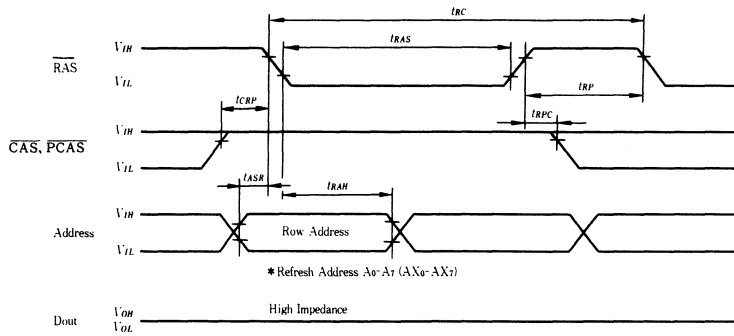
● Read Cycle



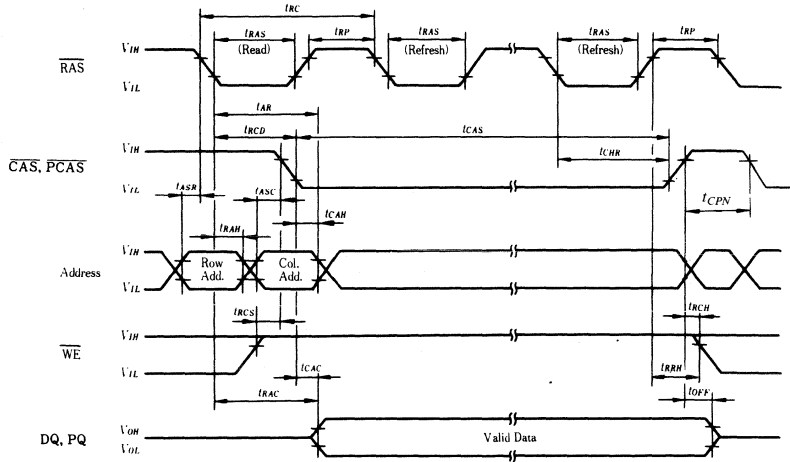
● Write Cycle



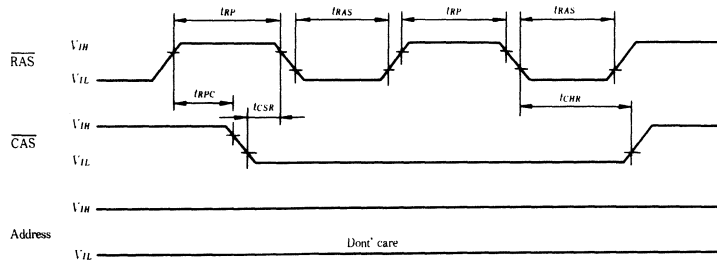
● RAS Only Refresh Cycle



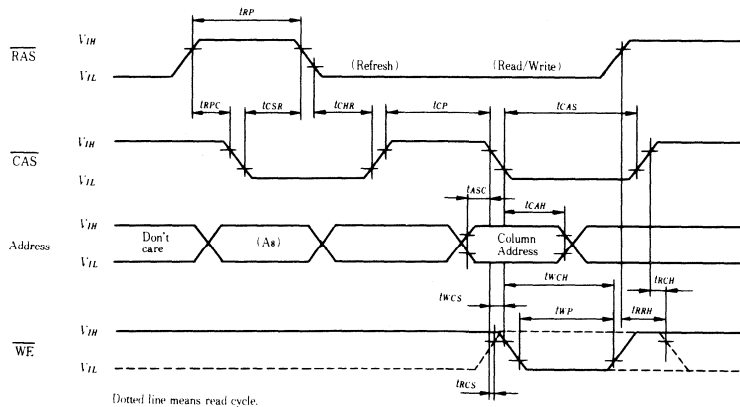
● Hidden Refresh Cycle



● CAS Before RAS Refresh Cycle

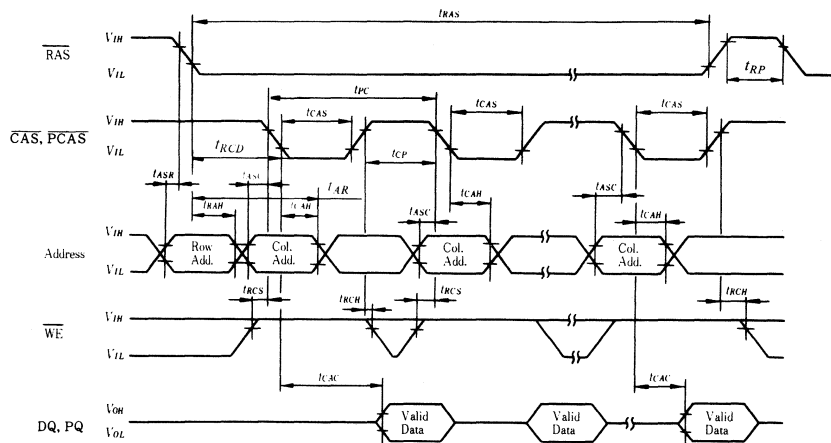


● COUNTER TEST

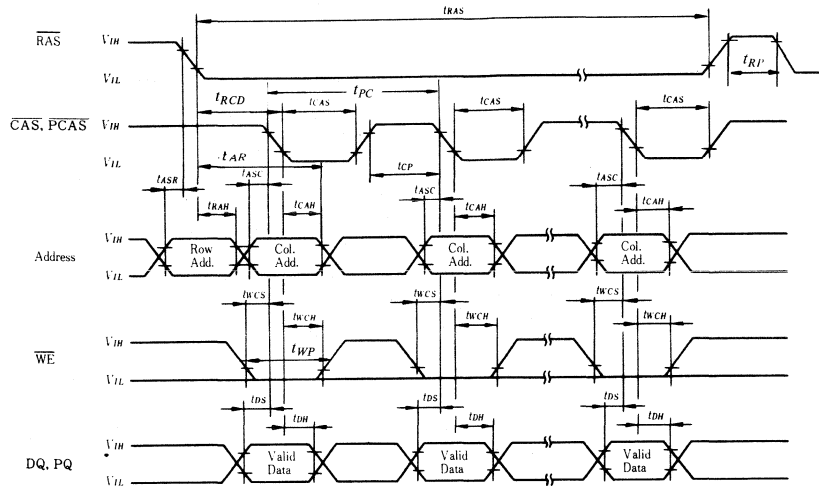


Parameter	Symbol	HB561003A/B-12		HB561003A/B-15		HB561003A/B-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Page Mode Supply Current	I_{CC7}	—	513	—	432	—	333	mA	
Page Mode Read or Write Cycle	t_{PC}	130	—	145	—	190	—	ns	
CAS Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns	

● Page Mode Read Cycle

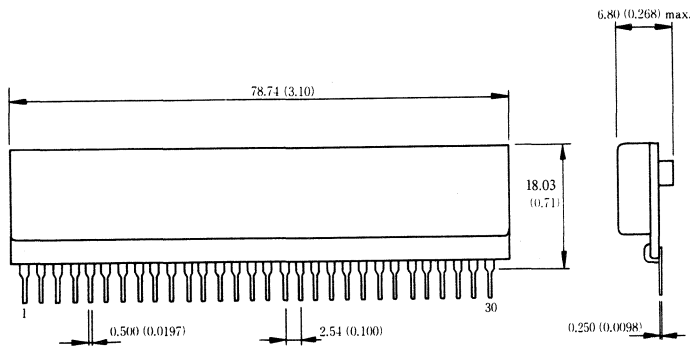


● Page Mode Write Cycle



■ PACKAGE OUTLINE

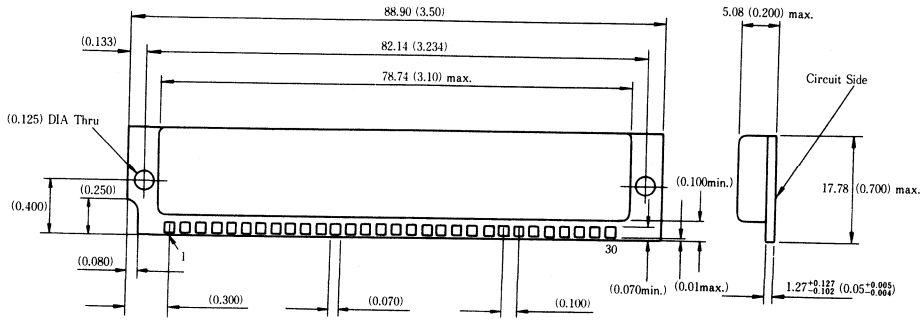
● HB561003A Series



Unit: mm (inch)

V _{cc}	1
$\overline{\text{CAS}}$	2
DQ0	3
A0	4
A1	5
DQ1	6
A2	7
A3	8
V _{ss}	9
DQ2	10
A4	11
A5	12
DQ3	13
A6	14
A7	15
DQ4	16
A8	17
NC	18
NC	19
DQ5	20
$\overline{\text{WE}}$	21
V _{ss}	22
DQ6	23
NC	24
DQ7	25
PQ	26
RAS	27
$\overline{\text{PCAS}}$	28
PD	29
V _{cc}	30

● HB561003B Series



Unit : mm (inch)

Note: Contact pads are overcoated with Tin/Lead.

V _{CC}	1
CAS	2
DQ ₀	3
A ₀	4
A ₁	5
DQ ₁	6
A ₂	7
A ₃	8
V _{SS}	9
DQ ₂	10
A ₄	11
A ₅	12
DQ ₃	13
A ₆	14
A ₇	15
DQ ₄	16
A ₈	17
NC	18
NC	19
DQ ₅	20
WE	21
V _{SS}	22
DQ ₆	23
NC	24
DQ ₇	25
PQ	26
RAS	27
PCAS	28
PD	29
V _{CC}	30

HB561004A Series

262,144-word x 4-bit Dynamic Random Access Memory Module

The HB561004A is a 1M dynamic random-access memory module organized as 262,144 x 4 bits in a 22-pin single-in-line package comprising four HM50256CP, 262,144 x 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together with two decoupling capacitors mounted beneath the PLCC.

FEATURES

- 262,144 words x 4 bits Organization
- Industry standard 22-pin Single Inline Package Memory Module
- Single 5V ($\pm 10\%$)
- Utilizes four 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561004A operates as four HM50256CP connected as shown in the functional block diagram.
- Low Power Dissipation:

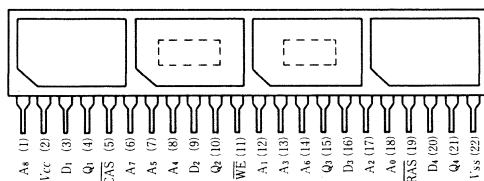
t_{RC}	Operating (typ)	Standby (typ)
220ns	1200mW	50mW
260ns	1000mW	
330ns	800mW	

- High speed:

	Access Time from \overline{RAS} (max)	Access Time from \overline{CAS} (max)	Read or Write Cycle (min)	Read Modify Write Cycle (min)
HB561004A-12	120ns	70ns	220ns	265ns
HB561004A-15	150ns	75ns	260ns	310ns
HB561004A-20	200ns	100ns	330ns	390ns

- Page mode capability
- 256 refresh cycles/4ms
- 3 variations of refresh
 - \overline{RAS} only refresh
 - \overline{CAS} before \overline{RAS} refresh
 - Hidden refresh
- Operating Ambient Air Temperature: 0°C to 70°C
- Common \overline{CAS} Control with Separate Data-in and Data-out
- Decoupling Capacitors Ready Mounted on Substrate

PIN ARRANGEMENT

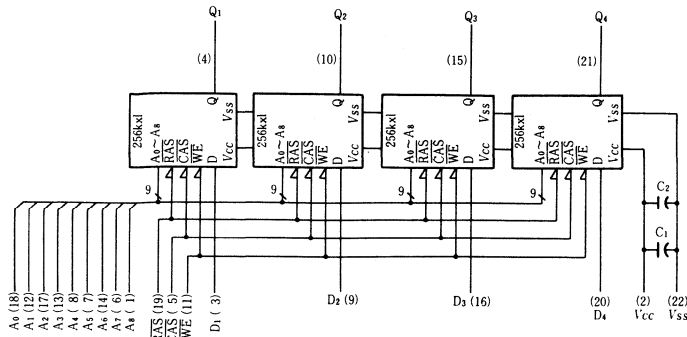


(Side View)

PIN NOMENCLATURE

A0 ~ A8	Address Input
\overline{CAS}	Column Address Strobe
D1 ~ D4	Data Inputs
Q1 ~ Q4	Data Outputs
\overline{RAS}	Row Address Strobe
\overline{WE}	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground

■FUNCTIONAL BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Voltage on any pin relative to V_{SS} : $-1V$ to $+7V$
 Operating temperature, T_a (Ambient): $0^{\circ}C$ to $+70^{\circ}C$
 Storage temperature (Ambient): $-55^{\circ}C$ to $+125^{\circ}C$
 Power dissipation: $4W$
 Short circuit output current: $50mA$

■RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^{\circ}C$)

Parameter	Symbol	min	typ	max	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Notes: 1. All voltage referenced to V_{SS}

■DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to $70^{\circ}C$ $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	min	max	Unit	Notes
Operating current $t_{RC}=330ns$ $t_{RC}=260ns$ $t_{RC}=220ns$	I_{CC1}	—	220 280 330	mA	1
Standby current	I_{CC2}	—	18	mA	
Refresh current $t_{RC}=330ns$ $t_{RC}=260ns$ $t_{RC}=220ns$	I_{CC3}	—	170 210 250	mA	RAS only Refresh
Standby current (Dout Enable)	I_{CC5}	—	40	mA	1
Refresh current $t_{RC}=330ns$ $t_{RC}=260ns$ $t_{RC}=220ns$	I_{CC6}	—	180 230 275	mA	CAS before RAS Refresh
Input leakage $0 < V_{in} < 7V$	I_{L1}	-10	10	μA	
Output leakage $0 < V_{out} < 7V$	I_{L0}	-10	10	μA	Dout is disabled
Output levels High ($I_{out} = -5mA$)	V_{OH}	2.4	V_{CC}	V	
Low ($I_{out} = 4.2mA$)	V_{OL}	0	0.4	V	

■CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^{\circ}C$)

Parameter	Symbol	typ	max	Unit	Notes
Address	C_{I1}	—	35	pF	2
Clocks	C_{I2}	—	45	pF	2, 3
Q	C_O	—	12	pF	2, 3
D	C_{I3}	—	10	pF	2

- Notes. 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 3. CAS = V_{IH} to disable D_{out} .

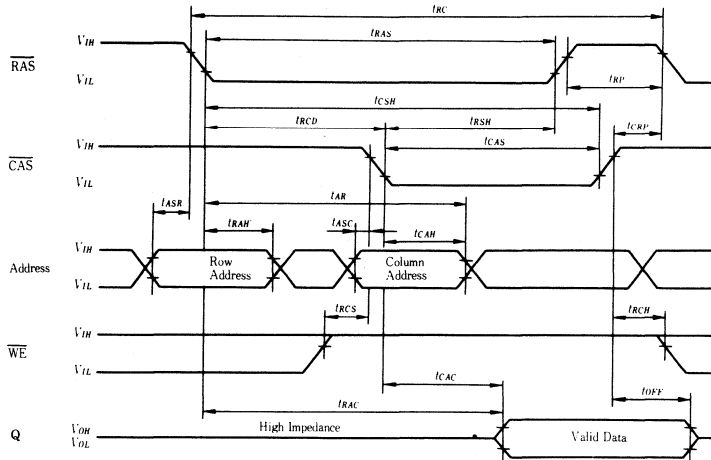
ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS^{1), 10), 11)}
 $(T_a = 0 \text{ to } +70^\circ\text{C}, V_{CC} = 5\text{V} \pm 10\%, V_{SS} = 0\text{V})$

Parameter	Symbol	HB561004A-12		HB561004A-15		HB561004A-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from RAS	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	t_{CAC}	—	70	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
RAS Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	t_{CAS}	70	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	t_{RCD}	35	50	35	75	35	100	ns	7
RAS Hold Time	t_{RSH}	70	—	75	—	100	—	ns	
CAS Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	25	—	30	—	ns	
Column Address Hold Time Referenced to RAS	t_{AR}	75	—	100	—	130	—	ns	
Read Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	45	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	t_{WCR}	95	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	45	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	45	—	45	—	55	—	ns	
Write Command to CAS Lead Time	t_{CWL}	45	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to RAS	t_{DHR}	95	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
CAS Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
CAS Set-up Time	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to RAS Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
CAS to WE Delay	t_{CWD}	70	—	75	—	100	—	ns	8
RAS to WE Delay	t_{RWD}	120	—	150	—	200	—	ns	

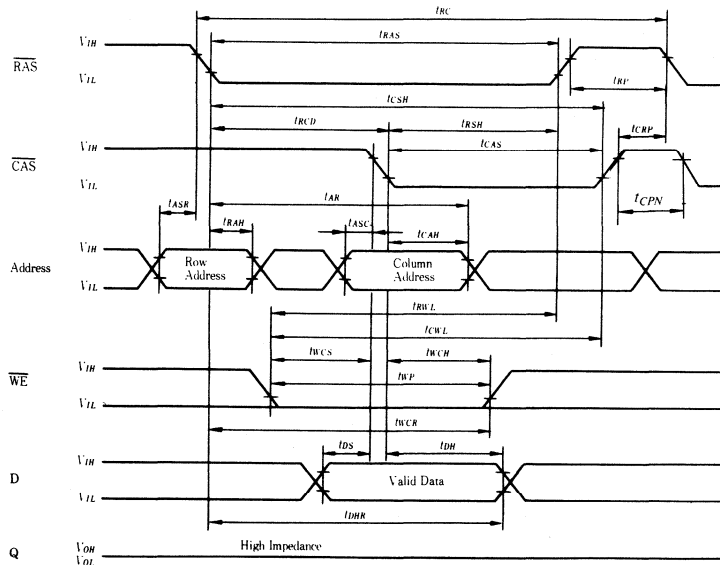
- Notes:
- AC measurements assume $t_T = 5\text{ns}$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended values shown in this table t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2TTL loads and 100pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
 - $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .
 - t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
 - These parameters are referenced to CAS leading edge in early write cycles and to WE leading edge in delayed write or read-modify-write cycles.
 - An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.
 - At least 8 CAS before RAS refresh cycles are required before using internal refresh counter.

■ WAVE FORMS

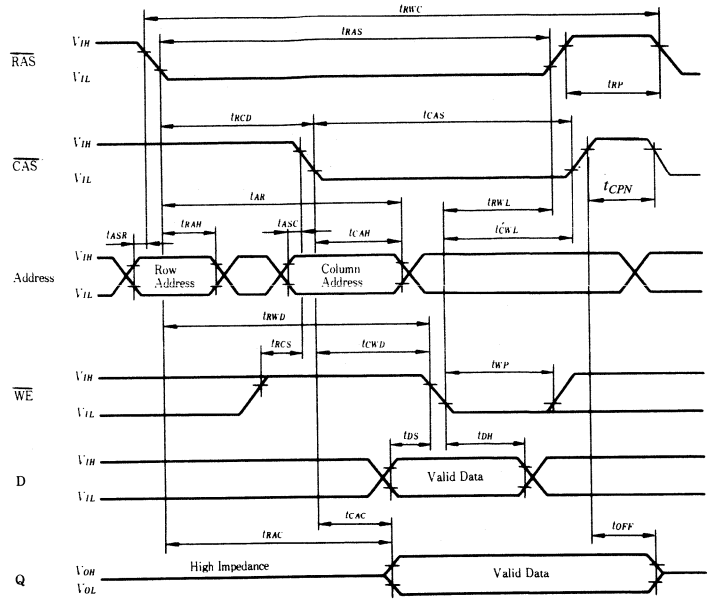
● Read Cycle



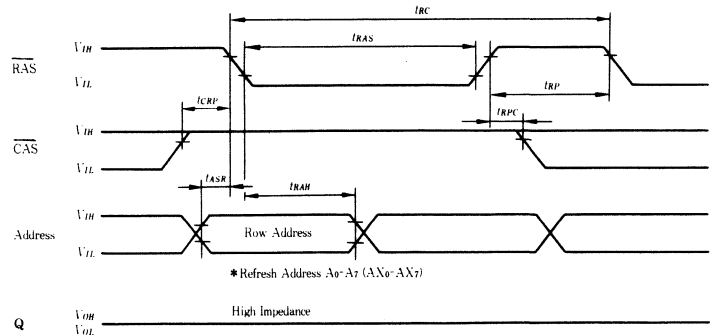
● Write Cycle



● Read Modify Write Cycle

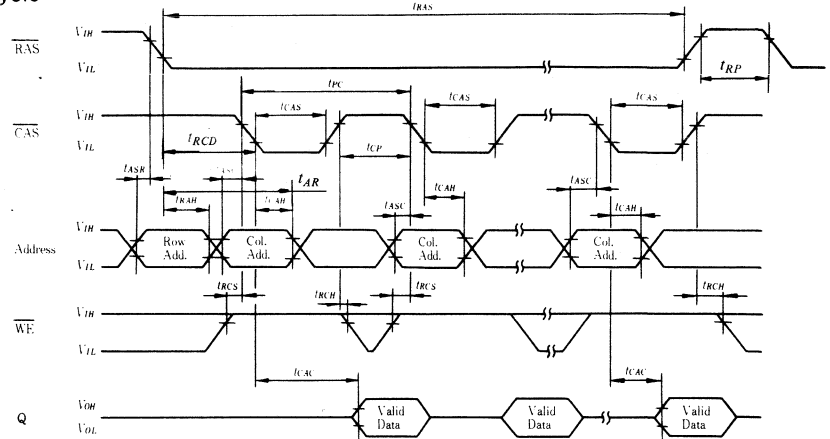


● RAS Only Refresh Cycle

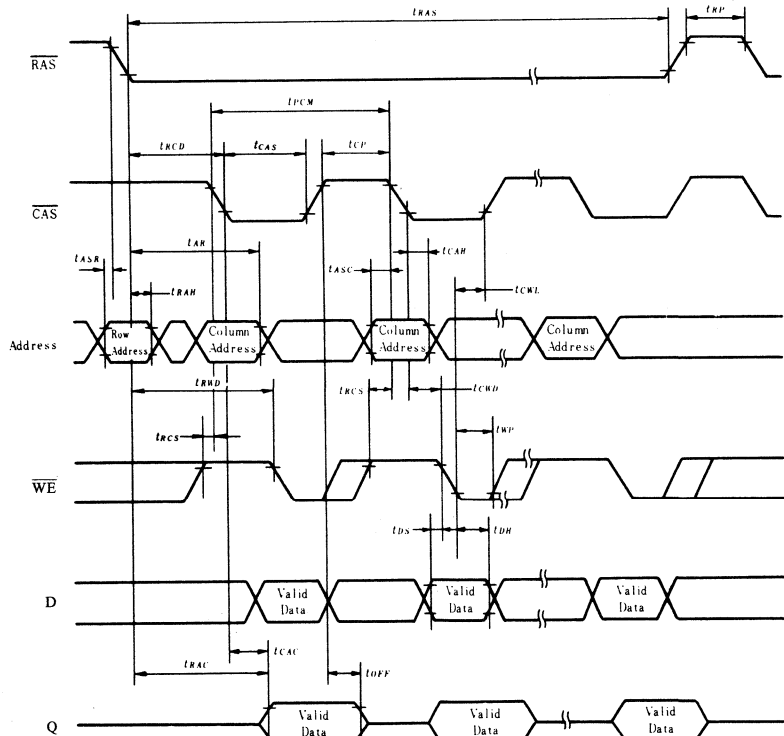


Parameter	Symbol	HB561004A-12		HB561004A-15		HB561004A-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Page Mode Supply Current	I_{CC7}	—	228	—	192	—	148	mA	
Page Mode Read or Write Cycle	t_{PC}	130	—	145	—	190	—	ns	
CAS Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns	
Page Mode Read Modify Write Cycle	t_{PCM}	175	—	195	—	250	—	ns	

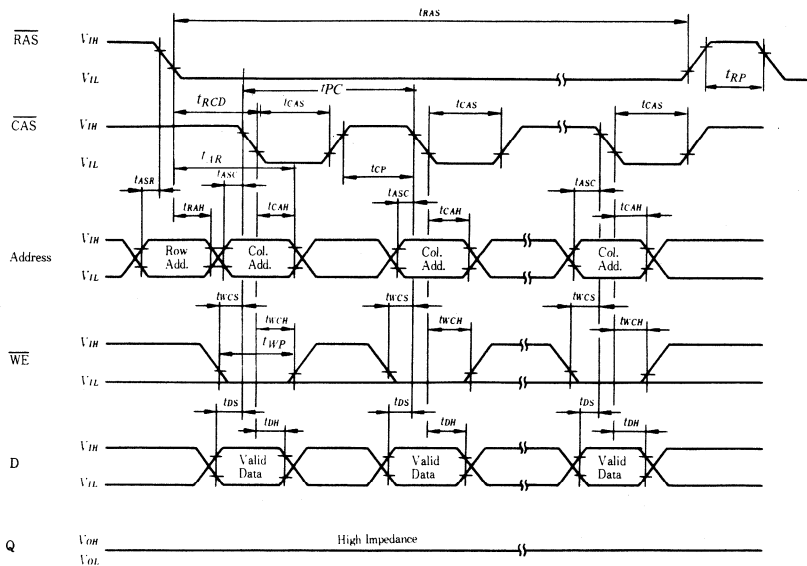
● Page Mode Read Cycle



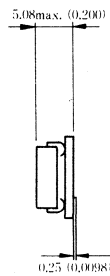
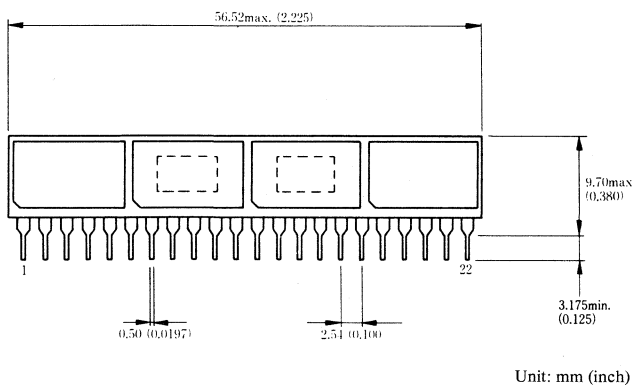
● PAGE MODE READ MODIFY WRITE CYCLE



● Page Mode Write Cycle



■ PACKAGE OUTLINE: Unit: mm(inch)



Pin No.	Name
1	A8
2	V _{CC}
3	D ₁
4	Q ₁
5	CAS
6	A7
7	A5
8	A4
9	D ₂
10	Q ₂
11	WE
12	A1
13	A3
14	A6
15	Q ₃
16	D ₃
17	A2
18	A0
19	RAS
20	D ₄
21	Q ₄
22	V _{SS}

HB561005A Series

262,144-word x 5-bit Dynamic Random Access Memory Module

The HB561005A is a 1.25M dynamic random-access memory module organized as 262,144 x 5 bits in a 24-pin single-in-line package comprising five HM50256CP, 262,144 x 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together with two decoupling capacitors mounted beneath the PLCC.

■FEATURES

- 262,144 words x 5 bits Organization
- Industry standard 24-pin Single Inline Package Memory Module
- Single 5V ($\pm 10\%$)
- Utilizes five 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561005A operates as five HM50256CP connected as shown in the functional block diagram.
- Low Power Dissipation:

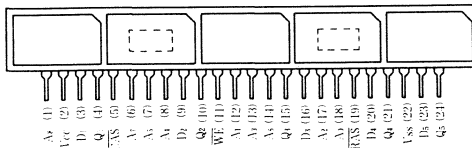
t_{RC}	Operating (typ)	Standby (typ)
220ns	1500mW	62.5mW
260ns	1250mW	
330ns	1000mW	

- High speed:

	Access Time from \overline{RAS} (max)	Access Time from \overline{CAS} (max)	Read or Write Cycle (min)	Read Modify Write Cycle (min)
HB561005A-12	120ns	70ns	220ns	265ns
HB561005A-15	150ns	75ns	260ns	310ns
HB561005A-20	200ns	100ns	330ns	390ns

- Page mode capability
- TTL compatible
- 256 refresh cycles /4ms
- 3 variations of refresh
 - \overline{RAS} only refresh
 - \overline{CAS} before \overline{RAS} refresh
 - Hidden refresh
- Operating Ambient Air Temperature: 0°C to +70°C
- Common \overline{CAS} Control with Separate Data-in and Data-out
- Decoupling Capacitors Ready Mounted on Substrate

■PIN ARRANGEMENT

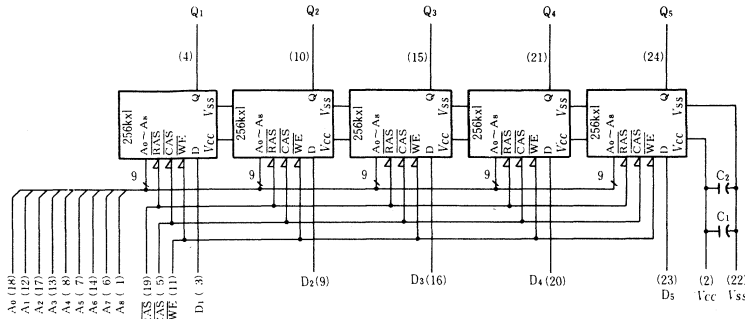


(Side View)

PIN NOMENCLATURE

A0 – A8	Address Inputs
\overline{CAS}	Column Address Strobe
D1 – D5	Data Inputs
Q1 – Q5	Data Outputs
\overline{RAS}	Row Address Strobe
\overline{WE}	Write Enable
V_{CC}	5V Supply
V_{SS}	Ground

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

- Voltage on any pin relative to V_{SS} : $-1V$ to $+7V$
- Operating temperature, T_a (Ambient): $0^{\circ}C$ to $+70^{\circ}C$
- Storage temperature (Ambient): $-55^{\circ}C$ to $+125^{\circ}C$
- Power dissipation: 5W
- Short circuit output current: 50mA

RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^{\circ}C$)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Notes: 1. All voltages referenced to V_{SS}

DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to $+70^{\circ}C$ $V_{CC}=5V \pm 10\%$, $V_{SS}=0V$)

Parameter	Symbol	min.	max.	Unit	Notes
Operating current $t_{RC}=330ns$ $t_{RC}=260ns$ $t_{RC}=220ns$	I_{CC1}	—	275 350 413	mA	1
Standby current	I_{CC2}	—	23	mA	
Refresh current $t_{RC}=330ns$ $t_{RC}=260ns$ $t_{RC}=220ns$	I_{CC3}	—	212 263 312	mA	RAS only Refresh
Standby current (Dout Enable)	I_{CC5}	—	50	mA	1
Refresh current $t_{RC}=330ns$ $t_{RC}=260ns$ $t_{RC}=220ns$	I_{CC6}	—	225 288 344	mA	CAS before RAS Refresh
Input leakage $0 < V_{in} < 7V$	I_{LI}	-10	10	μA	
Output leakage $0 < V_{out} < 7V$	I_{LO}	-10	10	μA	Dout is disabled
Output levels High ($I_{out} = -5mA$)	V_{OH}	2.4	V_{CC}	V	
Low ($I_{out} = 4.2mA$)	V_{OL}	0	0.4	V	

CAPACITANCE ($V_{CC} = 5V \pm 10\%$, $T_a = 25^{\circ}C$)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	—	40	pF	2
Clocks	C_{I2}	—	52	pF	2, 3
Q	C_O	—	12	pF	2, 3
D	C_B	—	10	pF	2

- Notes. 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 3. CAS = V_{IH} to disable D_{out} .

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

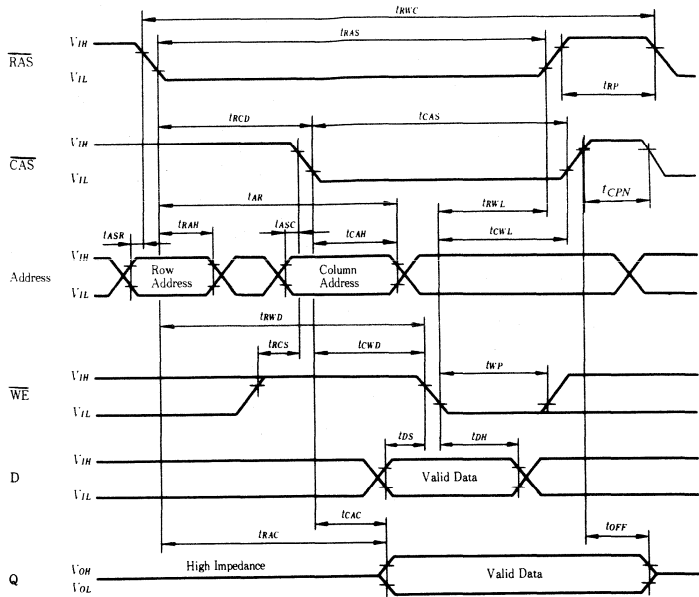
D, 10, 11)

 $(T_a = 0 \text{ to } +70^\circ\text{C}, V_{CC} = 5\text{V} \pm 10\%, V_{SS} = 0\text{V})$

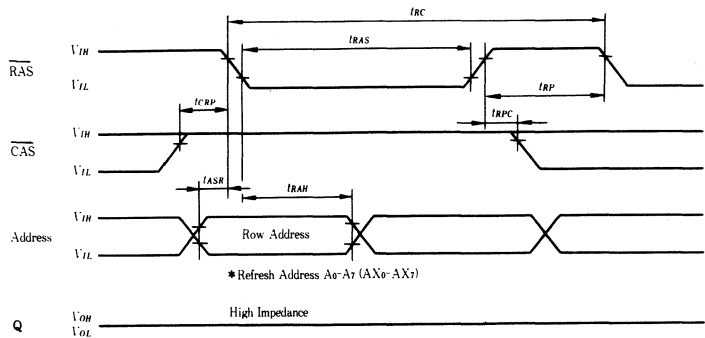
Parameter	Symbol	HB561005A-12		HB561005A-15		HB561005A-20		Unit	N te
		min.	max.	min.	max.	min.	max.		
Access Time from RAS	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from CAS	t_{CAC}	—	70	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
RAS Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
RAS Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
CAS Pulse Width	t_{CAS}	70	10000	75	10000	100	10000	ns	
RAS to CAS Delay Time	t_{RCD}	35	50	35	75	35	100	ns	7
RAS Hold Time	t_{RSH}	70	—	75	—	100	—	ns	
CAS Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
CAS to RAS Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	25	—	30	—	ns	
Column Address Hold Time referenced to RAS	t_{AR}	75	—	100	—	130	—	ns	
Read Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	45	—	45	—	55	—	ns	
Write Command Hold Time referenced to RAS	t_{WCR}	95	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	45	—	45	—	55	—	ns	
Write Command to RAS Lead Time	t_{RWL}	45	—	45	—	55	—	ns	
Write Command to CAS Lead Time	t_{CWL}	45	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	9
Data-in Hold Time	t_{DH}	45	—	45	—	55	—	ns	8, 9
Data-in Hold Time referenced to RAS	t_{DHR}	95	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to CAS	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
CAS Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
CAS Set-up Time	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to RAS Hold Time	t_{RPC}	0	—	0	—	0	—	ns	
Read-Write Cycle Time	t_{RWC}	265	—	310	—	390	—	ns	
CAS to WE Delay	t_{CWD}	70	—	75	—	100	—	ns	8
RAS to WE Delay	t_{RWD}	120	—	150	—	200	—	ns	

- Notes:
- AC measurements assume $t_T = 5\text{ns}$.
 - Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended values shown in this table t_{RAC} exceeds the value shown.
 - Measured with a load circuit equivalent to 2TTL loads and 100pF.
 - Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
 - $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
 - $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 - Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .
 - t_{WCS} , t_{CWD} and t_{RWD} are not restrictive operating parameters. They are included in the data sheet as electrical characteristics only; if $t_{WCS} \geq t_{WCS}(\text{min})$, the cycle is an early write cycle and the data output pin will remain open circuit (high impedance) throughout the entire cycle; if $t_{CWD} \geq t_{CWD}(\text{min})$ and $t_{RWD} \geq t_{RWD}(\text{min})$, the cycle is a read-write and the data output will contain data read from the selected cell; if neither of the above sets of conditions is satisfied the condition of the data out (at access time) is indeterminate.
 - These parameters are referenced to CAS leading edge in early write cycles and to $\overline{\text{WE}}$ leading edge in delayed write or read-modify-write cycles.
 - An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.
 - At least 8 CAS before RAS refresh cycles are required before using internal refresh counter.

● Read Modify Write Cycle

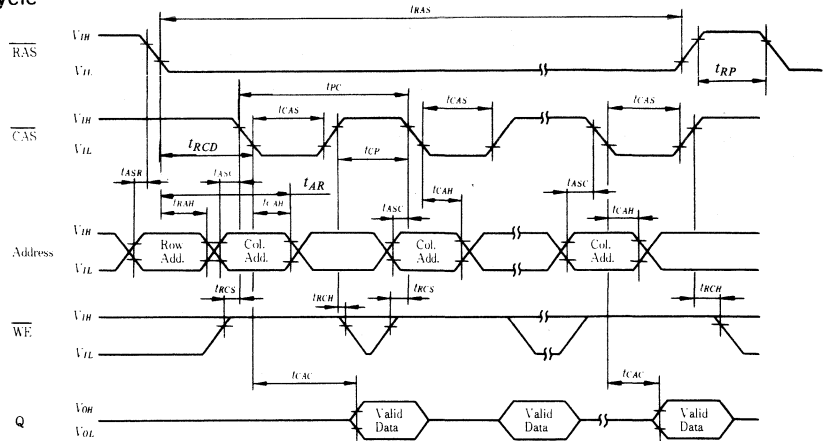


● RAS Only Refresh Cycle

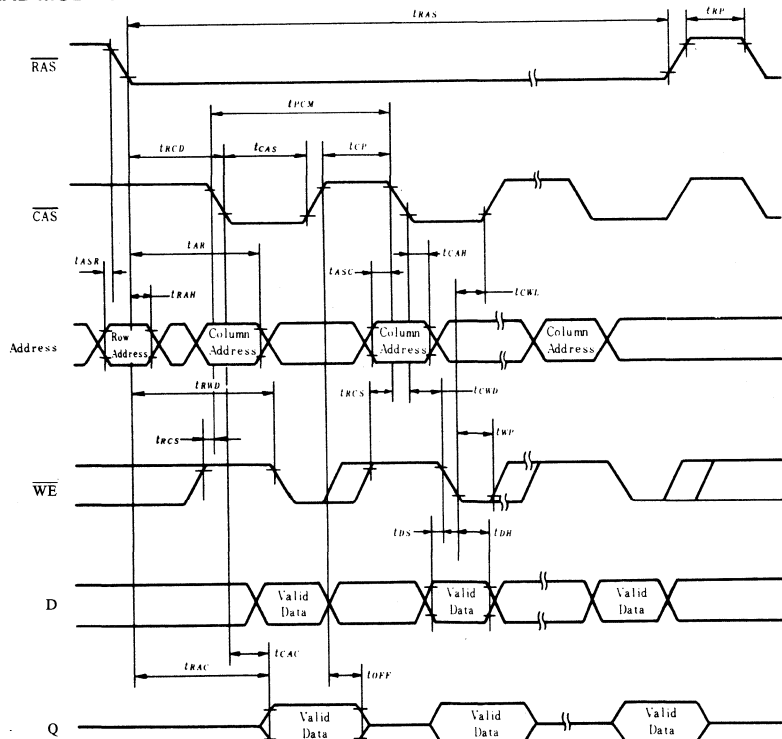


Parameter	Symbol	HB561005A-12		HB561005A-15		HB561005A-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Page Mode Supply Current	I_{CC7}	—	285	—	240	—	185	mA	
Page Mode Read or Write Cycle	t_{PC}	130	—	145	—	190	—	ns	
CAS Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns	
Page Mode Read Modify Write Cycle	t_{PCM}	175	—	195	—	250	—	ns	

● Page Mode Read Cycle



● PAGE MODE READ MODIFY WRITE CYCLE



HB561008B Series

262,144-word x 8-bit Dynamic Random Access Memory Module

The HB561008B is a 2M dynamic random-access memory module organized as 262,144 x 8 bits in a lead-less 30-pin single-in-line package comprising eight HM50256CP, 262,144 X 1 bit dynamic RAMs in 18-pin Plastic Leaded Chip Carrier mounted on top of a substrate together with decoupling capacitors mounted beneath the chip carriers.

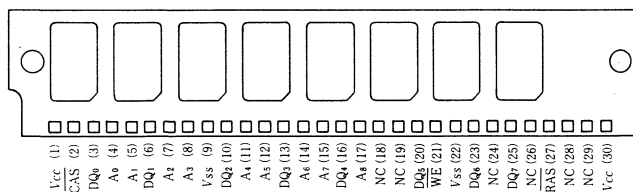
■FEATURES

- 262,144 words 8 bits Organization
- Industry standard 30-Pin Single Inline Package Memory Module
- Single 5V ($\pm 10\%$)
- Utilizes eight 256K Dynamic RAMs in PLCC (HM50256CP)
- HB561008B operates as eight HM50256CP as shown in the functional block diagram.
- Low Power; Operating: 1,920mW typ. ($t_{RC} = 260\text{ns}$)
Standby: 120mW typ.
- High speed:

	Access Time from $\overline{\text{RAS}}$ (max)	Access Time from $\overline{\text{CAS}}$ (max)	Read or Write Cycle (min)
HB561008B-12	120ns	70ns	220ns
HB561008B-15	150ns	75ns	260ns
HB561008B-20	200ns	100ns	330ns

- Page mode capability
- TTL compatible
- 256 refresh cycles: (4ms)
- 3 variations of refresh
 - $\overline{\text{RAS}}$ only refresh
 - $\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ refresh
 - Hidden refresh
- Operating Ambient Air Temperature: 0 to +70°C

■PIN ARRANGEMENT



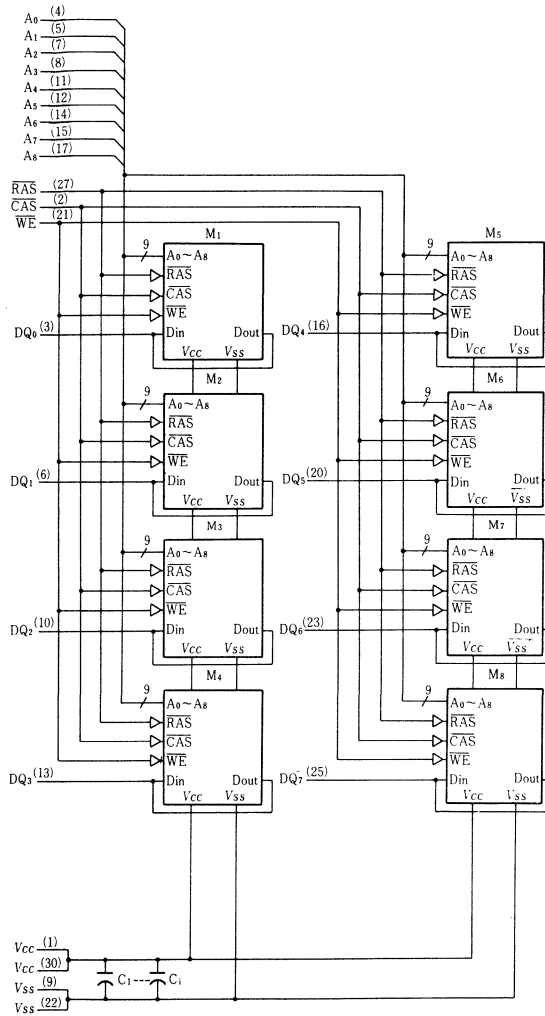
(Side View)

- Common $\overline{\text{CAS}}$ control for eight common Data-In and Data-Out lines.
- The common I/O feature dictates the use of only early write operations to prevent contention on D and Q.

PIN NOMENCLATURE

A0~A8	Address Inputs
$\overline{\text{CAS}}$	Column Address Strobes
DQ0~DQ7	Data In/Data Out
NC	No Connection
$\overline{\text{RAS}}$	Row Address Strobes
$\overline{\text{WE}}$	Write Enable
V_{cc}	+5V Supply
V_{ss}	Ground

■ FUNCTIONAL BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATING

- Voltage on any pin relative to V_{SS} : $-1V$ to $+7V$
- Operating temperature, T_a (Ambient): $0^{\circ}C$ to $+70^{\circ}C$
- Storage temperature (Ambient): $-55^{\circ}C$ to $+125^{\circ}C$
- Power dissipation: 8W
- Short circuit output current: 50mA

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a=0$ to $+70^{\circ}C$)

Parameter	Symbol	min.	typ.	max.	Unit	Notes
Supply Voltage	V_{CC}	4.5	5.0	5.5	V	1
Input High Voltage	V_{IH}	2.4	—	6.5	V	1
Input Low Voltage	V_{IL}	-1.0	—	0.8	V	1

Notes: 1. All voltages referenced to V_{SS}

DC ELECTRICAL CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}+10\%$, $V_{SS}=0\text{V}$)

Parameter		Symbol	min.	max.	Unit	Notes
Operating current	$t_{RC}=330\text{ns}$	I_{CC1}	—	440	mA	1
	$t_{RC}=260\text{ns}$			560		
	$t_{RC}=220\text{ns}$			660		
Standby current		I_{CC2}	—	36	mA	
Refresh current	$t_{RC}=330\text{ns}$	I_{CC3}	—	335	mA	$\overline{\text{RAS}}$ only Refresh
	$t_{RC}=260\text{ns}$			425		
	$t_{RC}=220\text{ns}$			495		
Standby current (Dout Enable)		I_{CC5}	—	80	mA	1
Refresh current	$t_{RC}=330\text{ns}$	I_{CC6}	—	360	mA	$\overline{\text{CAS}}$ before $\overline{\text{RAS}}$ Refresh
	$t_{RC}=260\text{ns}$			465		
	$t_{RC}=220\text{ns}$			550		
Input leakage	$0 < V_{out} < 7\text{V}$	I_{LI}	-10	10	μA	
Output leakage	$0 < V_{in} < 7\text{V}$	I_{LO}	-10	10	μA	Dout is disabled
Output levels	High ($I_{out} = -5\text{mA}$)	V_{OH}	2.4	V_{CC}	V	
	Low ($I_{out} = 4.2\text{mA}$)	V_{OL}	0	0.4	V	

CAPACITANCE ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 25^\circ\text{C}$)

Parameter	Symbol	typ.	max.	Unit	Notes
Address	C_{I1}	—	55	pF	2
Clocks	C_{I2}	—	70	pF	2, 3
DQ	$C_{I/O}$	—	17	pF	2, 3

- Notes: 1. I_{CC} depends on output loading condition when the device is selected, I_{CC} max is specified at the output open condition.
 2. Capacitance measured with Boonton Meter or effective capacitance measuring method.
 3. $\overline{\text{CAS}} = V_{IH}$ to disable D_{Out} .

ELECTRICAL CHARACTERISTICS AND RECOMMENDED AC OPERATING CONDITIONS

 ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 10\%$, $V_{SS}=0\text{V}$)^{1), 9), 10)}

Parameter	Symbol	HB561008B-12		HB561008B-15		HB561008B-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Access Time from $\overline{\text{RAS}}$	t_{RAC}	—	120	—	150	—	200	ns	2, 3
Access Time from $\overline{\text{CAS}}$	t_{CAC}	—	70	—	75	—	100	ns	3, 4
Output Buffer Turn-off Delay	t_{OFF}	—	30	—	40	—	50	ns	5
Transition Time (Rise and Fall)	t_T	3	50	3	50	3	50	ns	6
Random Read or Write Cycle Time	t_{RC}	220	—	260	—	330	—	ns	
$\overline{\text{RAS}}$ Precharge Time	t_{RP}	90	—	100	—	120	—	ns	
$\overline{\text{RAS}}$ Pulse Width	t_{RAS}	120	10000	150	10000	200	10000	ns	
$\overline{\text{CAS}}$ Pulse Width	t_{CAS}	70	10000	75	10000	100	10000	ns	
$\overline{\text{RAS}}$ to $\overline{\text{CAS}}$ Delay Time	t_{RCD}	35	50	35	75	35	100	ns	7
$\overline{\text{RAS}}$ Hold Time	t_{RSH}	70	—	75	—	100	—	ns	
$\overline{\text{CAS}}$ Hold Time	t_{CSH}	120	—	150	—	200	—	ns	
$\overline{\text{CAS}}$ to $\overline{\text{RAS}}$ Precharge Time	t_{CRP}	10	—	10	—	10	—	ns	
Row Address Set-up Time	t_{ASR}	0	—	0	—	0	—	ns	
Row Address Hold Time	t_{RAH}	15	—	15	—	20	—	ns	
Column Address Set-up Time	t_{ASC}	0	—	0	—	0	—	ns	
Column Address Hold Time	t_{CAH}	25	—	25	—	30	—	ns	
Column Address Hold Time referenced to $\overline{\text{RAS}}$	t_{AR}	75	—	100	—	130	—	ns	
Read Command Set-up Time	t_{WCS}	0	—	0	—	0	—	ns	8
Write Command Hold Time	t_{WCH}	45	—	45	—	55	—	ns	
Write Command Hold Time referenced to $\overline{\text{RAS}}$	t_{WCR}	95	—	120	—	155	—	ns	
Write Command Pulse Width	t_{WP}	45	—	45	—	55	—	ns	
Write Command to $\overline{\text{RAS}}$ Lead Time	t_{RWL}	45	—	45	—	55	—	ns	
Write Command to $\overline{\text{CAS}}$ Lead Time	t_{CWL}	45	—	45	—	55	—	ns	
Data-in Set-up Time	t_{DS}	0	—	0	—	0	—	ns	

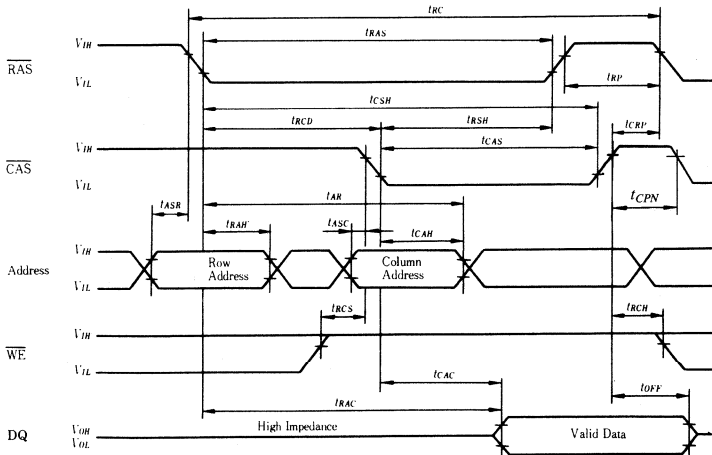
(to be continued)

Parameter	Symbol	HB561008B-12		HB561008B-15		HB561008B-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Data-in Hold Time	t_{DH}	45	—	45	—	55	—	ns	
Data-in Hold Time referenced to RAS	t_{DHR}	95	—	120	—	155	—	ns	
Read Command Set-up Time	t_{RCS}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to $\overline{\text{CAS}}$	t_{RCH}	0	—	0	—	0	—	ns	
Read Command Hold Time referenced to RAS	t_{RRH}	10	—	10	—	10	—	ns	
Refresh Period	t_{REF}	—	4	—	4	—	4	ms	
CAS Precharge Time	t_{CPN}	50	—	60	—	80	—	ns	
CAS Set-up Time	t_{CSR}	10	—	10	—	10	—	ns	
CAS Hold Time (CAS before RAS)	t_{CHR}	120	—	150	—	200	—	ns	
RAS Precharge to RAS Hold Time	t_{RPC}	0	—	0	—	0	—	ns	

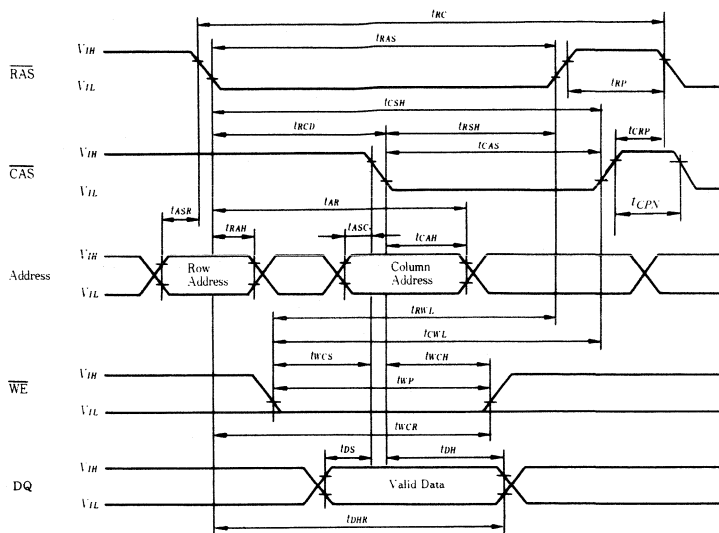
- Notes:
1. AC measurements assume $t_T = 5\text{ns}$.
 2. Assumes that $t_{RCD} \leq t_{RCD}(\text{max})$. If t_{RCD} is greater than the maximum recommended value shown in this table, t_{RAC} exceeds the value shown.
 3. Measured with a load circuit equivalent to 2TTL loads and 100pF.
 4. Assumes that $t_{RCD} \geq t_{RCD}(\text{max})$.
 5. $t_{OFF}(\text{max})$ defines the time at which the output achieves the open circuit condition and output voltage levels are not referred.
 6. $V_{IH}(\text{min})$ and $V_{IL}(\text{max})$ are reference levels for measuring timing of input signals. Also, transition times are measured between V_{IH} and V_{IL} .
 7. Operation with the $t_{RCD}(\text{max})$ limit insures that $t_{RAC}(\text{max})$ can be met. $t_{RCD}(\text{max})$ is specified as a reference point only; if t_{RCD} is greater than the specified $t_{RCD}(\text{max})$ limit, access time is controlled exclusively by t_{CAC} .
 8. An initial pause of 100 μs is required after power-up. Then execute at least 8 initialization cycles.
 9. At least 8 CAS before RAS refresh cycles are required before using internal refresh counter.

■ WAVE FORMS

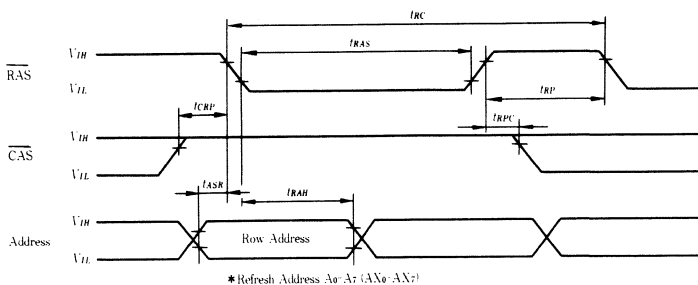
● Read Cycle



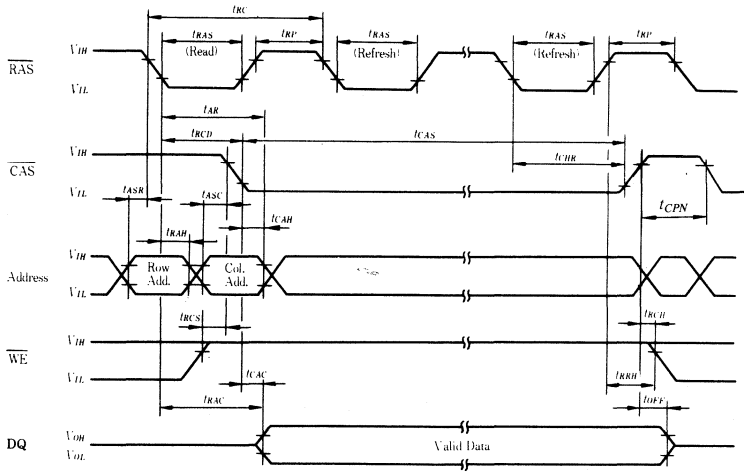
● Write Cycle



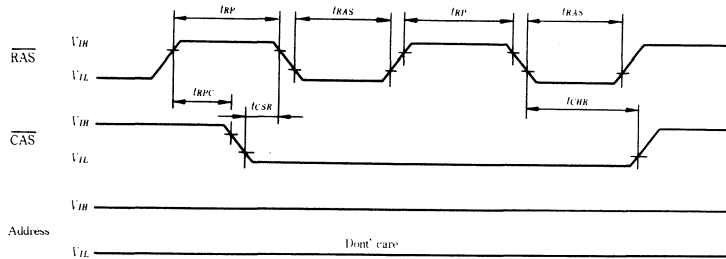
● $\overline{\text{RAS}}$ Only Refresh Cycle



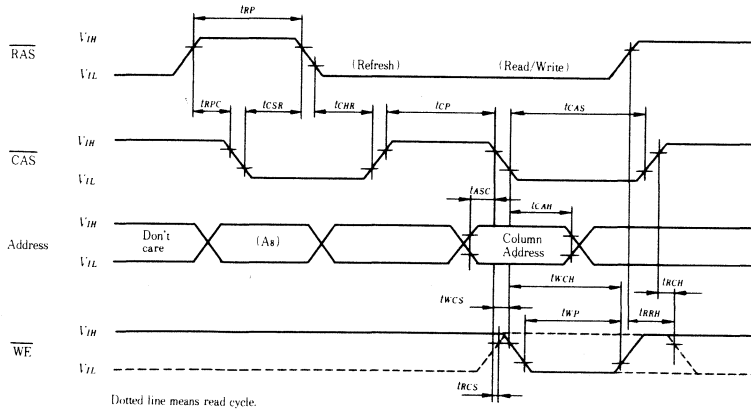
● Hidden Refresh Cycle



● CAS Before RAS Refresh Cycle

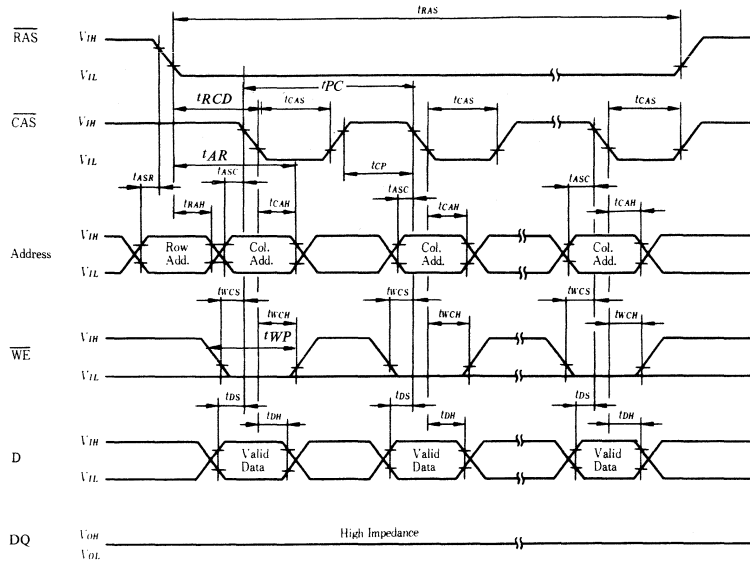


● COUNTER TEST

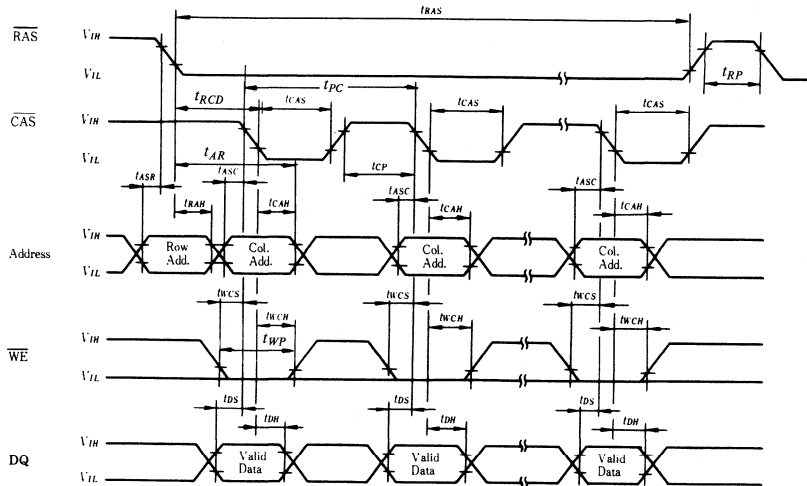


Parameter	Symbol	HB561008B-12		HB561008B-15		HB561008B-20		Unit	Note
		min.	max.	min.	max.	min.	max.		
Page Mode Supply Current	I_{CC7}	—	455	—	385	—	295	mA	
Page Mode Read or Write Cycle	t_{PC}	130	—	145	—	190	—	ns	
CAS Precharge Time, Page Cycle	t_{CP}	50	—	60	—	80	—	ns	

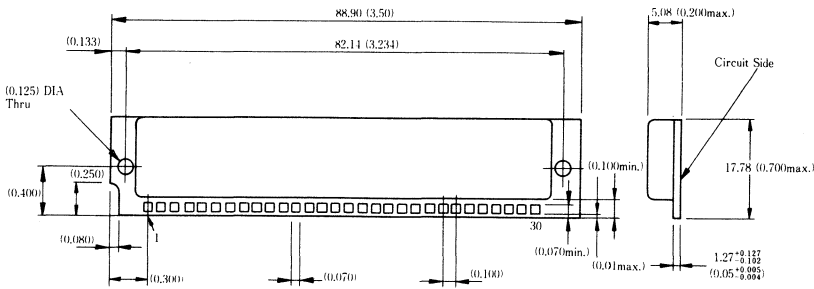
● Page Mode Read Cycle



● Page Mode Write Cycle



■ PACKAGE OUTLINE; Unit: mm (inch)



Note) Contact pads are overcoated with Tin/Lead.

Unit: mm (inch)

V_{CC}	1
\overline{CAS}	2
DQ0	3
A0	4
A1	5
DQ1	6
A2	7
A3	8
V_{SS}	9
DQ2	10
A4	11
A5	12
DQ3	13
A6	14
A7	15
DQ4	16
A8	17
NC	18
NC	19
DQ5	20
WE	21
V_{SS}	22
DQ6	23
NC	24
DQ7	25
NC	26
RAS	27
NC	28
NC	29
V_{CC}	30

MOS MASK ROM

HN61364P, HN61364FP

8192-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN61364P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

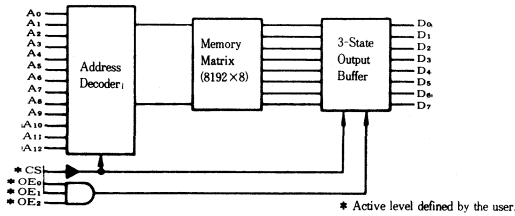
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS, OE₀ ~ OE₂ inputs and the memory content are defined by the user. The Chip Select input deselects the output and puts the chip in a powerdown mode.

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby 5μW (typ), Operation 50mW (typ)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V_T	-0.3 to +7.0	V
Operating Temperature	T_{opr}	-20 to +75	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (under Bias)	T_{bias}	-20 to +85	°C

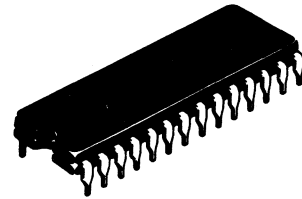
* with respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage *	V_{CC}	4.5	5.0	5.5	V
Input Voltage *	V_{IL}	-0.3	-	0.8	V
	V_{IH}	2.2	-	V_{CC}	V
Operating Temperature	T_{opr}	-20	-	75	°C

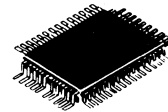
* with respect to V_{SS}

HN61364P



(DP-28)

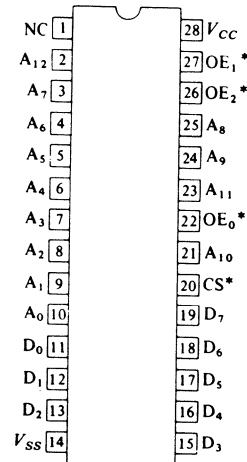
HN61364FP



(FP-54)

■ PIN ARRANGEMENT

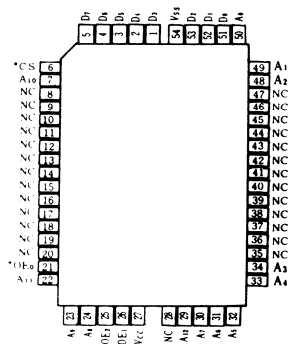
● HN61364P



(Top View)

* Mask Programmable

● HN61364FP



(Top View)

* Mask Programmable

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test Condition	min	typ**	max	Unit	
Input High-level Voltage	V_{IH}		2.2	—	V_{CC}	V	
Input Low-level Voltage	V_{IL}		-0.3	—	0.8	V	
Output High-level Voltage	V_{OH}	$I_{OH} = -205\mu A$	2.4	—	—	V	
Output Low-level Voltage	V_{OL}	$I_{OL} = 3.2mA$	—	—	0.4	V	
Input Leakage Current	I_{LI}	$V_{in} = 0$ to $5.5V$	—	—	2.5	μA	
Output High-level Leakage Current	I_{LOH}	$V_{out} = 2.4V$, $CS = 0.8V$, $\overline{CS} = 2.2V$	—	—	10	μA	
Output Low-level Leakage Current	I_{LOL}	$V_{out} = 0.4V$, $CS = 0.8V$, $\overline{CS} = 2.2V$	—	—	10	μA	
Supply Current	Active	I_{CC}^*	$V_{CC} = 5.5V$, $I_{out} = 0mA$, $t_{RC} = \text{min}$, $\text{duty} = 100\%$	—	10	25	mA
	Standby	I_{SB}	$V_{CC} = 5.5V$, $CS \geq V_{CC} - 0.2V$, $CS \leq 0.2V$	—	1	30	μA
Input Capacitance	C_{in}^{***}	$V_{in} = 0V$, $f = 1MHz$, $T_a = 25^\circ C$	—	—	10	pF	
Output Capacitance	C_{out}^{***}		—	—	15	pF	

* Steady state current ** $V_{CC} = 5V$, $T_a = 25^\circ C$

*** This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (READ CYCLE)

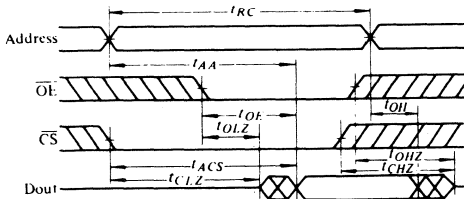
($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20$ to $+75^\circ C$, $t_r = t_f = 20ns$)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}^*	0	100	ns
Output Disable to Output in High Z	t_{OHZ}^*	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

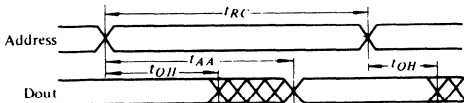
* t_{CHZ} and t_{OHZ} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

■ TIMING WAVEFORM

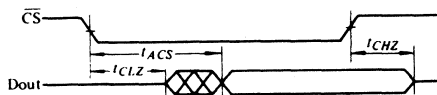
● Read Cycle (1)



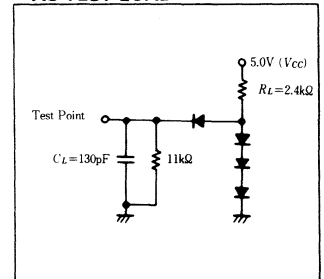
● Read Cycle (2) Notes 1, 3



● Read Cycle (3) Notes 2, 3



● AC TEST LOAD



- Notes 1. $t_r = t_f = 20ns$
- 2. C_L includes jig capacitance.
- 3. All diodes are 1S2074Ⓢ.

NOTES:

- 1. Device is continuously selected.
- 2. Address Valid prior to or coincident with CS transition low.
- 3. $OE = V_{IL}$
- 4. Input pulse level: 0.8 to 2.4V
- 5. Input and output reference level: 1.5V

HN61365P

8192-word x 8-bit CMOS Mask Programmable Read Only Memory

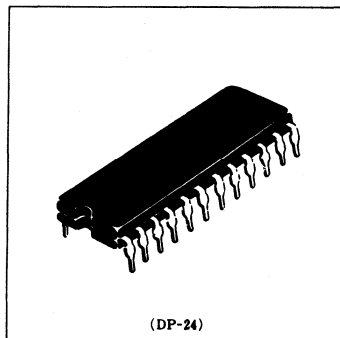
The HN61365P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS input and the memory content are defined by the user. The chip select input deselected the output and puts the chip in a power-down mode.

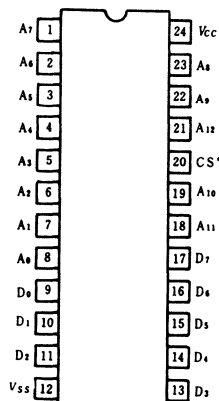
FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5 V Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation; Standby $5\mu\text{W}$ (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM



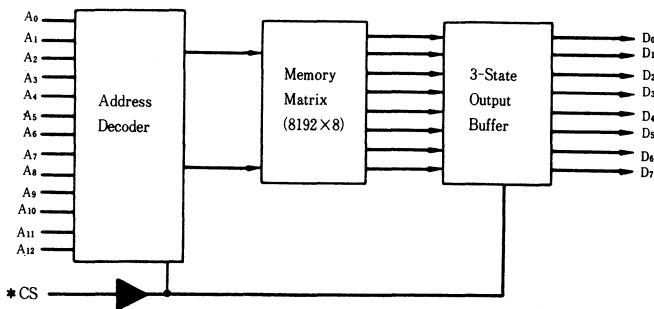
(DP-24)

PIN ARRANGEMENT



(Top View)

BLOCK DIAGRAM



* Active level defined by the user.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V_I	-0.3 to +7.0	V
Operating Temperature	T_{op}	-20 to +75	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (under bias)	T_{stg}	-20 to +85	°C

* with respect to V_{SS}

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	-0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	-20	—	75	°C

* With respect to V_{SS}

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-20$ to $+75^\circ C$)

Item	Symbol	Test Conditions	min	typ**	max	Unit
Input Voltage	V_{IH}		2.2	—	V_{CC}	V
	V_{IL}		-0.3	—	0.8	V
Output Voltage	V_{OH}	$I_{OH} = -205\mu A$	2.4	—	—	V
	V_{OL}	$I_{OL} = 3.2mA$	—	—	0.4	V
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim 5.5V$	—	—	2.5	μA
Output Leakage Current	I_{LOH}	$CS = 0.8V, \overline{CS} = 2.2V$	$V_{out} = 2.4V$	—	10	μA
	I_{LOL}		$V_{out} = 0.4V$	—	10	μA
Active Supply Current	I_{CC}^*	$V_{CC} = 5.5V, I_{OUT} = 0mA, f_{rc} = \text{min}, \text{duty} = 100\%$	—	10	25	mA
Stand by Supply Current	I_{SB}	$\overline{CS} \geq V_{CC} - 0.2V, CS \leq 0.2V, V_{CC} = 5.5V$	—	1	30	μA
Input Capacitance	C_{in}^{***}	$V_{in} = 0V, f = 1MHz, T_a = 25^\circ C$	—	—	10	pF
Output Capacitance	C_{out}^{***}		—	—	15	pF

* Steady state current ** $V_{CC} = 5V, T_a = 25^\circ C$ *** This parameter is sampled and not 100% tested.

AC CHARACTERISTICS

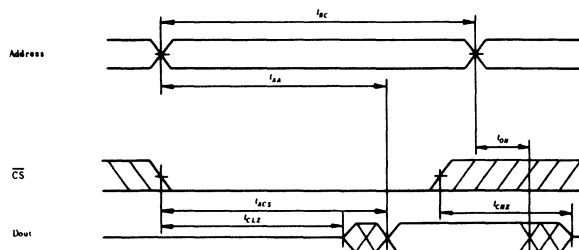
READ CYCLE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-20$ to $+75^\circ C$, $t_r = t_f = 20ns$)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}^*	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

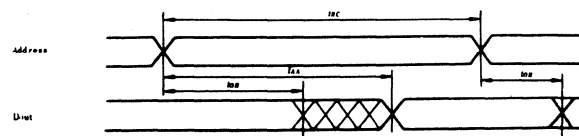
* t_{CHZ} define the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

TIMING WAVEFORM

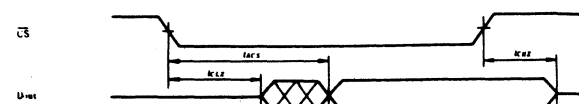
READ CYCLE (1)



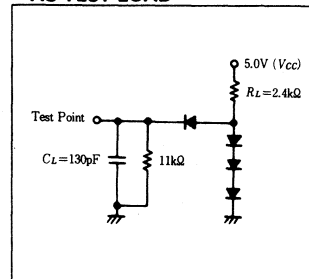
READ CYCLE (2) (Notes 1)



READ CYCLE (3) (Notes 2)



AC TEST LOAD



- Notes) 1. $t_r = t_f = 20ns$.
- 2. C_L includes jig capacitance.
- 3. All diodes are 1S2074Ⓢ.

- Notes)
- 1. Device is continuously selected
- 2. Address Valid prior to or coincident with \overline{CS} transition low.
- 3. Input pulse level : 0.8 to 2.4V
- 4. Input and output timing reference level : 1.5V

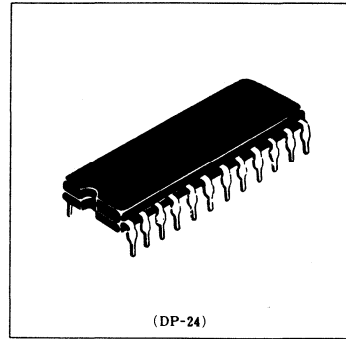
HN61366P

8192-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN61366P is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the OE input and the memory content are defined by the user.

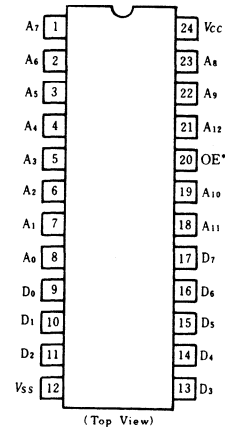


(DP-24)

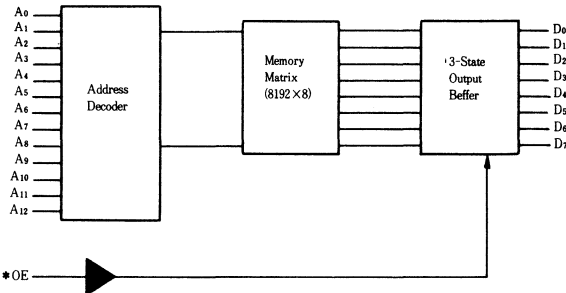
FEATURES

- Fully Static Operation
- Single +5V power supply
- Three-State Data Output for OR-Ties
- Mask Programmable Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Operation; 50mW (typ.)
- Pin Compatible with EPROM

PIN ARRANGEMENT



BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V_I	-0.3 to +7.0	V
Operating Temperature	T_{opr}	-20 to +75	°C
Storage Temperature	T_{stg}	-55 to +125	°C
Storage Temperature (under bias)	T_{bias}	-20 to +85	°C

* With respect to V_{SS}

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	-0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	-20	—	75	°C

* With respect to V_{SS}

ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-20$ to $+75^\circ C$)

Item	Symbol	Test Conditions	min	typ**	max	Unit
Input Voltage	V_{IH}		2.2	—	V_{CC}	V
	V_{IL}		-0.3	—	0.8	V
Output Voltage	V_{OH}	$I_{OH} = -205 \mu A$	2.4	—	—	V
	V_{OL}	$I_{OL} = 3.2 mA$	—	—	0.4	V
Input Leakage Current	I_{LI}	$V_{IN} = 0 \sim 5.5V$	—	—	2.5	μA
Output Leakage Current	I_{LOH}	$OE = 0.8V, \overline{OE} = 2.2V$	$V_{OUT} = 2.4V$		10	μA
	I_{LOL}		$V_{OUT} = 0.4V$		10	μA
Operating Supply Current	I_{CC}^*	$V_{CC} = 5.5V, I_{OUT} = 0mA, t_{RC} = \min$	—	10	25	mA
Input Capacitance	C_{in}^{***}	$V_{in} = 0V, f = 1MHz, T_a = 25^\circ C$	—	—	10	pF
Output Capacitance	C_{out}^{***}		—	—	15	pF

* Steady state current ** $V_{CC}=5V, T_a=25^\circ C$
 *** This parameter is sampled and not 100% tested.

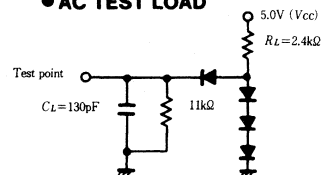
AC CHARACTERISTICS

READ CYCLE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=-20 \sim +75^\circ C$, $t_r=t_f=20ns$)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Output Disable to Output in High Z	t_{OHZ}^*	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

* t_{OHZ} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

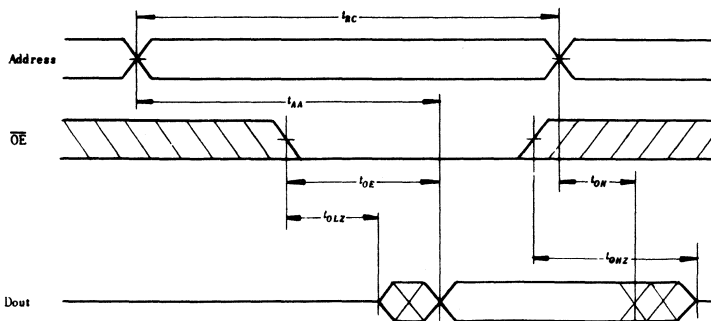
AC TEST LOAD



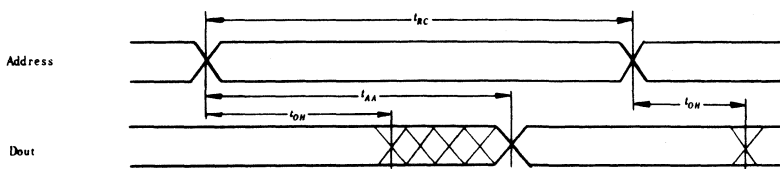
Notes) 1. $t_r=t_f=20ns$
 2. C_L includes jig capacitance.
 3. All diodes are 1S2074(Φ).

TIMING WAVEFORM

READ CYCLE (1)



READ CYCLE (2) ^{Note 1)}



Note) 1. $\overline{OE} = V_{IL}$
 2. Input pulse level : 0.8 to 2.4V
 3. Input and output timing reference level : 1.5V

HN613128P, HN613128FP

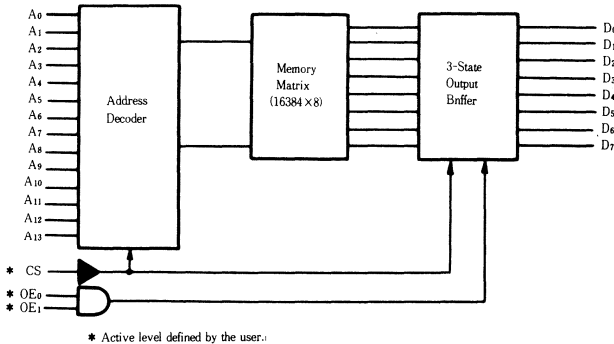
16384-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN613128P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the CS, OE₀, OE₁ input and the memory content are defined by the user. The Chip Select input deselected the output and puts the chip in a power-down mode.

FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-State Data Output for OR-Ties
- Mask Programmable Chip Select, Output Enable
- TTL Compatible
- Maximum Access Time; 250ns
- Low Power Standby and Low Power Operation;
 - Standby: 5μW (typ.)
 - Operation: 50mW (typ.)
- Pin Compatible with EPROM

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V _{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V _I	-0.3 to +7.0	V
Operating Temperature Range	T _{opr}	-20 to +75	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C
Storage Temperature Range (under bias)	T _{bias}	-20 to +85	°C

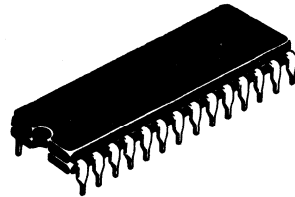
* With respect to V_{SS}.

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V _{CC}	4.5	5.0	5.5	V
Input Voltage*	V _{IL}	-0.3	—	0.8	V
	V _{IH}	2.2	—	V _{CC}	V
Operating Temperature	T _{opr}	-20	—	75	°C

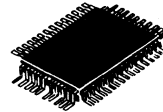
* With respect to V_{SS}.

HN613128P



(DP-28)

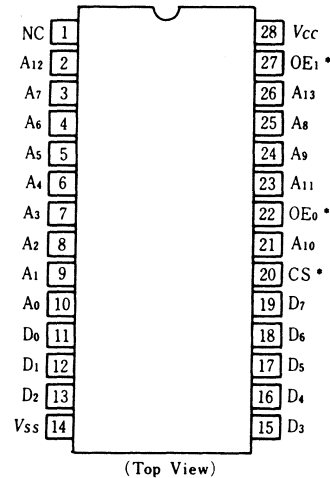
HN613128FP



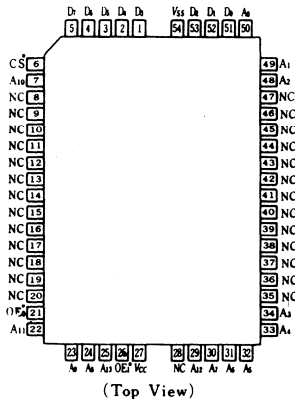
(FP-54)

PIN ARRANGEMENT

HN613128P



HN613128FP



■ ELECTRICAL CHARACTERISTICS ($V_{CC}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a = -20$ to $+75^\circ C$)

Item	Symbol	Test Condition	min	typ**	max	Unit
Input High-level Voltage	V_{IH}		2.2	—	V_{CC}	V
Input Low-level Voltage	V_{IL}		-0.3	—	0.8	V
Output High-level Voltage	V_{OH}	$I_{OH} = -205 \mu A$	2.4	—	—	V
Output Low-level Voltage	V_{OL}	$I_{OL} = 3.2 mA$	—	—	0.4	V
Input Leakage Current	I_{LI}	$V_a = 0$ to $5.5V$	—	—	2.5	μA
Output High-level Leakage Current	I_{LOH}	$V_{out} = 2.4V$, $CS = 0.8V$, $\overline{CS} = 2.2V$	—	—	10	μA
Output Low-level Leakage Current	I_{LOL}	$V_{out} = 0.4V$, $CS = 0.8V$, $\overline{CS} = 2.2V$	—	—	10	μA
Supply Current (Active/Standby)	I_{CC}^*/I_a	$V_{CC}=5.5V$, $I_{OUT}=0mA$, $t_{bc} = \min$, $duty = 100\%$, $\overline{CS} \cong V_{CC} - 0.2V$, $CS \leq 0.2V$	—	10/1	25/30	mA/ μA
Input Capacitance	C_{in}^{***}	$V_a = 0V$, $f = 1.0MHz$, $T_a = 25^\circ C$	—	—	10	pF
Output Capacitance	C_{out}^{***}	$V_a = 0V$, $f = 1.0MHz$, $T_a = 25^\circ C$	—	—	15	pF

* Steady state current ** $V_{CC}=5V$, $T_a=25^\circ C$

*** This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS (READ CYCLE)

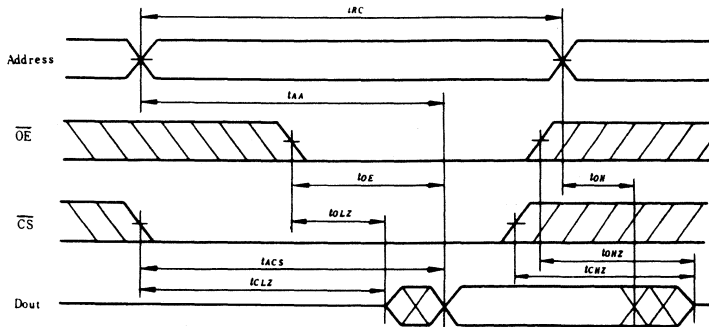
($V_{CC}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a = -20$ to $+75^\circ C$, All timing with $t_r = t_f = 20ns$)

Item	Symbol	HN613128P		Unit
		min	max	
Read Cycle Time	t_{RC}	250	—	ns
Address Access Time	t_{AA}	—	250	ns
Chip Select Access Time	t_{ACS}	—	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip deselection to Output in High Z	t_{CHZ}^*	0	100	ns
Output Disable to Output in High Z	t_{OHZ}^*	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

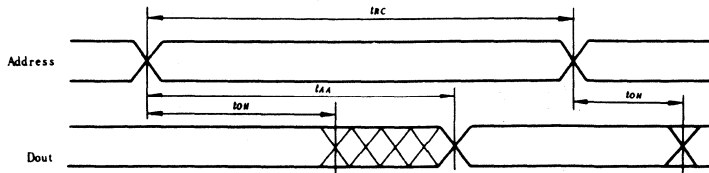
* t_{CHZ} and t_{OHZ} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

■ TIMING WAVEFORM

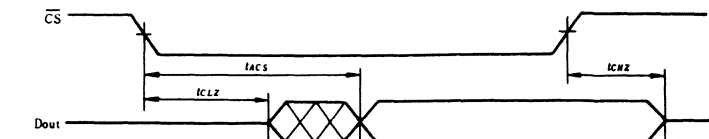
● READ CYCLE (1)



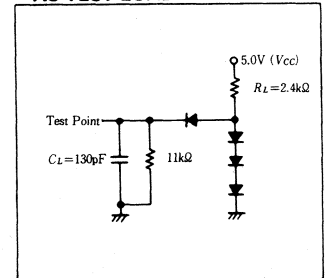
● READ CYCLE (2) (Notes 1, 3)



● READ CYCLE (3) (Notes 2, 3)



● AC TEST LOAD



- Notes) 1. $t_r = t_f = 20ns$.
- 2. C_L includes jig capacitance.
- 3. All diodes are 1S2074(□).

NOTES:

1. Device is continuously selected.
2. Address Valid prior to or coincide with \overline{CS} transition low.
3. $OE = V_{IL}$.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level 1.5V

HN61256P, HN61256FP

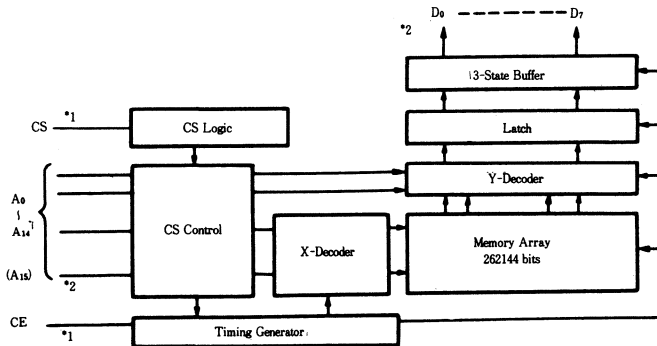
32768×8-bit or 65536×4-bit CMOS Mask Programmable Read Only Memory

The Hitachi HN61256P/FP is a mask programmable 32768 x 8-bit or 65536x4-bit CMOS read only memory. It operates from a single power supply and is compatible with TTL. Low power consumption makes this memory well-suited for battery-operation or hand-held personal computers. Memory expansion can be implemented through one chip select input. Either active "High" or active "Low" or chip select input and a chip enable input are defined at mask level. The organization of 8 bit or 4 bit is defined by the user.

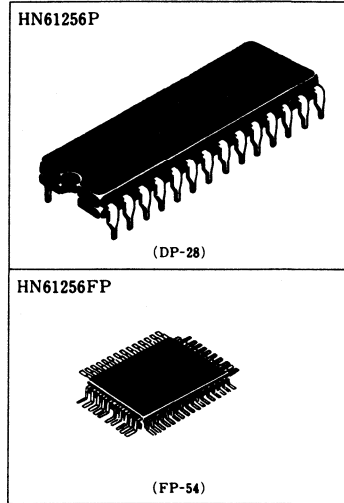
■ FEATURES

- Mask-programmable selection of either 4-bit or 8-bit organization
- Three-state outputs, can be wire-ORed.
- One mask programmable chip select terminal facilitates memory expansion.
- A single 5V power supply ($\pm 10\%$)
- Low power consumption: Operation 7.5mW (typ.), Standby 5 μ W (typ.)
- TTL compatible
- Access time: 3.5 μ s (max)

■ BLOCK DIAGRAM

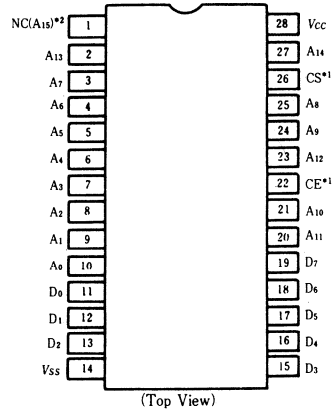


- *1 Active level defined at mask level.
 - *2 Mask programmable selection of either 4-bit or 8-bit organization.
- In 4-bit organization, data outputs are D₀ to D₃.

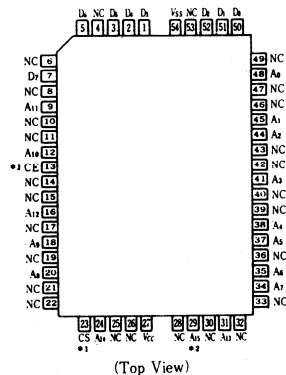


■ PIN ARRANGEMENT

● HN61256P



● HN61256FP



- *1. Active level defined by user
- *2. Upper address of 4-bit organization.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage*	V_{CC}	-0.3~+7.0	V
All Input and output Voltage*	V_I	-0.3~ V_{CC}	V
Operating Temperature Range	T_{opr}	0~+75	°C
Storage Temperature Range	T_{stg}	-55~+125	°C
Bias Storage Temperature Range	T_{bias}	-20~+85	°C

Note: * Referenced to V_{SS} .

■ ELECTRICAL CHARACTERISTICS

($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0 \sim +75^\circ C$)

Item	Symbol	Test Conditions	min	typ**	max	Unit
Input "High" Level Voltage	V_{IH}		2.4	—	V_{CC}	V
Input "Low" Level Voltage	V_{IL}		0	—	0.8	V
Output "High" Level Voltage	V_{OH}	$I_{OH} = -100 \mu A$	2.4	—	—	V
Output "Low" Level Voltage	V_{OL}	$I_{OL} = 1.6 mA$	—	—	0.4	V
Input Leakage Current	I_{LI}	$V_{in} = 0 \sim 5.5V$	—	—	2.5	μA
Output "High" Level Leakage Current	I_{LOH}	$CE = 0.8V$	—	—	5	μA
Output "Low" Level Leakage Current	I_{LOL}	$CE = 2.4V$	—	—	5	μA
Supply Current	In stand-by	$CS \geq V_{CC} - 0.2V$, $CS \leq 0.2V$	—	1	30	μA
	In operation	I_{CC}^*	—	1.5	3.0	mA
Input Capacitance	C_{in}^{***}	$V_{in} = 0V, f = 1MHz, T_a = 25^\circ C$	—	—	10	pF
Output Capacitance	C_{out}^{***}		—	—	12.5	pF

* Steady state current ** $V_{CC}=5V, T_a=25^\circ C$

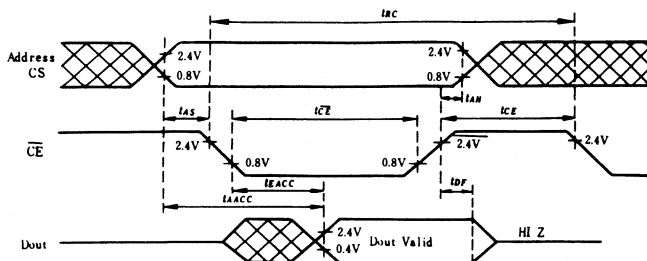
*** This parameter is sampled and not 100% tested.

■ AC CHARACTERISTICS

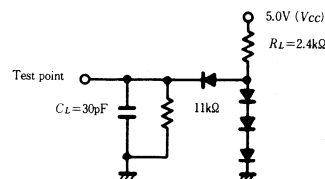
● READ CYCLE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0 \sim +75^\circ C$, $t_r = t_f = 20ns$)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	4.0	—	μs
Address Access Time	t_{AACC}	—	3.5	μs
Chip Enable Access Time	t_{EACC}	—	3.0	μs
Data Hold Time from Address	t_{DF}^*	0.05	0.5	μs
Address Set-up Time	t_{AS}	0.5	—	μs
Address Hold Time	t_{AH}	0	—	μs
Chip Enable ON Time	t_{CE}	3.0	—	μs
Chip Enable OFF Time	t_{CE}	0.5	—	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.



● AC TEST LOAD



- Notes) 1. $t_r = t_f = 20ns$.
- 2. C_t includes jig capacitance.
- 3. All diodes are 1S2074 Φ .

HN613256P, HN613256FP

32768-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN613256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized system.

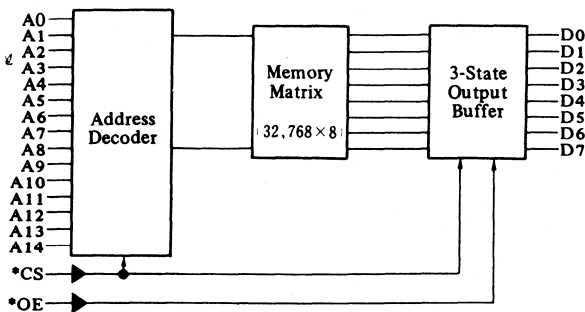
To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation.

The active level of the CS and OE input, and the memory content are defined by the user. The Chip Select input deselected the output and puts the chip in a power-down mode.

■ FEATURES

- Fully Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-state Data Output for OR-ties
- Mask Programmable Chip Select and Output Enable
- TTL Compatible
- Maximum Access Time: 250ns
- Low Power Standby and Low Power Operation; Standby $5\mu\text{W}$ (typ.), Operation 50mW (typ.)
- Pin Compatible with EPROM

■ BLOCK DIAGRAM



* Active level defined by the user.

■ ABSOLUTE MAXIMUM RATINGS

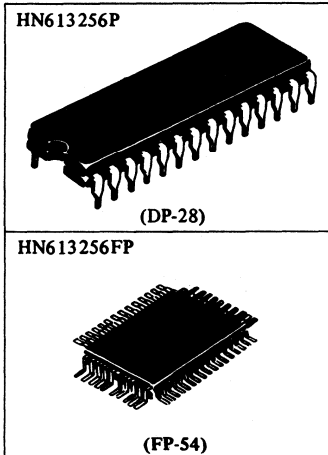
Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V_T	-0.3 to +7.0	V
Operating Temperature Range	T_{opr}	-20 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	-20 to +85	°C

*With respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

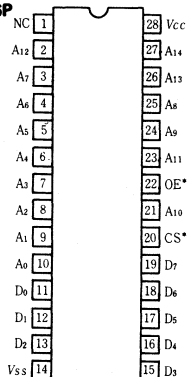
Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	-0.3	—	0.8	V
	V_{IH}	2.2	—	V_{CC}	V
Operating Temperature	T_{opr}	-20	—	75	°C

* With respect to V_{SS} .



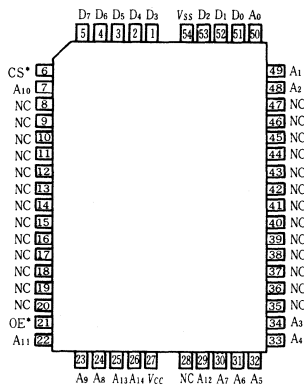
■ PIN ARRANGEMENT

● HN613256P



(Top View)

● HN613256FP



(Top View)

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5.0V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20 \sim +75^\circ C$)

Item	Symbol	Test Condition	min	typ**	max	Unit			
Input Voltage.	V_{IH}		2.2	-	V_{CC}	V			
	V_{IL}		-0.3	-	0.8	V			
Output Voltage	V_{OH}	$I_{OH} = -205 \mu A$	2.4	-	-	V			
	V_{OL}	$I_{OL} = 3.2 \text{ mA}$	-	-	0.4	V			
Input Leakage Current	I_{LI}	$V_{in} = 0 \sim 5.5V$	-	-	2.5	μA			
Output Leakage Current	I_{LOH}	$CS = 0.8V, \overline{CS} = 2.2V$	$V_{out} = 2.4V$		-	10	μA		
	I_{LOL}		$V_{out} = 0.4V$		-	10	μA		
Supply Current	Active	I_{CC}^*	$V_{CC} = 5.5V, I_{out} = 0mA, t_{RC} = \text{min}, \text{duty} = 100\%$			-	15	30	mA
	Standby	I_{SB}	$V_{CC} = 5.5V, \overline{CS} \geq V_{CC} - 0.2V, CS \leq 0.2V$			-	1	30	μA
Input Capacitance	C_{in}^{***}	$V_{in} = 0V, f = 1 \text{ MHz}, T_a = 25^\circ C$	-	-	10	pF			
Output Capacitance	C_{out}^{***}		-	-	15	pF			

* Steady state current *** This parameter is sampled and not 100% tested.
 ** $V_{CC} = 5V, T_a = 25^\circ C$

■ AC CHARACTERISTICS (READ CYCLE)

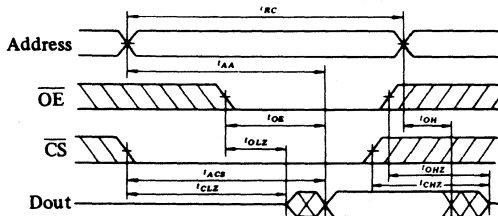
($V_{CC} = 5V \pm 10\%$, $V_{SS} = 0V$, $T_a = -20 \sim +75^\circ C$, $t_r = t_f = 20ns$)

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	250	-	ns
Address Access Time	t_{AA}	-	250	ns
Chip Select Access Time	t_{ACS}	-	250	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	-	ns
Output Enable to Output Valid	t_{OE}	-	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	-	ns
Chip Deselection to Output in High Z	t_{CHZ}	0	100	ns
Output Disable to Output in High Z	t_{OHZ}	0	100	ns
Output Hold from Address Change	t_{OH}	10	-	ns

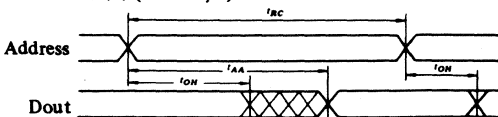
* t_{OHZ} and t_{OLZ} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

■ TIMING WAVEFORM

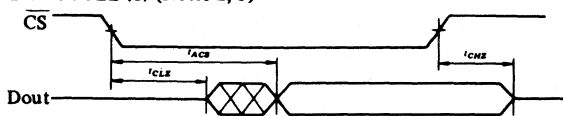
● READ CYCLE (1)



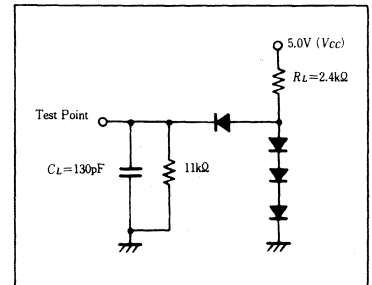
● READ CYCLE (2) (Notes 1, 3)



● READ CYCLE (3) (Notes 2, 3)



● AC TEST LOAD



Notes: 1. $t_r = t_f = 20ns$
 2. C_L includes jig capacitance
 3. All diodes are 1S2074®

NOTES:

1. Device is continuously selected.
2. Address Valid prior to or coincident with \overline{CS} transition low.
3. $\overline{OE} = V_{IL}$.
4. Input pulse level: 0.8 to 2.4V
5. Input and output reference level: 1.5V

HN623256P, HN623256FP

32678-word X 8-bit Mask Programmable Read Only Memory

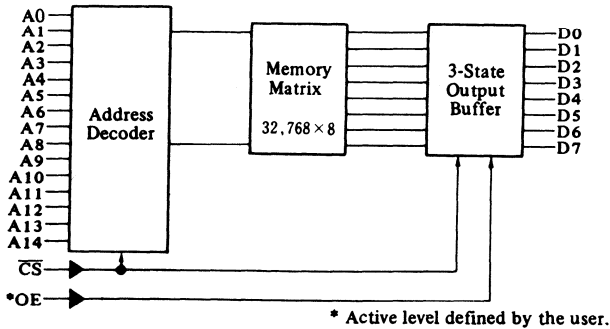
The HN623256P/FP is a mask-programmable, byte-organized memory designed for use in bus-organized systems.

The device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The active level of the OE inputs are defined by the user. The Chip Select input deselects the output and puts the chip in a power-down mode.

■ FEATURES

- Maximum Access Time 150ns
- Fully Static Operation
- Automatic Power Down
- Single+5 Volt Power Supply
- Three-State Data Output for OR-Ties
- Output Enable Mask Programmable
- TTL Compatible
- Low Power Standby and Low Power Operation; Standby: 5μW (typ)
Operation: 100mW (typ)

■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

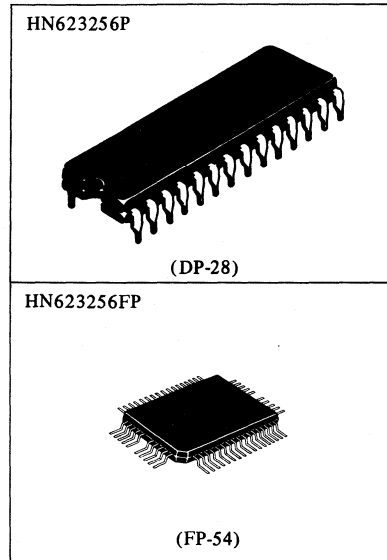
Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to 7.0	V
All Input and Output Voltage*	V_T	-0.3** to V_{CC}	V
Operating Temperature Range	T_{opr}	-20 to +75	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Bias Storage Temperature Range	T_{bias}	-20 to +85	°C

* With respect to V_{SS}

** Pulse width 50ns MAX: -1.5V (All Input)

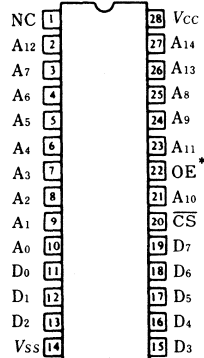
■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	-0.3	-	0.8	V
	V_{IH}	2.0	-	V_{CC}	V
Operating Temperature	T_{opr}	-20	-	75	°C



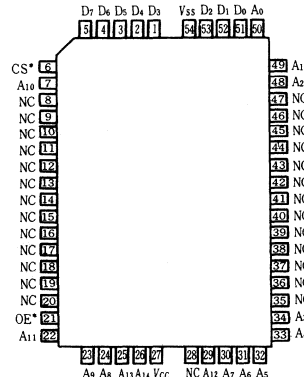
■ PIN ARRANGEMENT

● HN623256P



(Top View)

● HN623256FP



(Top View)

■ ELECTRICAL CHARACTERISTICS

($V_{CC}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a=-20$ to $+75^\circ C$ unless otherwise noted)

Item	Symbol	Test Conditions	min.	typ.	max.	Unit	
Input High-level Voltage	V_{IH}		2.0	—	V_{CC}	V	
Input Low-level Voltage	V_{IL}		-1.0**	—	0.8	V	
Output High-level Voltage	V_{OH}	$I_{OH}=-205\mu A$	2.4	—	—	V	
Output Low-level Voltage	V_{OL}	$I_{OL}=3.2mA$	—	—	0.4	V	
Input Leakage Current	$ I_{LI} $	$V_{in}=0$ to $5.5V$	—	—	2.5	μA	
Output High-level Leakage Current	I_{LOH}	$V_{out}=2.4V$, $\overline{CS}=2.0V$	—	—	10	μA	
Output Low-level Leakage Current	I_{LOL}	$V_{out}=0.4V$, $\overline{CS}=2.0V$	—	—	10	μA	
Supply Current	Active	I_{CC}^*	$V_{CC}=5.5V$, $I_{out}=0mA$, $t_{RC}=\text{min.}$	—	20 _p	45	mA
	Standby	I_{SB}	$V_{CC}=5.5V$, $\overline{CS} \geq V_{CC}-0.2V$	—	1	30	μA
Input Capacitance	C_{in}^{***}	$V_{in}=0V$, $f=1.0MHz$, $T_a=25^\circ C$	—	—	10	pF	
Output Capacitance	C_{out}^{***}	$V_{in}=0V$, $f=1.0MHz$, $T_a=25^\circ C$	—	—	15	pF	

* Specified under stable condition ** Pulse width 50ns, DC: -0.3V min.

*** This parameter is sampled and not 100% tested.

■ RECOMMENDED AC OPERATING CONDITIONS

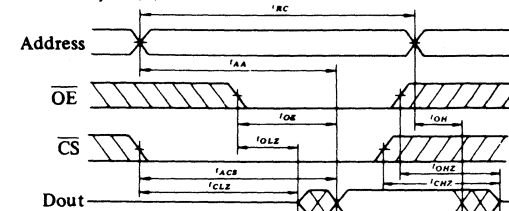
($V_{CC}=5.0V \pm 10\%$, $V_{SS}=0V$, $T_a=-20$ to $+75^\circ C$, $t_r=t_f=10ns$)

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	150	—	ns
Address Access Time	t_{AA}	—	150	ns
Chip Select Access Time	t_{ACS}	—	150	ns
Chip Selection to Output in Low Z	t_{CLZ}	10	—	ns
Output Enable to Output Valid	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Chip Deselection to Output in High Z	t_{CHZ}^*	0	100	ns
Chip Disable to Output in High Z	t_{OHZ}^*	0	100	ns
Output Hold from Address Change	t_{OH}	10	—	ns

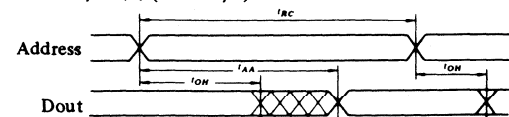
* t_{CHZ} and t_{OHZ} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

■ TIMING WAVEFORM

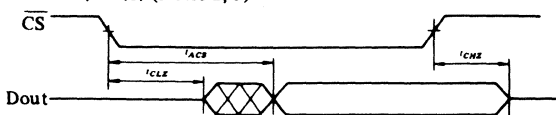
● Read Cycle (1)



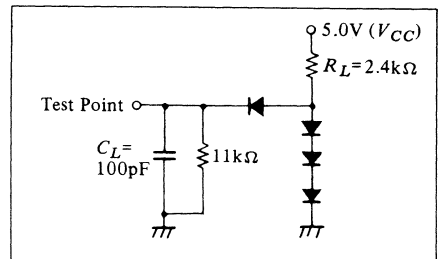
● Read Cycle (2) (Notes 1, 3)



● Read Cycle (3) (Notes 2, 3)



● AC TEST LOAD



- Notes: 1. $t_r=t_f=10ns$
- 2. C_L includes jig capacitance
- 3. All diodes are 1S2074 (F)

Notes)

1. Device is continuously selected.
2. Address Valid prior to or coincident with \overline{CS} transition low.
3. $OE=V_{IL}$.
4. V_{CC} Valid prior to Address
5. Input pulse level: 0.8 to 2.4V
6. Input and output reference level: 1.5V

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V_I	-0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range (Under Bias)	T_{bias}	-20 to +85	°C

* with respect to V_{SS}

■ ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0 \sim +70^\circ C$)

Item		Symbol	Test Condition	min	typ	max	Unit
Input Voltage		V_{IH}		2.2	-	V_{CC}	V
		V_{IL}		-0.3	-	0.8	V
Output Voltage		V_{OH}	$I_{OH} = -100 \mu A$	2.4	-	-	V
		V_{OL}	$I_{OL} = 1.6 mA$	-	-	0.4	V
Input Leakage Current		I_{LI}	$V_{IN} = 0$ to 5.5V	-	-	2.5	μA
Output Leakage Current		I_{LOH}	$CE = 2.2V$	$V_{out} = 2.4V$	-	10	μA
		I_{LOL}		$V_{out} = 0.4V$	-	10	μA
Supply Current	Active	I_{CC}	$V_{CC} = 5.5V$, $I_{out} = 0mA$, $t_{RC} = 5 \mu s$	-	-	10	mA
	Standby	I_{SB}	$V_{CC} = 5.5V$, $V_{IH} \geq V_{CC} - 0.2V$, $V_{IL} \leq 0.2V$, $CE \geq V_{CC} - 0.2V$	-	-	50	μA
Input Capacitance		C_{in}^*	$V_{in} = 0V$, $f = 1MHz$, $T_a = 25^\circ C$	-	-	10	pF
Output Capacitance		C_{out}^*		-	-	15	pF

* This parameter is sampled and not 100% tested.

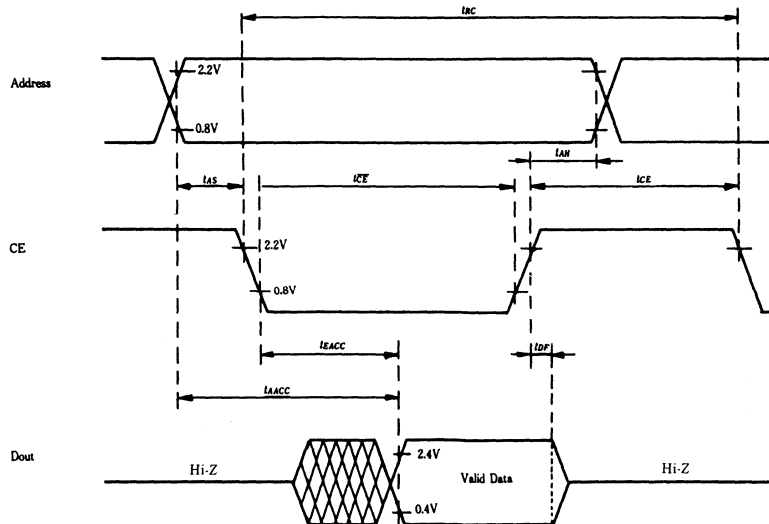
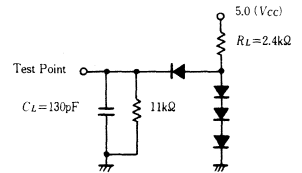
■ AC CHARACTERISTICS

Item	Symbol	min	max	Unit
Read Cycle Time	t_{RC}	5.0	-	μs
Address Access Time	t_{AAC}	-	5.0**	μs
Chip Enable Access Time	t_{EACC}	-	3.0	μs
Data Hold Time from Address	t_{DH}^*	0	0.5	μs
Address Setup Time	t_{AS}	2.0	-	μs
Address Hold Time	t_{AH}	0	-	μs
Chip Enable ON Time	t_{CE}	3.0	-	μs
Chip Enable OFF Time	t_{CE}	2.0	-	μs

* t_{DH} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

** In case of $t_{AS} = 2.0 \mu s$

● AC TEST LOAD



HN62301AP, HN62301AFP

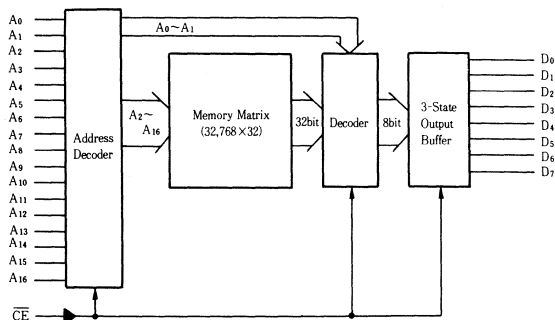
131,072-word x 8-bit Mask Programmable Read Only Memory

The HN62301AP/FP is a mask-programmable byte-organized memory designed for use in bus-organized systems. To facilitate use, the device operates from a single power supply, has compatibility with TTL, and requires no clocks or refreshing because of static operation. The Chip Enable input deselected the output and puts the chip in a power-down mode.

■ FEATURES

- Static Operation
- Automatic Power Down
- Single +5V Power Supply
- Three-State Data Output for OR-Ties
- TTL Compatible
- Maximum Access Time-250ns
- Lower Power Standby and Low Power Operation;
- Standby 2.5mW (typ.), Operation: 75mW (typ.)

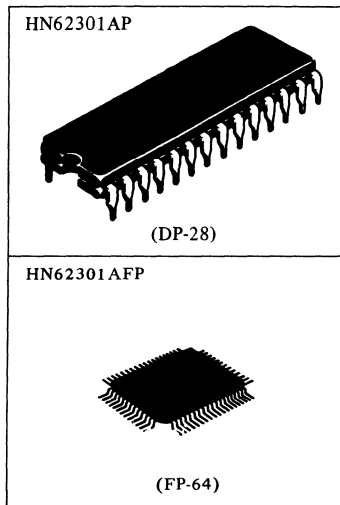
■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS

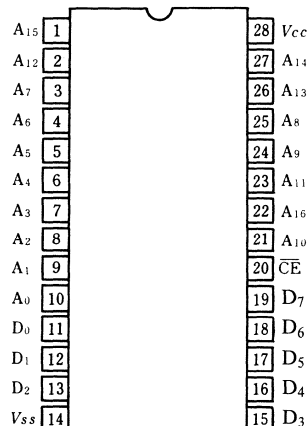
Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input and Output Voltage*	V_T	-0.3 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{sig}	-55 to +125	°C
Bias Storage Temperature Range	T_{bias}	-20 to +85	°C

* With respect to V_{SS} .



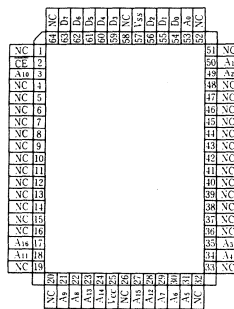
■ PIN ARRANGEMENT

● HN62301AP



(Top View)

● HN62301AFP



(Top View)

■ RECOMMENDED DC OPERATING CONDITIONS ($T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage*	V_{CC}	4.5	5.0	5.5	V
Input Voltage*	V_{IL}	-0.3	-	0.8	V
	V_{IH}	2.2	-	V_{CC}	V

* With respect to V_{SS}

■ ELECTRICAL CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Item	Symbol	Test Conditions	min.	typ.**	max.	Unit	
Normal Operating Current	I_{CC}^*	$t_{RC} = \text{min.}, V_{CC} = 5.5\text{V}, I_{out} = 0\text{ mA}$	-	15	50	mA	
Stand by Current	I_{SB}	$\overline{CE} \geq V_{CC} - 0.2\text{V}, V_{CC} = 5.5\text{V}$	-	0.5	2	mA	
Input Leakage Current	I_{LI}	$V_{in} = 0$ to 5.5V , other 0V	-10	-	10	μA	
Output Leakage Current	I_{LOH}	$\overline{CE} = 2.2\text{V}$	$V_{out} = 2.4\text{V}$	-	-	10	μA
	I_{LOL}		$V_{out} = 0.4\text{V}$	-	-	10	μA
Output Voltage	V_{OH}	$I_{out} = -205\ \mu\text{A}$	2.4	-	-	V	
	V_{OL}	$I_{out} = 3.2\text{ mA}$	-	-	0.4	V	

* Steady state current ** $V_{CC} = 5\text{V}$, $T_a = 25^\circ\text{C}$

■ CAPACITANCE ($V_{CC} = 5\text{V} \pm 10\%$, $T_a = 25^\circ\text{C}$, $f = 1\text{ MHz}$, $V_{in} = 0\text{V}$)

Item	Symbol	typ.	max.	Unit
Input Capacitance ($A_0 \sim A_{16}, \overline{CE}$)	C_{in}	-	10	pF
Output Capacitance ($D_0 \sim D_7$)	C_{out}	-	15	pF

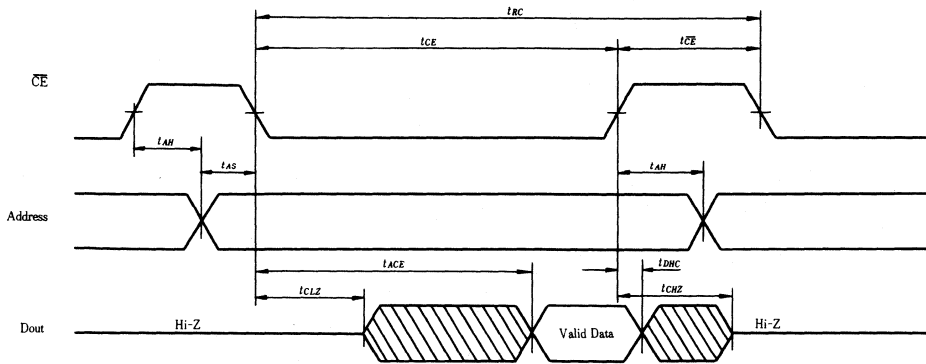
Note) These parameters are sampled and not 100% tested.

■ AC CHARACTERISTICS ($V_{CC} = 5\text{V} \pm 10\%$, $V_{SS} = 0\text{V}$, $T_a = 0$ to $+70^\circ\text{C}$, $t_r = t_f = 10\text{ns}$)

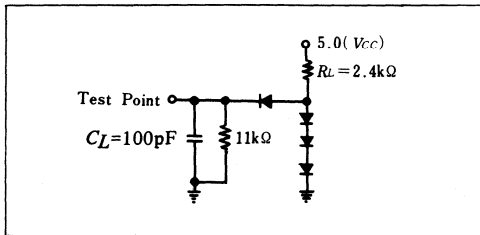
Item	Symbol	min.	max.	Unit
Cycle Time	t_{RC}	280	-	ns
\overline{CE} Access Time	t_{ACE}	-	250	ns
\overline{CE} Enable Pulse Width	t_{CE}	250	-	ns
\overline{CE} Disable Pulse Width	$t_{\overline{CE}}$	30	-	ns
Address Set up Time	t_{AS}	0	-	ns
Address Hold Time	t_{AH}	0	-	ns
Chip Disable to Output in High Z	t_{CHZ}^*	10	100	ns
Data Hold Time from \overline{CE}	t_{DHC}	0	-	ns
Chip Enable to Output in Low Z	t_{CLZ}	10	-	ns

* t_{CHZ} defines the time at which the output achieves the open circuit condition and is not reference to output voltage levels.

■ TIMING CHART



● AC TEST LOAD



- Notes)
1. $t_r = t_f = 10ns$
 2. C_L includes jig capacitance.
 3. All diodes are 1S2074 (H).
 4. Input pulse level: 0.8 to 2.4V
 5. Input and output timing reference level: 1.5V

HN62301BP HN62301BFP

Preliminary

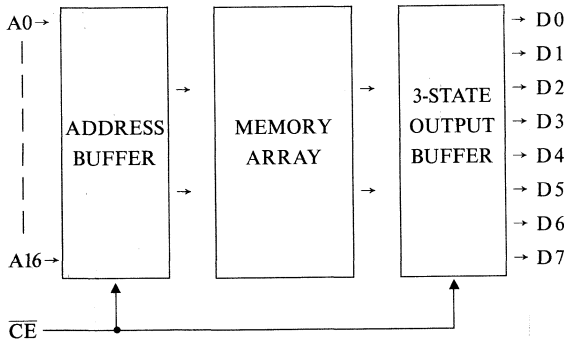
131072-word x 8-bit CMOS Mask Programmable Read Only Memory

The HN62301BP/BFP is a 1M-bit CMOS mask-programmable ROM organized as 131072 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62301BP/BFP, which provides large capacity of 1M bits, is ideally suited for kanji character generators.

■FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access time: 150ns
- Low Power Consumption: 100mW typ. active
5μW typ. standby
- Byte-Wide Data Organization

■BLOCK DIAGRAM



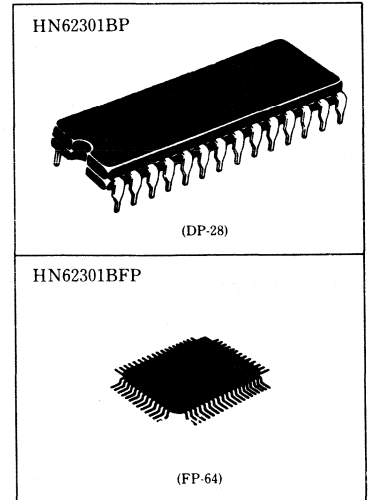
■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input or Output Voltage*	V_I	-1.5** to $V_{CC}+0.3$	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-20 to +85	°C

(Notes) * With respect to V_{SS} .

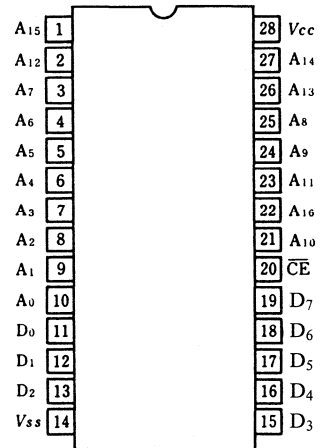
**With pulse width of 50 ns, -0.3V(min.) for DC level.

The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales, Dept., regarding specifications.



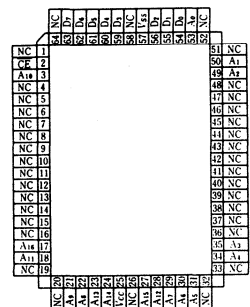
■PIN ARRANGEMENT

● HN62301BP



(Top View)

● HN62301BFP



(Top View)

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.0	—	$V_{CC} + 0.3$	V
	V_{IL}	-1.0*	—	0.8	V

* With pulse width of 50 ns: $-0.3V(\text{min.})$ for DC level.

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	Test Conditions	min.	max.	Unit	
Supply Current	Active	I_{CC}	$V_{CC}=5.5V$, $I_{OUT}=0mA$, $t_{RC}=\text{min.}$	—	50	mA
	Standby	I_{SB}	$V_{CC}=5.5V$, $\overline{CE} \geq V_{CC} - 0.2V$	—	30	μA
Input Leakage Current	$ I_{LI} $	$V_{in}=0$ to $5.5V$	—	10	μA	
Output Leakage Current	$ I_{LO} $	$\overline{CE}=2.0V$, $V_{OUT}=0$ to V_{CC}	—	10	μA	
Output Voltage	V_{OH}	$I_{OH}=-205\mu A$	2.4	—	V	
	V_{OL}	$I_{OL}=3.2mA$	—	0.4	V	

CAPACITANCE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^{\circ}C$, $V_{in}=0V$, $f=1MHz$)

Item	Symbol	min.	max.	Unit
Input Capacitance	C_{in}	—	10	pF
Output Capacitance	C_{out}	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Input Pulse Level: 0.8 to 2.4V

Input and Output Timing Reference Level: 1.5V

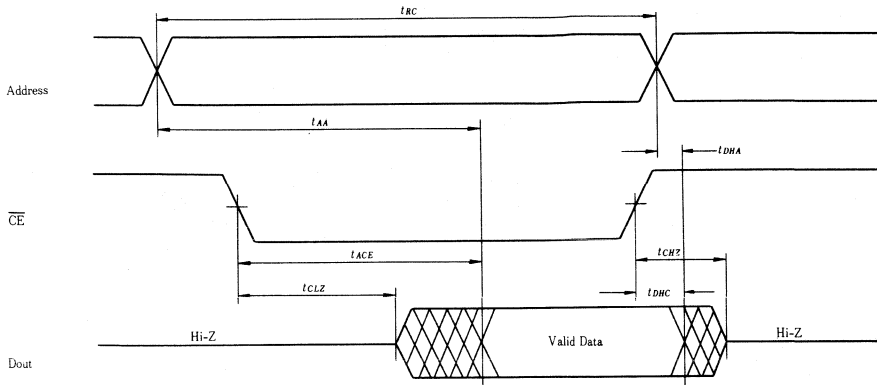
Input Rise and Fall Time: 10 ns

Output load: 1 TTL gate + $C_L = 100pF$ (including jig capacitance)

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	150	—	ns
Address Access Time	t_{AA}	—	150	ns
\overline{CE} Access Time	t_{ACE}	—	150	ns
Chip Enable to Output in Low Z	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Chip Disable to Output in High Z	t_{CHZ}^*	—	70	ns
Output Hold Time from \overline{CE}	t_{DHC}	0	—	ns

* t_{CHZ} defines the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

■ TIMING DIAGRAM



- (Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA} or t_{DHC} , whichever occurs first.
 2. The time at which the data output becomes valid is defined by t_{AA} or t_{ACE} , whichever occurs last.

HN62301DP HN62301DFP

Preliminary

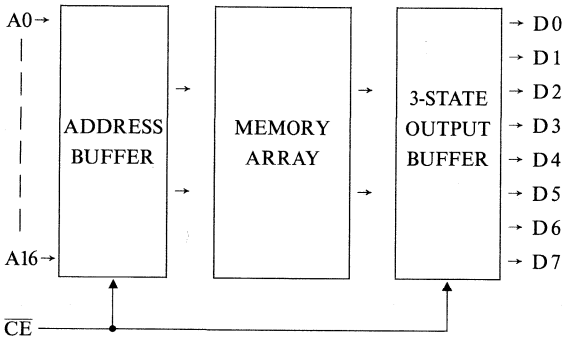
131072-word X 8-bit CMOS Mask Programmable Read Only Memory

The HN62301DP/DFP is a 1M-bit CMOS mask-programmable ROM organized as 131072 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62301DP/DFP, which provides large capacity of 1M bits, is ideally suited for kanji character generators.

■FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time: 150ns
- Low Power Consumption: 100mW typ. active
5μW typ. standby
- Byte-Wide Data Organization
- Address Valid Coincident with \overline{CE} Transition Low

■BLOCK DIAGRAM



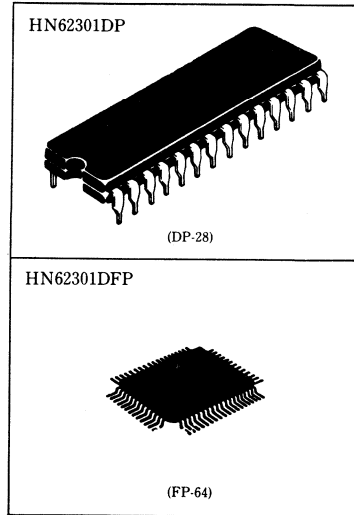
■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input or Output Voltage*	V_T	-1.5** to $V_{CC}+0.3$	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-20 to +85	°C

(Notes) * With respect to V_{SS} .

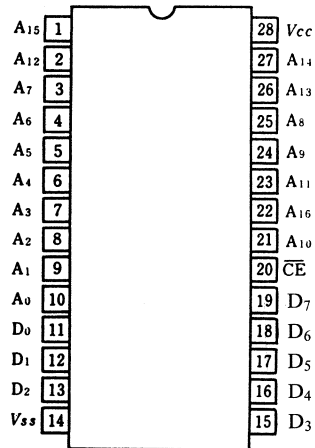
**With pulse width of 50 ns, -0.3V (min.) for DC level.

The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept., regarding specifications.



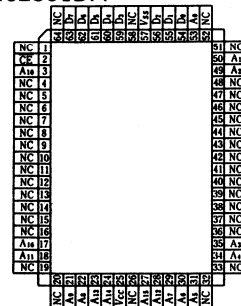
■PIN ARRANGEMENT

●HN62301DP



(Top View)

●HN62301DFP



(Top View)

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	2.0	—	$V_{CC}+0.3$	V
	V_{IH}	-1.0*	—	0.8	V

* With pulse width of 50 ns: -0.3V for DC level

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	Test Conditions	min.	max.	Unit	
Supply Current	Active	I_{CC}	$V_{CC}=5.5V$, $I_{OUT}=0mA$, $t_{RC}=\min.$	—	50	mA
	Standby	I_{SB}	$V_{CC}=5.5V$, $\overline{CE} \geq V_{CC}-0.2V$	—	30	μA
Input Leakage Current	$ I_{LI} $	$V_{in}=0$ to $5.5V$	—	10	μA	
Output Leakage Current	$ I_{LO} $	$\overline{CE}=2.0V$, $V_{OUT}=0$ to V_{CC}	—	10	μA	
Output Voltage	V_{OH}	$I_{OH}=-205\mu A$	2.4	—	V	
	V_{OL}	$I_{OL}=3.2mA$	—	0.4	V	

CAPACITANCE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^{\circ}C$, $V_{in}=0V$, $f=1MHz$)

Item	Symbol	min.	max.	Unit
Input Capacitance	C_{in}	—	10	pF
Output Capacitance	C_{out}	—	15	pF

Note) This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Input Pulse Level: 0.8 to 2.4V

Input and Output Timing Reference Level: 1.5V

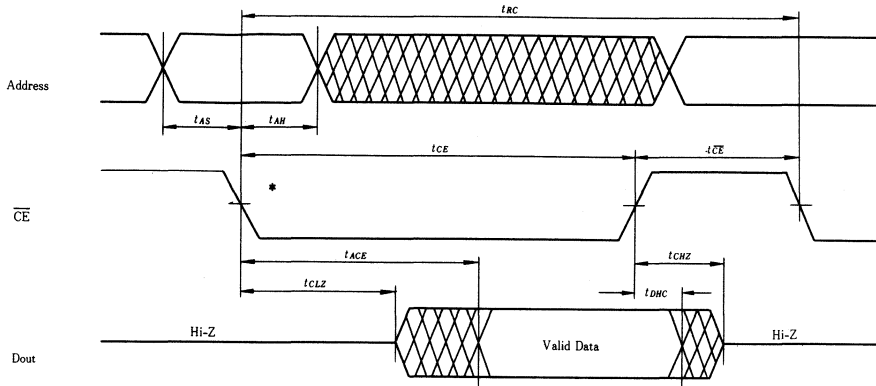
Input Rise and Fall Time: 10ns

Output Load: 1 TTL gate + $C_L = 100pF$ (including jig capacitance)

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Setup Time	t_{AS}	0	—	ns
Address Hold Time	t_{AH}	50	—	ns
\overline{CE} Access Time	t_{ACE}	—	150	ns
Chip Enable to Output in Low Z	t_{CLZ}	10	—	ns
Chip Disable to Output in High Z	t_{CHZ}^*	—	70	ns
Output Hold Time from \overline{CE}	t_{DHC}	0	—	ns
\overline{CE} Enabled Pulse Width	t_{CE}	150	—	ns
\overline{CE} Disabled Pulse Width	$t_{\overline{CE}}$	50	—	ns

* t_{CHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

■ TIMING DIAGRAM



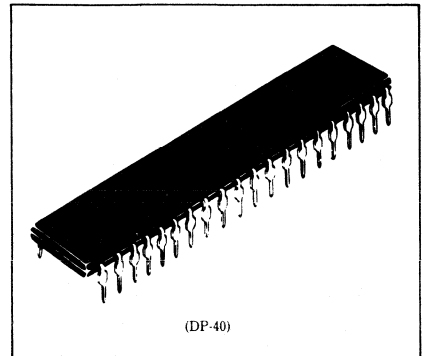
(Notes) 1. Address is latched at the \overline{CE} negative transition.

131072-word × 16-bit CMOS Mask Programmable Read Only Memory

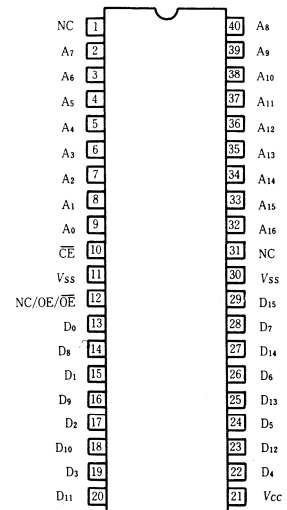
The HN62402P is a 2M bit CMOS mask-programmable ROM organized as 131072 words by 16 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62402P, which provides large capacity of 2M bits, is ideally suited for kanji character generators.

■FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time: 200ns
- Low Power Consumption: 100mW typ. active
5μW typ. standby
- Word-Wide Data Organization

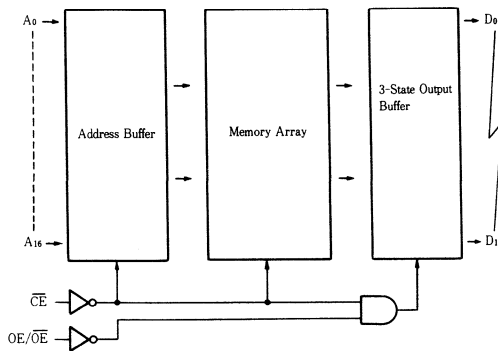


■PIN ARRANGEMENT



(Top View)

■BLOCK DIAGRAM



■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input or Output Voltage*	V_I	-0.3 to $V_{CC}+0.3$	V
Operating Temperature Range	T_{opr}	.0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-20 to +85	°C

* With respect to V_{SS} .

The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept., regarding specifications.

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2.2	—	$V_{CC}+0.3$	V
	V_{IL}	-0.3	—	0.8	V

* With pulse width of 50ns: -0.3V for DC level

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	Test Conditions	min.	max.	Unit	
Supply Current	Active	I_{CC}	$V_{CC}=5.5V$, $I_{OUT}=0mA$, $t_{RC}=\text{min.}$	—	50	mA
	Standby	I_{SB}	$V_{CC}=5.5V$, $\overline{CE} \geq V_{CC}-0.2V$	—	30	μA
Input Leakage Current	$ I_{LI} $	$V_{in}=0$ to $5.5V$	—	10	μA	
Output Leakage Current	$ I_{LO} $	$\overline{CE}=2.2V$, $V_{OUT}=0$ to V_{CC}	—	10	μA	
Output Voltage	V_{OH}	$I_{OH}=-205\mu A$	2.4	—	V	
	V_{OL}	$I_{OL}=1.6mA$	—	0.4	V	

CAPACITANCE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^{\circ}C$, $V_{in}=0V$, $f=1MHz$)

Item	Symbol	min.	max.	Unit
Input Capacitance	C_{in}	—	15	pF
Output Capacitance	C_{out}	—	15	pF

(Note) This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Input Pulse Level: 0.8 to 2.4V

Input and Output Timing Reference Level: 1.5V

Input Rise and Fall Time: 10ns

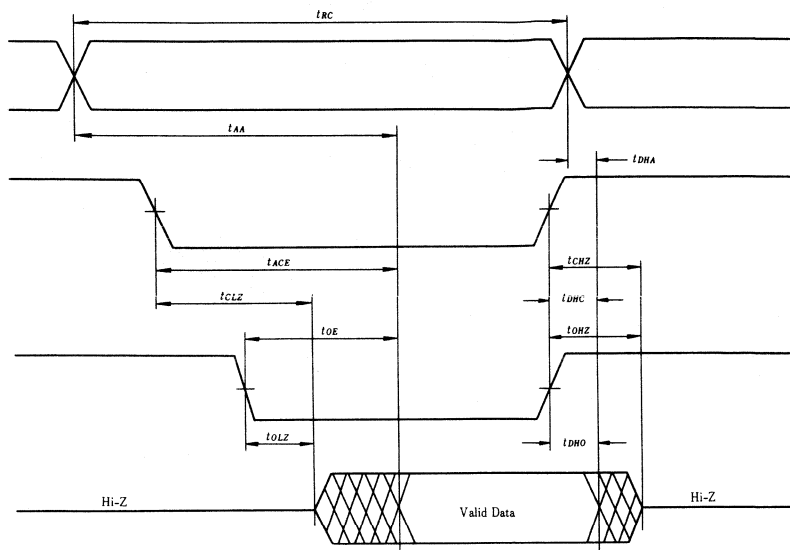
Output load: 1 TTL gate + $C_L = 100pF$ (including jig capacitance)

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	200	—	ns
Address Access Time	t_{AA}	—	200	ns
\overline{CE} Access Time	t_{ACE}	—	200	ns
Chip Enable to Output in Low Z	t_{CLZ}	10	—	ns
Output Hold Time from Address Change	t_{DHA}	0	—	ns
Chip Deselection to Output in High Z	t_{CHZ}^*	—	70	ns
Output Hold Time from \overline{CE}	t_{DHC}	0	—	ns
OE Access Time	t_{OE}	—	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	—	ns
Output Disable to Output in High Z	t_{OHZ}^*	—	70	ns
Output Hold Time from OE	t_{DHO}	0	—	ns

* t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

■ TIMING DIAGRAM



- (Notes) 1. The time at which the data output becomes invalid is defined by t_{DHA} , t_{DHC} or t_{DHO} , whichever occurs first.
2. The time at which the data output becomes valid is defined by t_{AA} , t_{ACE} or t_{OE} , whichever occurs last.
3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ} , whichever occurs last.

HN62302P

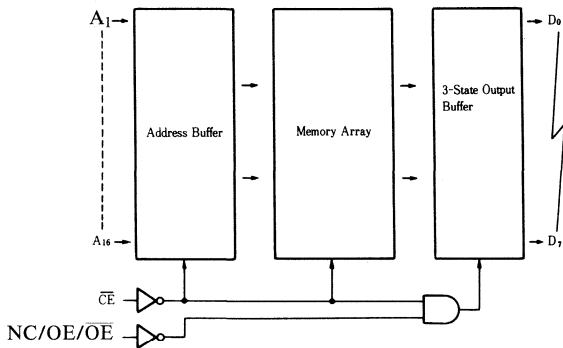
262,144 x 8 bit CMOS Mask Programmable Read Only Memory

The HN62302P is a 2M bit CMOS mask-programmable ROM organized as 262144 words by 8 bits. Realizing low power consumption, this memory is allowed for battery operation. In addition, the HN62302P, which provides large capacity of 2M bits, is ideally suited for kanji character generators.

■FEATURES

- Single +5V Power Supply
- Three-State Data Output for OR-Tieing
- TTL Compatible
- Maximum Access Time: 200ns
- Low Power Consumption: 100mW typ. active
5 μ W typ. standby
- Byte Wide Data Organization

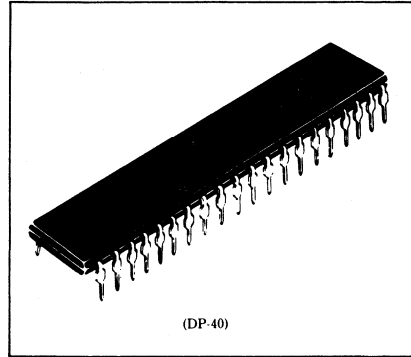
■BLOCK DIAGRAM



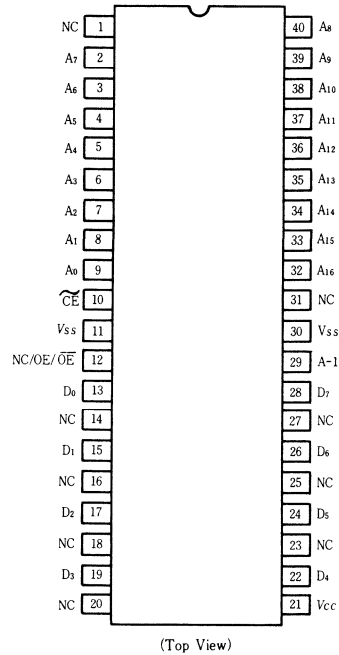
■ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.3 to +7.0	V
All Input or Output Voltage*	V_I	-0.3 to $V_{CC}+0.3$	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Temperature Under Bias	T_{bias}	-20 to +85	°C

* With respect to V_{SS} .



■PIN ARRANGEMENT



The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept., regarding specifications.

RECOMMENDED OPERATING CONDITIONS ($V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IH}	2 ?	–	$V_{CC} + 0.3$	V
	V_{IL}	-0.3	–	0.8	V

* With pulse width of 50ns: $-0.3V$ for DC level

DC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item		Symbol	Test Conditions	min.	max.	Unit
Supply Current	Active	I_{CC}	$V_{CC}=5.5V$, $I_{OUT}=0mA$, $t_{rc} = \text{min.}$	–	50	mA
	Standby	I_{SB}	$V_{CC}=5.5V$, $\overline{CE} \geq V_{CC} - 0.2V$	–	30	μA
Input Leakage Current		$ I_{LI} $	$V_{in} = 0$ to $5.5V$	–	10	μA
Output Leakage Current		$ I_{LO} $	$\overline{CE}=2.2V$, $V_{OUT}=0$ to V_{CC}	–	10	μA
Output Voltage		V_{OH}	$I_{OH} = -205\mu A$	2.4	–	V
		V_{OL}	$I_{OL} = 1.6mA$	–	0.4	V

CAPACITANCE ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=25^{\circ}C$, $V_{in} = 0V$, $f=1MHz$)

Item	Symbol	min.	max.	Unit
Input Capacitance	C_{in}	–	15	pF
Output Capacitance	C_{out}	–	15	pF

Note) This parameter is sampled and not 100% tested.

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Input Pulse Level: 0.8 to 2.4V

Input and Output Timing Reference Level: 1.5V

Input Rise and-Fall Time: 10ns

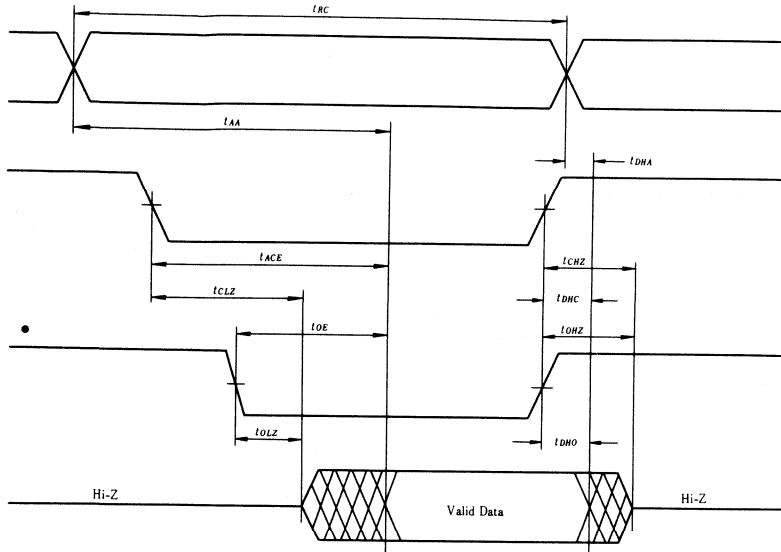
Output load: 1 TTL gate + $C_L = 100pF$ (including jig capacitance)

AC ELECTRICAL CHARACTERISTICS ($V_{CC}=5V \pm 10\%$, $V_{SS}=0V$, $T_a=0$ to $+70^{\circ}C$)

Item	Symbol	min.	max.	Unit
Read Cycle Time	t_{RC}	200	–	ns
Address Access Time	t_{AA}	–	200	ns
\overline{CE} Access Time	t_{ACE}	–	200	ns
Chip Enable to Output in Low Z	t_{CLZ}	10	–	ns
Output Hold Time from Address Change	t_{DHA}	0	–	ns
Chip Deselection to Output in High Z	t_{CHZ}^*	–	70	ns
Output Hold Time from \overline{CE}	t_{DHC}	0	–	ns
OE Access Time	t_{OE}	–	100	ns
Output Enable to Output in Low Z	t_{OLZ}	10	–	ns
Output Disable to Output in High Z	t_{OHZ}^*	–	70	ns
Output Hold Time from OE	t_{DHO}	0	–	ns

* t_{CHZ} and t_{OHZ} define the time at which the output goes to the high impedance state and is not referenced to output voltage levels.

■ TIMING DIAGRAM



- (Notes)
1. The time at which the data output becomes invalid is defined by t_{DHA} , t_{DHC} or t_{DHO} , whichever occurs first.
 2. The time at which the data output becomes valid is defined by t_{AA} , t_{ACE} or t_{OE} , whichever occurs last.
 3. The time at which the data output becomes invalid from the high impedance state is defined by t_{CLZ} or t_{OLZ} , whichever occurs last.

MOS PROM

HN482764G Series — Maintenance Only

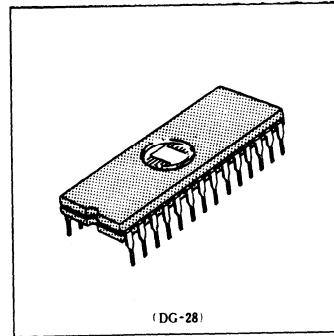
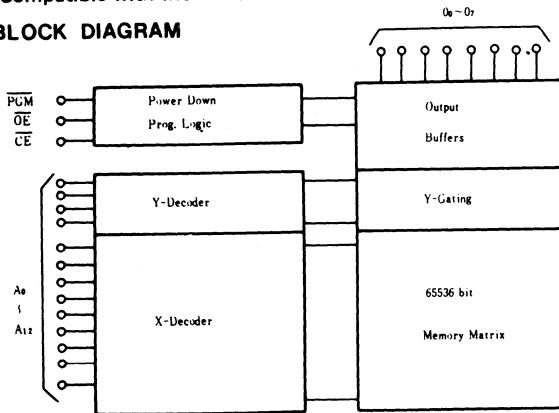
8192-word x 8-bit UV Erasable and Programmable Read Only Memory

The HN482764G is a 8192 word by 8 bit erasable and electrically programmable ROM. This device is packaged in a 28 pin dual-in-line package with transparent lid. The transparent lid on the package allows the memory content to be erased with ultraviolet light.

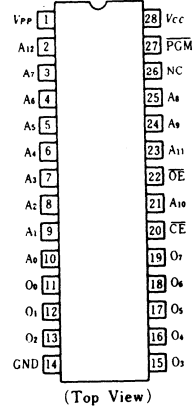
■ FEATURES

- Single Power Supply +5V ± 5%
- Simple Programming Program Voltage: +21V D.C.
Program with one 50ms Pulse
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode.
- Access Time HN482764G-2 200ns max
HN482764G 250ns max
HN482764G-3 300ns max
- High Performance Programming Available
- Low Standby Current 35mA max.
- Compatible with Intel 2764

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ MODE SELECTION

Mode	Pins	CE (20)	OE (22)	PGM (1)	V _{PP} (28)	V _{CC} (28)	Outputs (11~13, 15~19)
Read		V _{IL}	V _{IL}	V _{IN}	V _{CC}	V _{CC}	Dout
Stand-by		V _{IN}	×	×	V _{CC}	V _{CC}	High Z
Program		V _{IL}	×	V _{IL}	V _{PP}	V _{CC}	Din
Program Verify		V _{IL}	V _{IL}	V _{IN}	V _{PP}	V _{CC}	Dout
Program Inhibit		V _{IN}	×	×	V _{PP}	V _{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T _{op}	0 to +70	°C
Storage Temperature Range	T _{stg}	-65 to +125	°C
All Input and Output Voltage*	V _I	-0.6 to +7	V
V _{PP} Voltage*	V _{PP}	-0.6 to +26.5	V

* : with respect to GND

Note) This device is not available for new application.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 5\%$, $V_{PP}=V_{CC}\pm 0.6\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC}=5.25\text{V}$, $V_{iA}=-5.25\text{V}$	—	—	10	μA
Output Leakage Current	I_{LO}	$V_{CC}=5.25\text{V}$, $V_{out}=-5.25\text{V}/0.45\text{V}$	—	—	10	μA
V_{PP} Current	I_{PP1}	$V_{PP}=V_{CC}+0.6\text{V}$	—	—	15	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{\text{CE}}=V_{IH}$	—	—	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{\text{CE}}=\overline{\text{OE}}=V_{IL}$	—	40	100	mA
Input Low Voltage	V_{IL}		-0.1^*	—	0.8	V
Input High Voltage	V_{IH}		2.0	—	$V_{CC}+1^{**}$	V
Output Low Voltage	V_{OL}	$I_{OL}=2.1\text{mA}$	—	—	0.45	V
Output High Voltage	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	—	—	V

*: DC, -0.6V AC 20ns. ** : DC, $V_{CC}+1.5\text{V}$ AC 20ns.

● AC CHARACTERISTICS ($T_a=0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 5\%$, $V_{PP}=V_{CC}\pm 0.6\text{V}$)

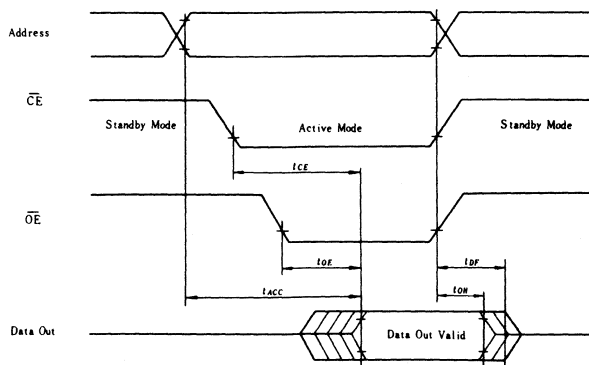
Parameter	Symbol	Test Conditions	HN482764G-2		HN482764G		HN482764G-3		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{\text{CE}}=\overline{\text{OE}}=V_{IL}$	—	200	—	250	—	300	ns
CE to Output Delay	t_{CE}	$\overline{\text{OE}}=V_{IL}$	—	200	—	250	—	300	ns
OE to Output Delay	t_{OE}	$\overline{\text{CE}}=V_{IL}$	10	80	10	100	10	150	ns
OE High to Output Float	t_{OF}	$\overline{\text{CE}}=V_{IL}$	0	60	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{\text{CE}}=\overline{\text{OE}}=V_{IL}$	0	—	0	—	0	—	ns

Note : t_{OF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Output Load: 1TTL Gate + 100pF
 Reference Level for Measuring Timing: 0.8V and 2.0V



● CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{iA} = 0\text{V}$	—	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	—	8	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC}=5\text{V} \pm 5\%$, $V_{PP}=21\text{V} \pm 0.5\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in} = 5.25\text{V}$	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		-0.1*	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC} + 1^{**}$	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}} = \text{PGM} = V_{IL}$	—	—	30	mA

*: DC, -0.6V AC 20ns. **: DC, $V_{CC} + 1.5\text{V}$ AC 20ns.

● AC PROGRAMMING CHARACTERISTICS ($T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC}=5\text{V} \pm 5\%$, $V_{PP}=21\text{V} \pm 0.5\text{V}$)

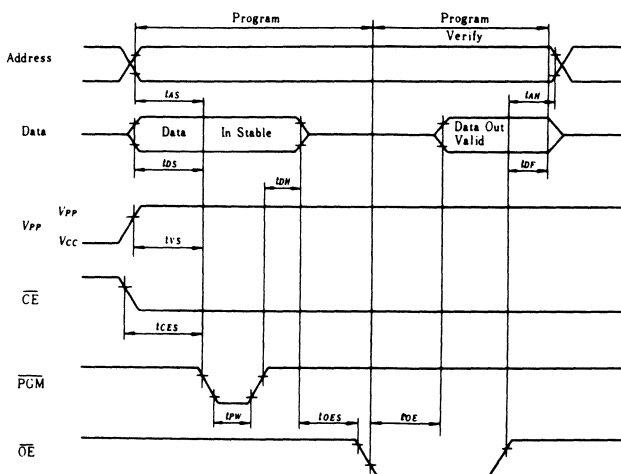
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{\text{OE}}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
PGM Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		—	—	150	ns

Note: t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ ns}$
 Reference Level for Measuring Timing: 0.8V and 2V

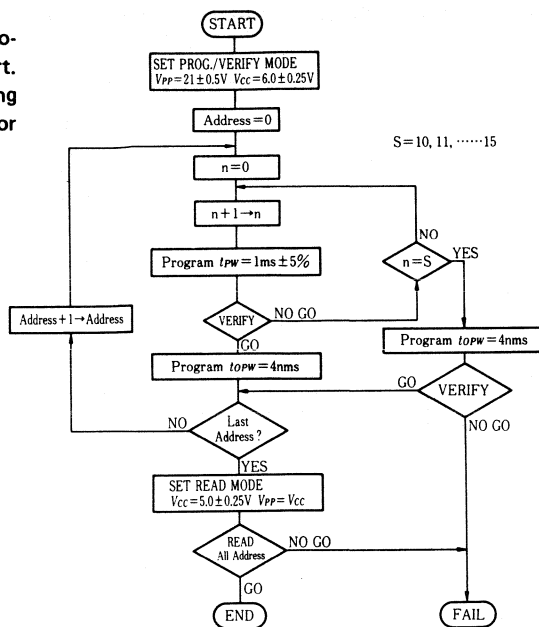


■ ERASE

Erasure of HN482764 is performed by exposure to Ultra-violet light of 2537A, and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is $15\text{W} \cdot \text{sec}/\text{cm}^2$

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=21\text{V} \pm 0.5\text{V}$)

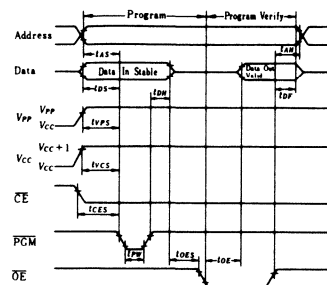
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
OE Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
OE to Output Float Delay *	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
PGM Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
CE Setup Time	t_{CES}		2	—	—	μs
Data Valid from OE	t_{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 ** t_{OPW} is defined as mentioned in flort chart.

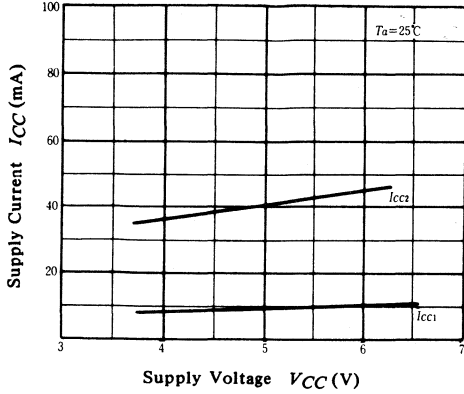
● SWITCHING CHARACTERISTICS

Test Condition

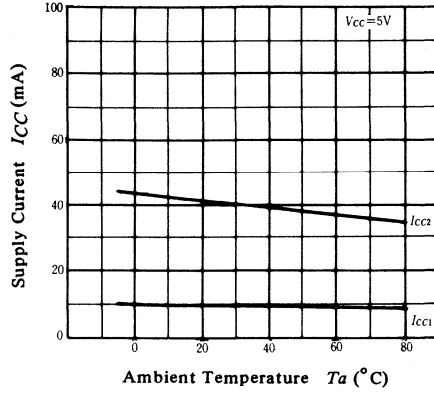
- Input Pulse Level: 0.45V to 2.4V
- Input Rise and Fall Time: ≤ 20 ns
- Reference Level for Measuring Timing: 0.8V and 2V



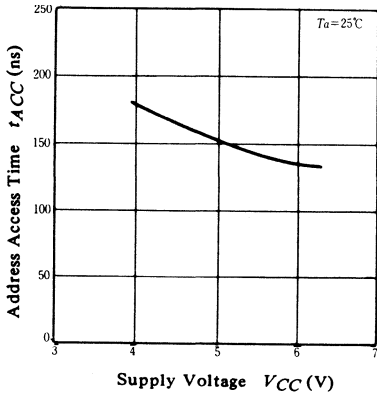
SUPPLY CURRENT VS. SUPPLY VOLTAGE



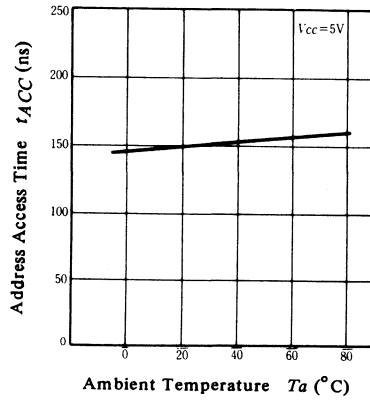
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



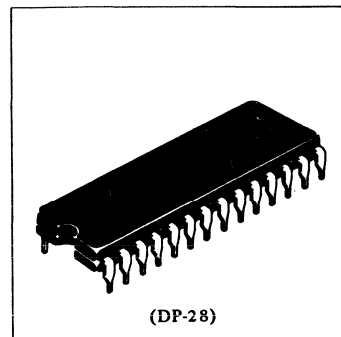
HN482764P Series — Maintenance Only

8192-word x 8-bit One Time Electrically Programmable ROM

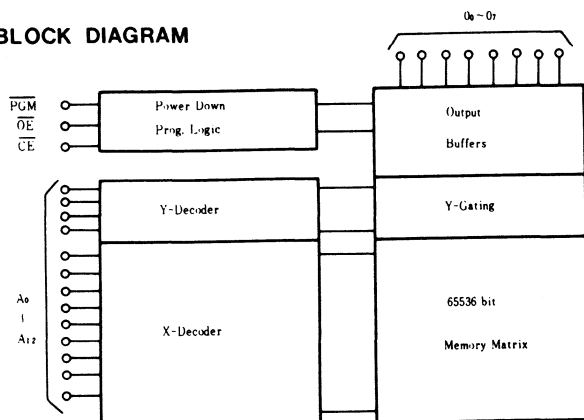
The HN482764P is a 8192 word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN482764P are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, dual-in-line plastic package. Therefore, this device can not be re-written.

■ FEATURES

- Single Power Supply +5V ±5%
- Simple Programming. Program Voltage: +21V D.C.
Program with one 50ms Pulse
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Mode
- Access Time 250/300ns max.
- Low Standby Current 35mA max.
- Compatible with Intel P2764



■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	Pins CE. (20)	OE (22)	PGM (27)	V _{PP} (1)	V _{CC} (28)	Outputs (11~13, 15~19)
Read	V _{IL}	V _{IL}	V _{IH}	V _{CC}	V _{CC}	Dout
Stand-by	V _{IH}	×	×	V _{CC}	V _{CC}	High Z
Program	V _{IL}	×	V _{IL}	V _{PP}	V _{CC}	Din
Program Verify	V _{IL}	V _{IL}	V _{IH}	V _{PP}	V _{CC}	Dout
Program Inhibit	V _{IH}	×	×	V _{PP}	V _{CC}	High Z

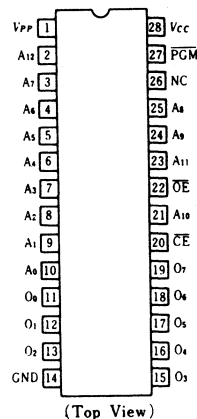
× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T _{opr}	0 to +70	°C
Storage Temperature Range	T _{sig}	-55 to +125	°C
All Input and Output Voltage*	V _T	-0.6 to +7	V
V _{PP} Voltage*	V _{PP}	-0.6 to +26.5	V

* with respect to GND

■ PIN ARRANGEMENT



Note) This device is not available for new application.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6\text{V}$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC} = 5.25\text{V}$, $V_{in} = 5.25\text{V}$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{CC} = 5.25$, $V_{out} = 5.25\text{V}/0.45\text{V}$	-	-	10	μA
V_{PP} Current	I_{PP1}	$V_{PP} = V_{CC} + 0.6\text{V}$	-	-	15	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{\text{CE}} = V_{IH}$	-	-	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{\text{CE}} = \text{OE} = V_{IL}$	-	40	100	mA
Input Low Voltage	V_{IL}		-0.1*	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1$ **	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

*: DC, -0.6V AC 20ns. **: DC, $V_{CC} + 1.5\text{V}$ AC 20ns.

● AC CHARACTERISTICS ($T_a = 5\text{V} \pm 5\%$, $V_{PP} = V_{CC} \pm 0.6\text{V}$, $T_a = 0$ to $+70^\circ\text{C}$)

Parameter	Symbol	Test Conditions	HN482764P		HN482764P-3		Unit
			min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	250	-	300	ns
$\overline{\text{CE}}$ to Output Delay	t_{CE}	$\overline{\text{OE}} = V_{IL}$	-	250	-	300	ns
$\overline{\text{OE}}$ to Output Delay	t_{OE}	$\overline{\text{CE}} = V_{IL}$	10	100	10	150	ns
$\overline{\text{OE}}$ High to Output Float*	t_{DF}	$\overline{\text{CE}} = V_{IL}$	0	90	0	130	ns
Address to Output Hold	t_{OH}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	-	0	-	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

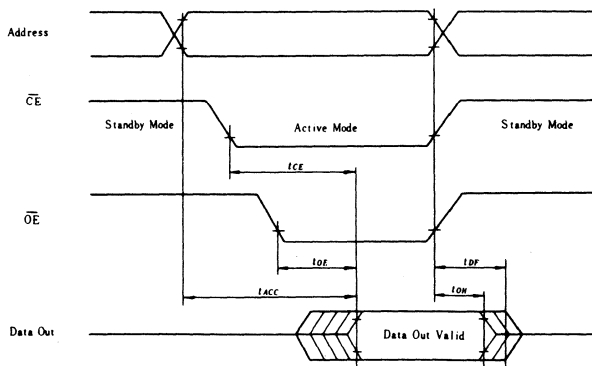
Test Condition

Input Pulse Levels: 0.45V to 2.4V

Reference Level for Measuring Timing: 0.8V and 2V

Input Rise and Fall Times: $\leq 20\text{ns}$.

Output Load: 1TTL Gate + 100pF



● CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	-	8	12	pF

■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 21\text{V} \pm 0.5\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in} = 5.25\text{V}$	—	—	10	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	—	—	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	—	—	V
V_{CC} Current (Active)	I_{CC2}		—	—	100	mA
Input Low Level	V_{IL}		-0.1*	—	0.8	V
Input High Level	V_{IH}		2.0	—	$V_{CC} + 1^{**}$	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}} = \text{PGM} = V_{IL}$	—	—	30	mA

*: DC, -0.6V AC 20ns. **: DC, $V_{CC} + 1.5\text{V}$ AC 20ns.

● AC PROGRAMMING CHARACTERISTICS ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 21\text{V} \pm 0.5\text{V}$)

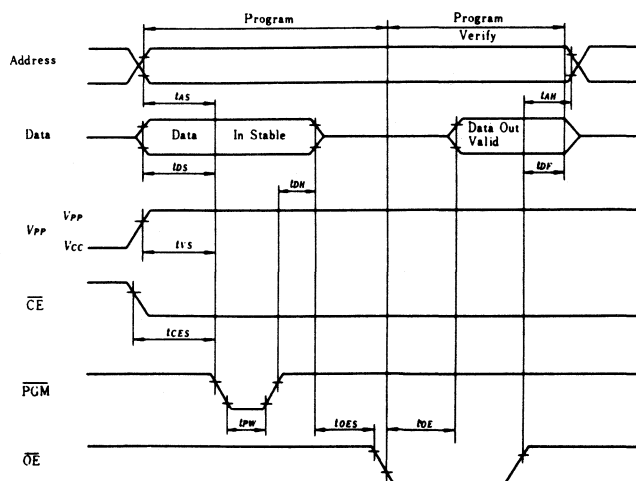
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
$\overline{\text{OE}}$ Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VS}		2	—	—	μs
PGM Pulse Width During Programming	t_{PW}		45	50	55	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	—	—	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		—	—	150	ns

Note: t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.

● SWITCHING CHARACTERISTICS

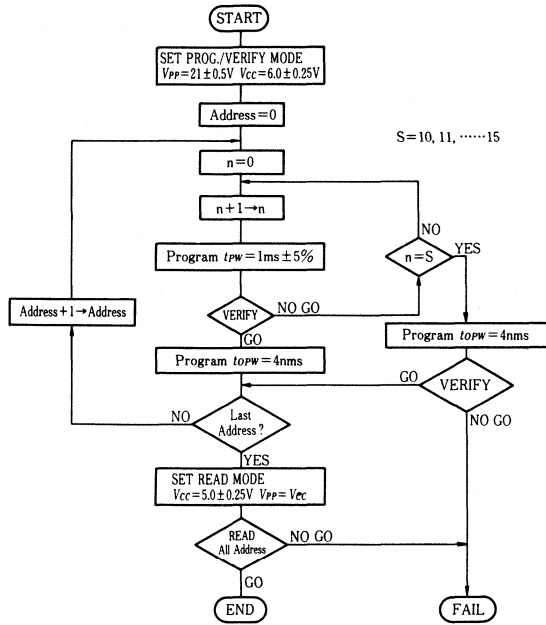
Test Condition

Input Pulse Level: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ ns}$
 Reference Level for Measuring Timing: 0.8V and 2V



■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (Ta=25°C±5°C, Vcc=6V±0.25V, Vpp=21V±0.5V)

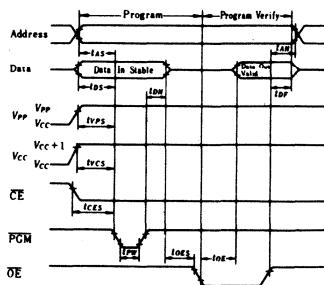
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	tAS		2	—	—	μs
OE Setup Time	tOES		2	—	—	μs
Data Setup Time	tDS		2	—	—	μs
Address Hold Time	tAH		0	—	—	μs
Data Hold Time	tDH		2	—	—	μs
OE to Output Float Delay*	tDF		0	—	130	ns
Vpp Setup Time	tVPS		2	—	—	μs
Vcc Setup Time	tVCS		2	—	—	μs
PGM Pulse Width during Initial Program	tPW		0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	tOPW		3.8	—	63	ms
CE Setup Time	tCES		2	—	—	μs
Data Valid from OE	tOE		—	—	150	ns

Notes) * tDF defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 ** tOPW is defined as mentioned in flort chart.

● SWITCHING CHARACTERISTICS

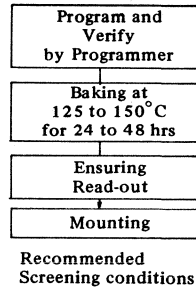
Test Condition

- Input Pulse Level: 0.45V to 2.4V
- Input Rise and Fall Time: ≤ 20 ns
- Reference Level for Measuring Timing: 0.8V and 2V

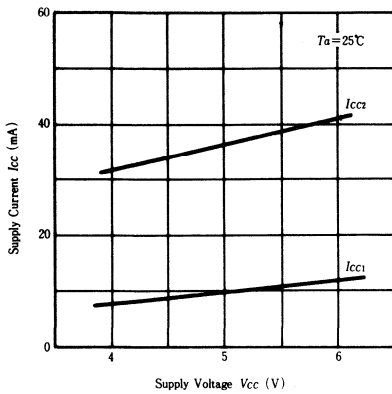


RECOMMENDED SCREENING CONDITIONS

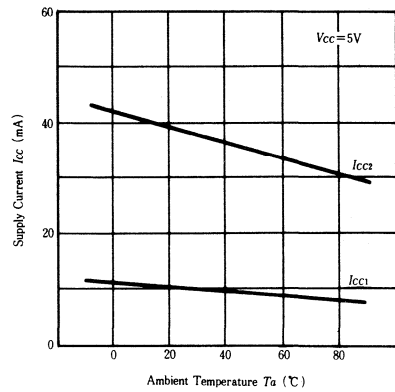
Before mounting, please make the screening (baking without bias) shown in the right.



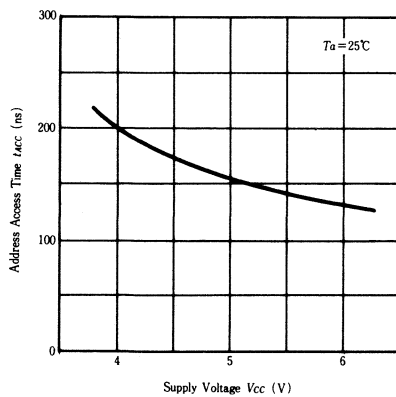
SUPPLY CURRENT VS. SUPPLY VOLTAGE



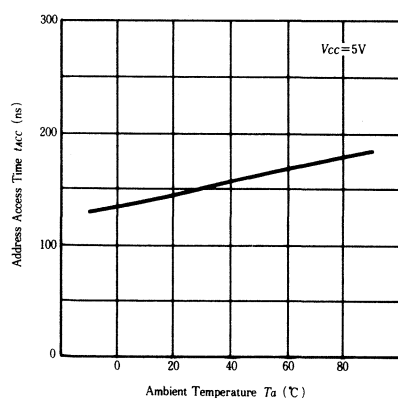
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



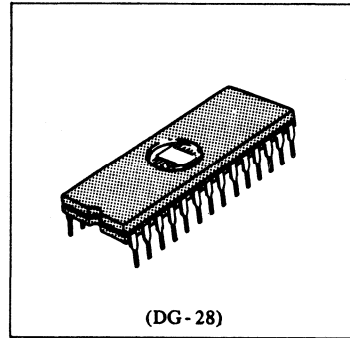
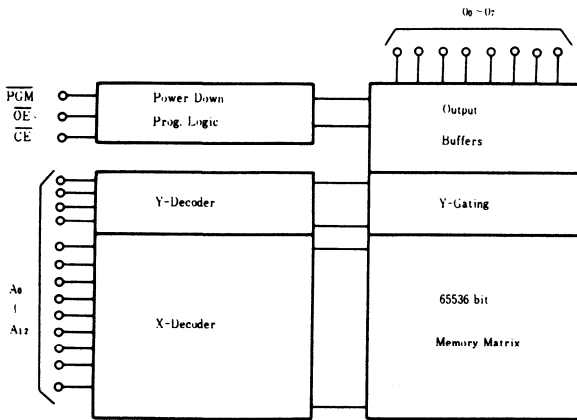
HN27C64G Series

8192-word x 8-bit U.V. Erasable and Programmable CMOS ROM

■ FEATURES

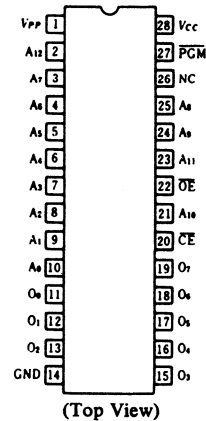
- Low Power Dissipation 20mW/MHz typ. (Active Mode)
5 μ W typ. (Stand by Mode)
- Access Time 150ns max. (HN27C64G-15)
200ns max. (HN27C64G-20)
250ns max. (HN27C64G-25)
- Single Power Supply +5V \pm 10%
- Simple Programming Program Voltage; +21V D.C.
Program with One 50ms Pulse
- Support High Performance Programming
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Fully Decoded On-chip Address Decode
- Compatible with Intel 2764

■ BLOCK DIAGRAM



(DG-28)

■ PIN ARRANGEMENT



■ MODE SELECTION

Mode	Pins	CE (20)	OE (22)	PGM (27)	V _{PP} (1)	V _{CC} (28)	Outputs (11~13, 15~19)
Read		V _{IL}	V _{IL}	V _{IN}	V _{CC}	V _{CC}	Dout
Stand-by		V _{IN}	×	×	V _{CC}	V _{CC}	High Z
Program		V _{IL}	×	V _{IL}	V _{PP}	V _{CC}	Din
Program Verify		V _{IL}	V _{IL}	V _{IN}	V _{PP}	V _{CC}	Dout
Program Inhibit		V _{IN}	×	×	V _{PP}	V _{CC}	High Z

× : don't care

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*	V_T	-1.0** ~ +7.0	V
V_{CC} Voltage*	V_{CC}	-0.6 ~ +7.0	V
V_{PP} Voltage*	V_{PP}	-0.6 ~ +25	V
Operating Temperature Range	T_{opr}	0 ~ +70	°C
Storage Temperature Range	T_{stg}	-65 ~ +125	°C

* With respect to GND

**Pulse Width: 50ns, DC: -0.6V

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a=0\sim+70^\circ\text{C}$, $V_{CC}=6\text{V}\pm 0.25\text{V}$, $V_{PP}=V_{CC}\pm 0.6\text{V}$)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC}=5.5\text{V}$, $V_{in}=\text{GND to } V_{CC}$	-	-	2	μA
Output Leakage Current	I_{LO}	$V_{CC}=5.5\text{V}$, $V_{out}=\text{GND to } V_{CC}$	-	-	2	μA
V_{PP} Current	I_{PP1}	$V_{PP}=V_{CC}+0.6\text{V}$	-	1	100	μA
V_{CC} Current (Stand-by)	I_{SB1}	$\overline{\text{CE}}=V_{IH}$	-	-	1	mA
	I_{SB2}	$\overline{\text{CE}}=V_{CC}\pm 0.3\text{V}$	-	1	100	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{\text{CE}}=V_{IL}$, $I_{out}=0\text{ mA}$	-	-	30	mA
	I_{CC2}	$f=5\text{MHz}$, $I_{out}=0\text{ mA}$	-	-	30	mA
Input Voltage	V_{IL}		-1.0*	-	0.8	V
	V_{IH}		2.2	-	** $V_{CC}+1.5$	V
Output Voltage	V_{OL}	$I_{OL}=2.1\text{ mA}$	-	-	0.45	V
	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	-	-	V

* Pulse Width: 50ns, DC: V_{IL} min = -0.3V** Pulse Width $\leq 20\text{ns}$, DC V_{IH} max = $V_{CC} + 1.0\text{V}$. Mode selection is unfixed between $V_{IH}=V_{CC}+1\text{V}$ and 11.5 V

● AC CHARACTERISTICS ($T_a=0\sim+70^\circ\text{C}$, $V_{CC}=5\text{V}\pm 10\%$, $V_{PP}=V_{CC}\pm 0.6\text{V}$)

Parameter	Symbol	Test Condition	HN27C64G-15		HN27C64G-20		HN27C64G-25		Unit
			min	max	min	max	min	max	
Address to Output Delay	t_{ACC}	$\overline{\text{CE}}=\overline{\text{OE}}=V_{IL}$, $\text{PGM}=V_{IH}$	-	150	-	200	-	250	ns
$\overline{\text{CE}}$ to Output Delay	t_{CE}	$\overline{\text{OE}}=V_{IL}$, $\text{PGM}=V_{IH}$	-	150	-	200	-	250	ns
$\overline{\text{OE}}$ to Output Delay	t_{OE}	$\overline{\text{CE}}=V_{IL}$, $\text{PGM}=V_{IH}$	10	60	10	70	10	100	ns
$\overline{\text{OE}}$ High to Output Float	t_{DF}	$\overline{\text{CE}}=V_{IL}$, $\text{PGM}=V_{IH}$	0	50	0	60	0	90	ns
Address to Output Hold	t_{OH}	$\overline{\text{CE}}=\overline{\text{OE}}=V_{IL}$, $\text{PGM}=V_{IH}$	0	-	0	-	0	-	ns

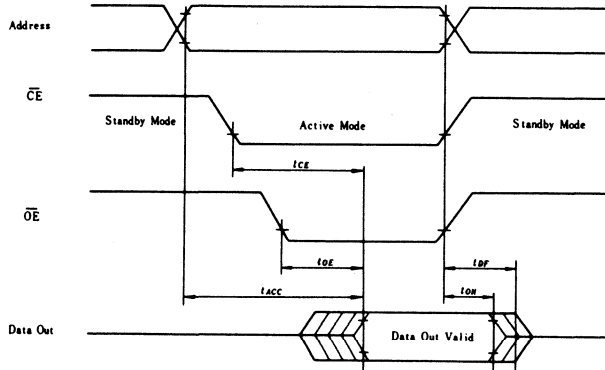
● CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in}=0\text{V}$	-	4	6	pF
Output Capacitance	C_{out}	$V_{out}=0\text{V}$	-	8	12	pF

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	≤20ns
Output Load:	1TTL + 100pF
Reference Level for Measuring Timing:	0.8V and 2V



■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 21\text{V} \pm 0.5\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25\text{V}/0.45\text{V}$	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1\text{ mA}$	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		-0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	$V_{CC} + 1.0$	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}} = \text{PGM} = V_{IL}$	–	–	30	mA

Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .

2. V_{PP} must not exceed 25V including overshoot.

3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 21\text{V}$.

4. Do not alter V_{PP} either V_{IL} to 21V or 21V to V_{IL} when $\overline{\text{CE}} = \text{PGM} = \text{Low}$.

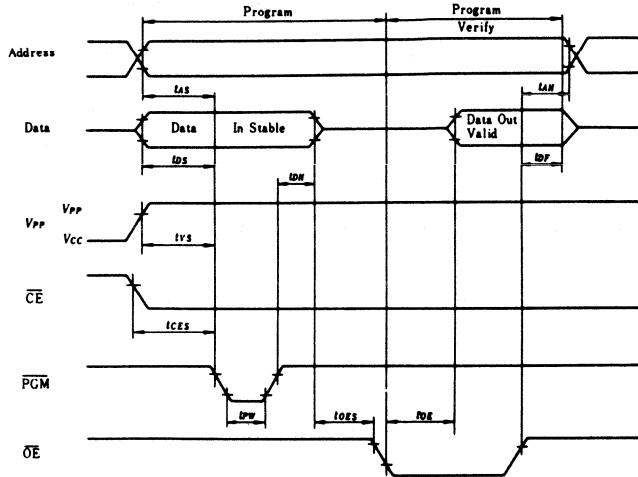
● AC PROGRAMMING CHARACTERISTICS ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{V} \pm 0.25\text{V}$, $V_{PP} = 21\text{V} \pm 0.5\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	–	–	μs
OE Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
OE to Output Float Delay	t_{DF}		0	–	130	ns
V_{PP} Setup Time	t_{VS}		2	–	–	μs
PGM Pulse Width During Programming	t_{PW}		25	50	55	ms
CE Setup Time	t_{CES}		2	–	–	μs
Data Valid from OE	t_{OE}		–	–	150	ns

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level:	0.45V to 2.4V
Input Rise and Fall Time:	≤20ns
Reference Level for Measuring Timing:	0.8V and 2V

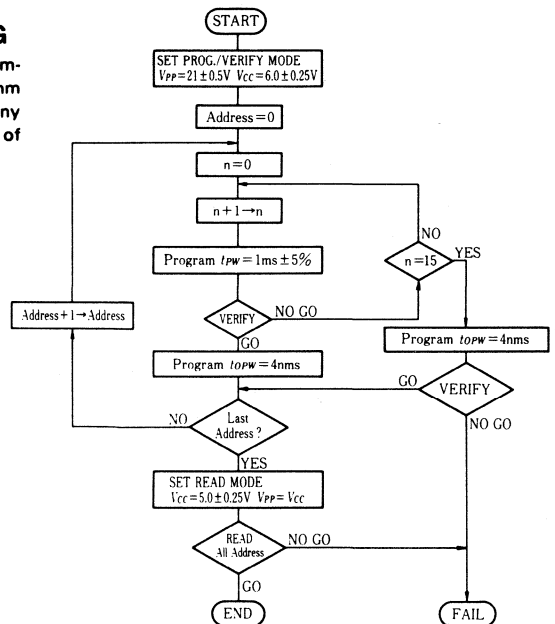


■ ERASE

Erase of HN27C64 is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W-sec/cm².

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C}\pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V}\pm 0.25\text{V}$, $V_{PP}=21\text{V}\pm 0.5\text{V}$)

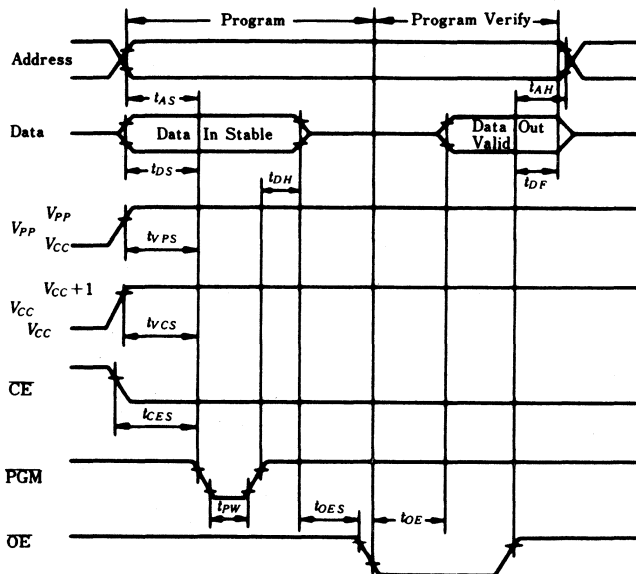
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		2	—	—	μs
OE Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Address Hold Time	t_{AH}		0	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
OE to Output Float Delay*	t_{DF}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
PGM Pulse Width during Initial Program	t_{PW}		0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	t_{OPW}		3.8	—	63	ms
CE Setup Time	t_{CES}		2	—	—	μs
Data Valid from OE	t_{OV}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 ** t_{OPW} is defined as mentioned in float chart.

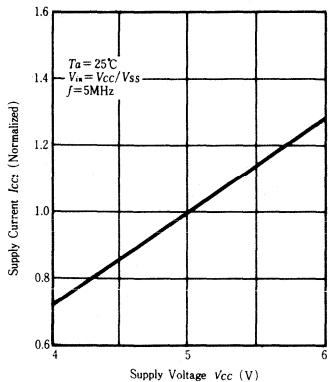
● SWITCHING CHARACTERISTICS

Test Condition

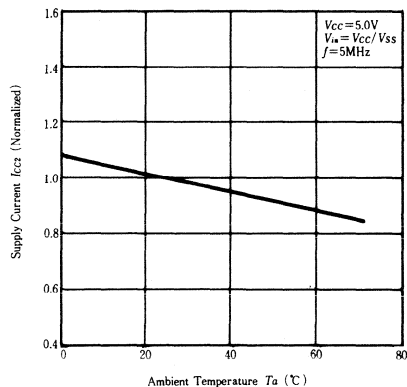
Input Pulse Level: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Reference Level for Measuring Timing: 0.8V and 2V



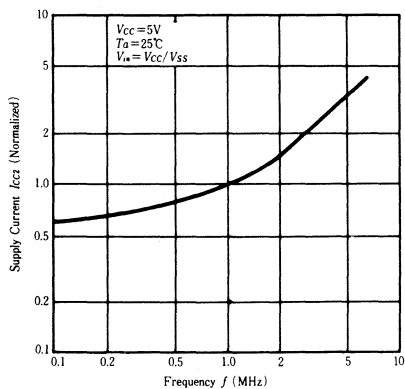
SUPPLY CURRENT VS. SUPPLY VOLTAGE



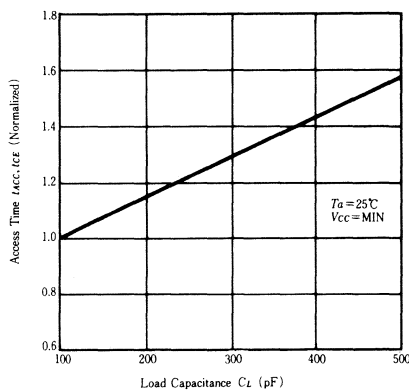
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



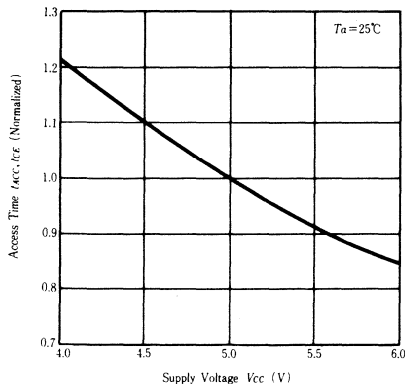
SUPPLY CURRENT VS. FREQUENCY



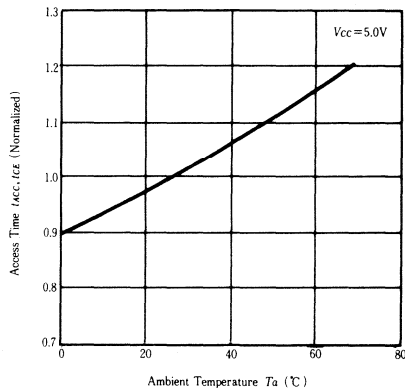
ACCESS TIME VS. LOAD CAPACITANCE



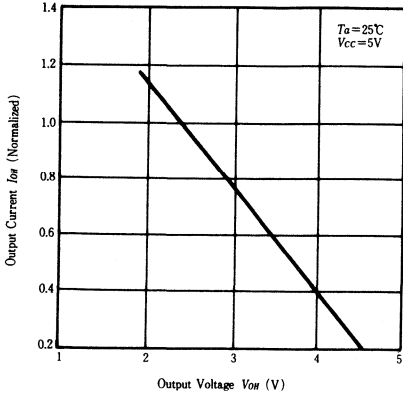
ACCESS TIME VS. SUPPLY VOLTAGE



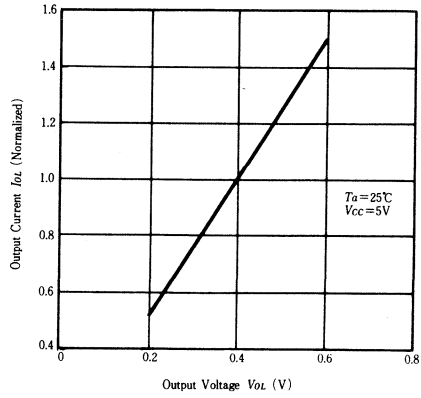
ACCESS TIME VS. AMBIENT TEMPERATURE



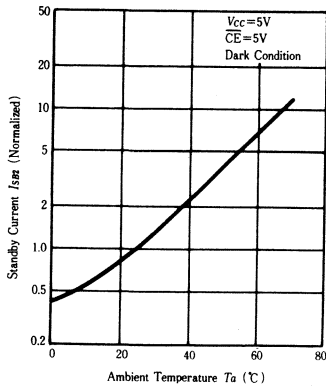
OUTPUT CURRENT VS. OUTPUT VOLTAGE



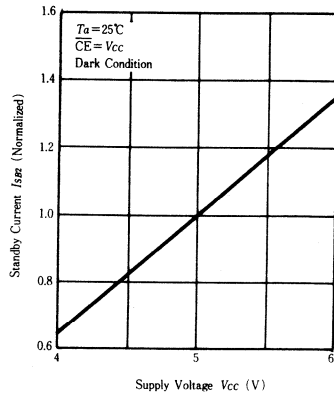
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



STANDBY CURRENT VS. SUPPLY VOLTAGE



HN27C64FP Series

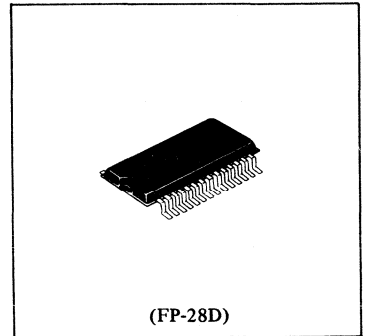
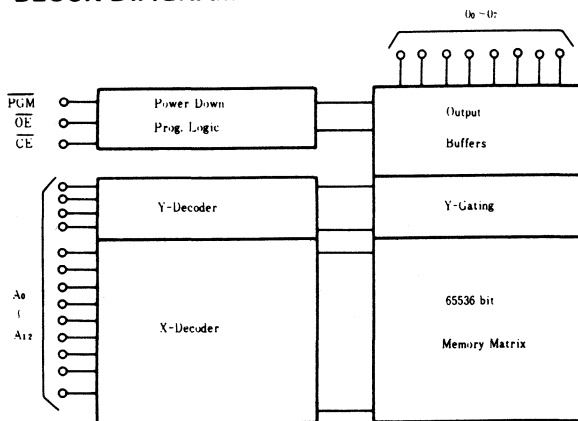
8192-word x 8-bit One Time Electrically Programmable CMOS ROM

The HN27C64FP is a 8192-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27C64FP are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic flat package (SOP). Therefore, this device can not be re-written.

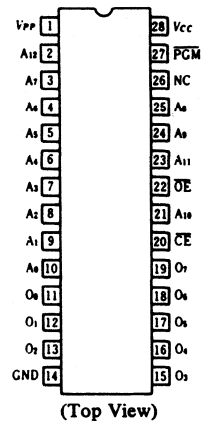
■ FEATURES

- **Low Power Dissipation** 20mW/MHz typ. (Active Mode)
5μW typ. (Stand by Mode)
- **Access Time** 200ns max. (HN27C64FP-20)
250ns max. (HN27C64FP-25)
- **Single Power Supply** +5V± 5 %
- **Simple Programming** Program Voltage; +21V D.C.
- **Support High Performance Programming**
- **Static** No Clocks Required
- **Inputs and Outputs TTL Compatible During Both Read and Program Modes**
- **Fully Decoded On-chip Address Decode**

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



MODE SELECTION

Mode	Pins CE (20)	OE (22)	PGM (27)	V _{PP} (1)	V _{CC} (28)	Outputs (11~13, 15~19)
Read	V _{IL}	V _{IL}	V _{IH}	V _{CC}	V _{CC}	Dout
Stand-by	V _{IH}	X	X	V _{CC}	V _{CC}	High Z
Program	V _{IL}	X	V _{IL}	V _{PP}	V _{CC}	Din
Program Verify	V _{IL}	V _{IL}	V _{IH}	V _{PP}	V _{CC}	Dout
Program Inhibit	V _{IH}	X	X	V _{PP}	V _{CC}	High Z

X : don't care

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltage*	V _T	-1.0**~+7.0	V
V _{CC} Voltage*	V _{CC}	-0.6~+7.0	V
V _{PP} Voltage*	V _{PP}	-0.6~+25	V
Operating Temperature Range	T _{OPR}	0~+70	°C
Storage Temperature Range	T _{stg}	-55~+125	°C

* With respect to GND

**Pulse Width: 50ns, DC: -0.6V

READ OPERATION

DC AND OPERATING CHARACTERISTICS (T_a = 0~+70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Conditions	min	typ	max	Unit
Input Leakage Current	I _{LI}	V _{CC} =5.25V, V _{in} =GND to V _{CC}	-	-	2	μA
Output Leakage Current	I _{LO}	V _{CC} =5.25V, V _{out} =GND to V _{CC}	-	-	2	μA
V _{PP} Current	I _{PP1}	V _{PP} =V _{CC} +0.6V	-	1	100	μA
V _{CC} Current (Stand-by)	I _{SB1}	CE=V _{IH}	-	-	1	mA
	I _{SB2}	CE=V _{CC} ±0.3V	-	1	100	μA
V _{CC} Current (Active)	I _{CC1}	CE=V _{IL} , I _{out} =0 mA	-	-	30	mA
	I _{CC2}	f=5MHz, I _{out} =0 mA	-	-	30	mA
Input Voltage	V _{IL}		-1.0*	-	0.8	V
	V _{IH}		2.2	-	V _{CC} +1.5**	V
Output Voltage	V _{OL}	I _{OL} =2.1 mA	-	-	0.45	V
	V _{OH}	I _{OH} =-400μA	2.4	-	-	V

* Pulse Width: 50ns, DC: V_{IL} min = -0.3V

** Pulse Width ≤ 20ns, DC V_{IH} max = V_{CC} + 1.0V

AC CHARACTERISTICS (T_a = 0~+70°C, V_{CC} = 5V ± 5%, V_{PP} = V_{CC} ± 0.6V)

Parameter	Symbol	Test Condition	HN27C64FP-20		HN27C64FP-25		Unit
			min	max	min	max	
Address to Output Delay	t _{ACC}	CE=OE=V _{IL} , PGM=V _{IH}	-	200	-	250	ns
CE to Output Delay	t _{CE}	OE=V _{IL} , PGM=V _{IH}	-	200	-	250	ns
OE to Output Delay	t _{OE}	CE=V _{IL} , PGM=V _{IH}	10	70	10	100	ns
OE High to Output Float	t _{DF}	CE=V _{IL} , PGM=V _{IH}	0	60	0	90	ns
Address to Output Hold	t _{OH}	CE=OE=V _{IL} , PGM=V _{IH}	0	-	0	-	ns

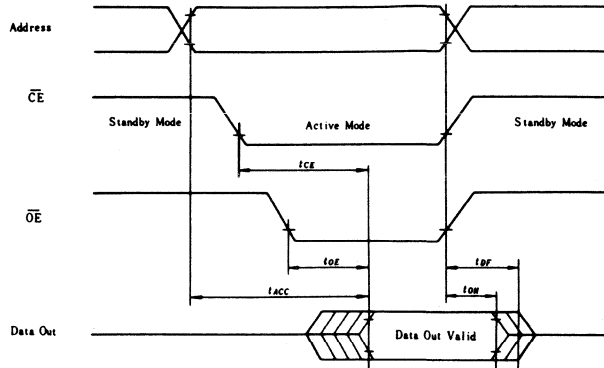
CAPACITANCE (T_a = 25°C, f = 1MHz)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C _{in}	V _{in} = 0V	-	4	6	pF
Output Capacitance	C _{out}	V _{out} = 0V	-	8	12	pF

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Output Load: 1TTL + 100pF
 Reference Level for Measuring Timing: 0.8V and 2V



■ PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = 21\text{V} \pm 0.5\text{V}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 6.25\text{V}/0.45\text{V}$	-	-	2	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V
V_{CC} Current (Active)	I_{CC}		-	-	30	mA
Input Low Level	V_{IL}		-0.1	-	0.8	V
Input High Level	V_{IH}		2.2	-	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}} = \text{PGM} = V_{IL}$	-	-	30	mA

Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .

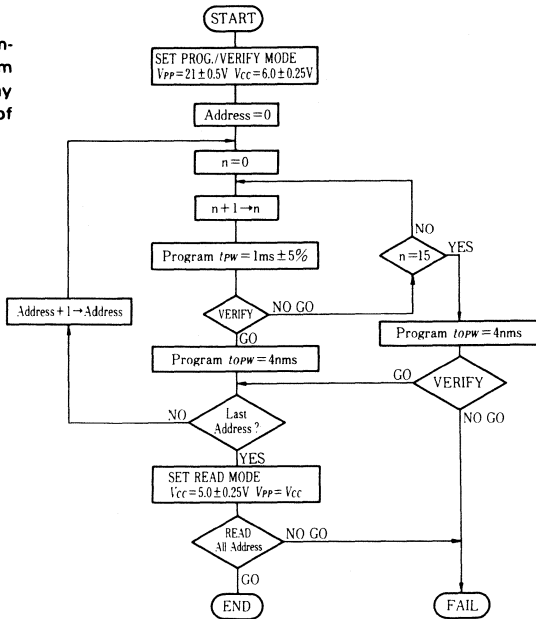
2. V_{PP} must not exceed 25V including overshoot.

3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 21\text{V}$.

4. Do not alter V_{PP} either V_{IL} to 21V or 21V to V_{IL} when $\overline{\text{CE}} = \text{PGM} = \text{Low}$.

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● AC PROGRAMMING CHARACTERISTICS (T_a=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=21V±0.5V)

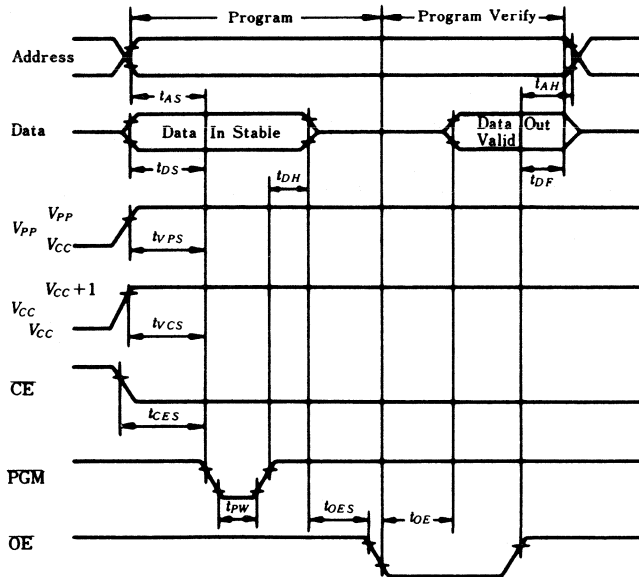
Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t _{AS}		2	—	—	μs
OE Setup Time	t _{OS}		2	—	—	μs
Data Setup Time	t _{DS}		2	—	—	μs
Address Hold Time	t _{AH}		0	—	—	μs
Data Hold Time	t _{DH}		2	—	—	μs
OE to Output Float Delay*	t _{DF}		0	—	130	ns
V _{PP} Setup Time	t _{VPS}		2	—	—	μs
V _{CC} Setup Time	t _{VCS}		2	—	—	μs
PGM Pulse Width during Initial Program	t _{PW}		0.95	1.0	1.05	ms
PGM Pulse Width during Over Program**	t _{OPW}		3.8	—	63	ms
CE Setup Time	t _{CS}		2	—	—	μs
Data Valid from OE	t _{OE}		—	—	150	ns

Notes) * t_{DF} defines the time at which the output achieves the open circuit condition and is not referenced to output voltage levels.
 ** t_{OPW} is defined as mentioned in flow chart.

● **SWITCHING CHARACTERISTICS**

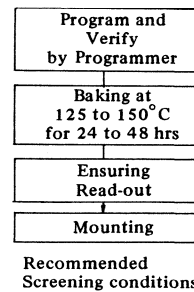
Test Condition

Input Pulse Level:	0.45V to 2.4V
Input Rise and Fall Time:	≤20ns
Reference Level for Measuring Timing:	0.8V and 2V



■ **RECOMMENDED SCREENING CONDITIONS**

Before mounting, please make the screening (baking without bias) shown in the right.



HN27128AG Series

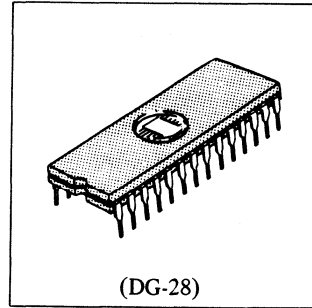
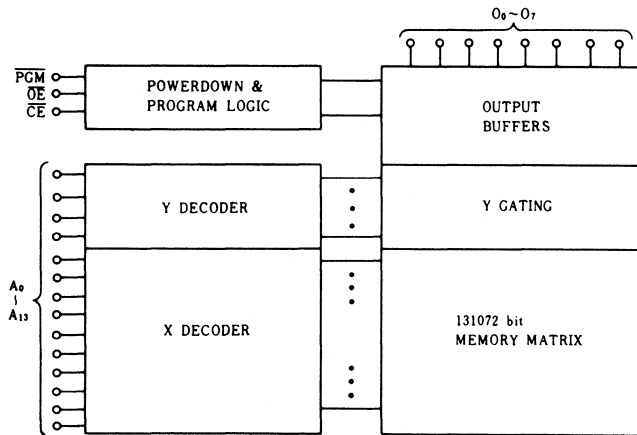
16384-word × 8-bit UV Erasable and Programmable Read Only Memory

The HN27128AG is a 16384-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin, dual-in-line package with transparent window. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

■ FEATURES

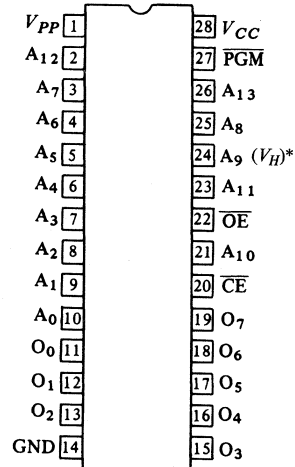
- Single Power Supply +5V ±5%
- High Performance Program Voltage: +12.5V D.C.
High Performance Programming Operations
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time HN27128AG-17: 170ns (max.)
HN27128AG-20: 200ns (max.)
HN27128AG-25: 250ns (max.)
HN27128AG-30: 300ns (max.)
- Absolute Max. Rating of 14.0V Max.
V_{pp} pin
- Low Stand-by Current 35mA Max. (stand-by)
- Device Identifier Mode Manufacturer Code and Device Code
- Compatible with INTEL 27128A

■ BLOCK DIAGRAM



(DG-28)

■ PIN ARRANGEMENT



(Top View)

*V_H = 12.0V ± 0.5V

■ MODE SELECTION

MODE	Pins	\overline{CE} (20)	\overline{OE} (22)	\overline{PGM} (27)	V_{PP} (1)	V_{CC} (28)	A9 (24)	Outputs (11~13, 15~19)
Read		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	×	Dout
Output Disable		V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	×	High Z
Stand by		V_{IH}	×	×	V_{CC}	V_{CC}	×	High Z
High Performance Program		V_{IL}	×	V_{IL}	V_{PP}	V_{CC}	×	Din
Program Verify		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	×	Dout
Program Inhibit		V_{IH}	×	×	V_{PP}	V_{CC}	×	High Z
Identifier		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_H^*	Code

Note) X . . . Don't care

* $V_H = 12.0V \pm 0.5V$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	°C
Voltage on Pin 24 (A9)	V_{ID}	-0.6 to +13.5	V
All Input and Output Voltages*	V_{IN}, V_{out}	-0.6 to +7	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to 70°C , $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25V$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25V/0.45V$	-	-	10	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.25V$	-	-	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}$	-	-	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE} = \overline{OE} = V_{IL}$	-	40	100	mA
Input Low voltage	V_{IL}		-0.1*	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC}+1^{**}$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

*: DC, 0.6V AC 20ns. **: DC, $V_{CC}+1.5V$ AC 20ns.

** : Mode selection is unfixed between $V_{IH} = V_{CC} + 1V$ and $V_{IH} = 11.5V$.

● AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC}=5\text{V} \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Condition	HN27128AG-17		HN27128AG-20		HN27128AG-25		HN27128AG-30		Unit
			min.	max.	min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$	–	170	–	200	–	250	–	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$	–	170	–	200	–	250	–	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$	–	75	–	75	–	100	–	120	ns
\overline{OE} High Output Float	t_{DF}	$\overline{CE}=V_{IL}$	0	55	0	55	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$	0	–	0	–	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

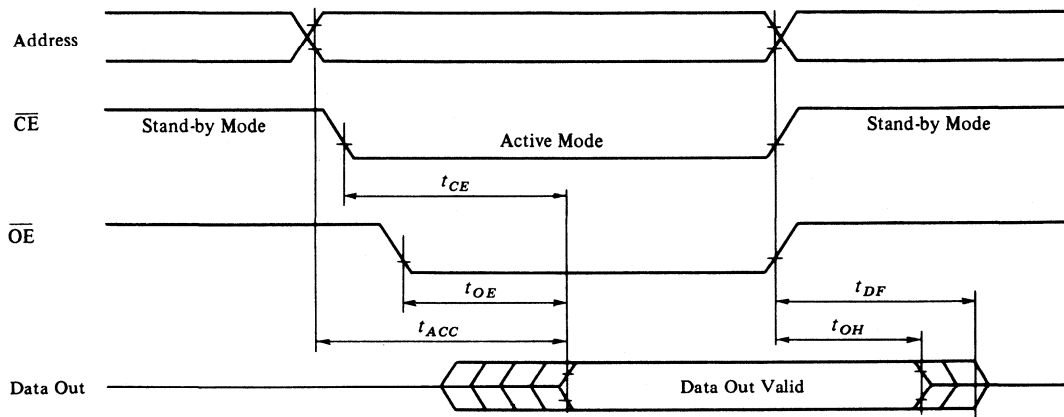
Test Condition

Input Pulse Levels: 0.45V to 2.4V

Input Rise and Fall Time: $\leq 20\text{ns}$

Output Load: 1 TTL Gate +100pF

Reference Level for Measuring Timing: 0.8V and 2.0V

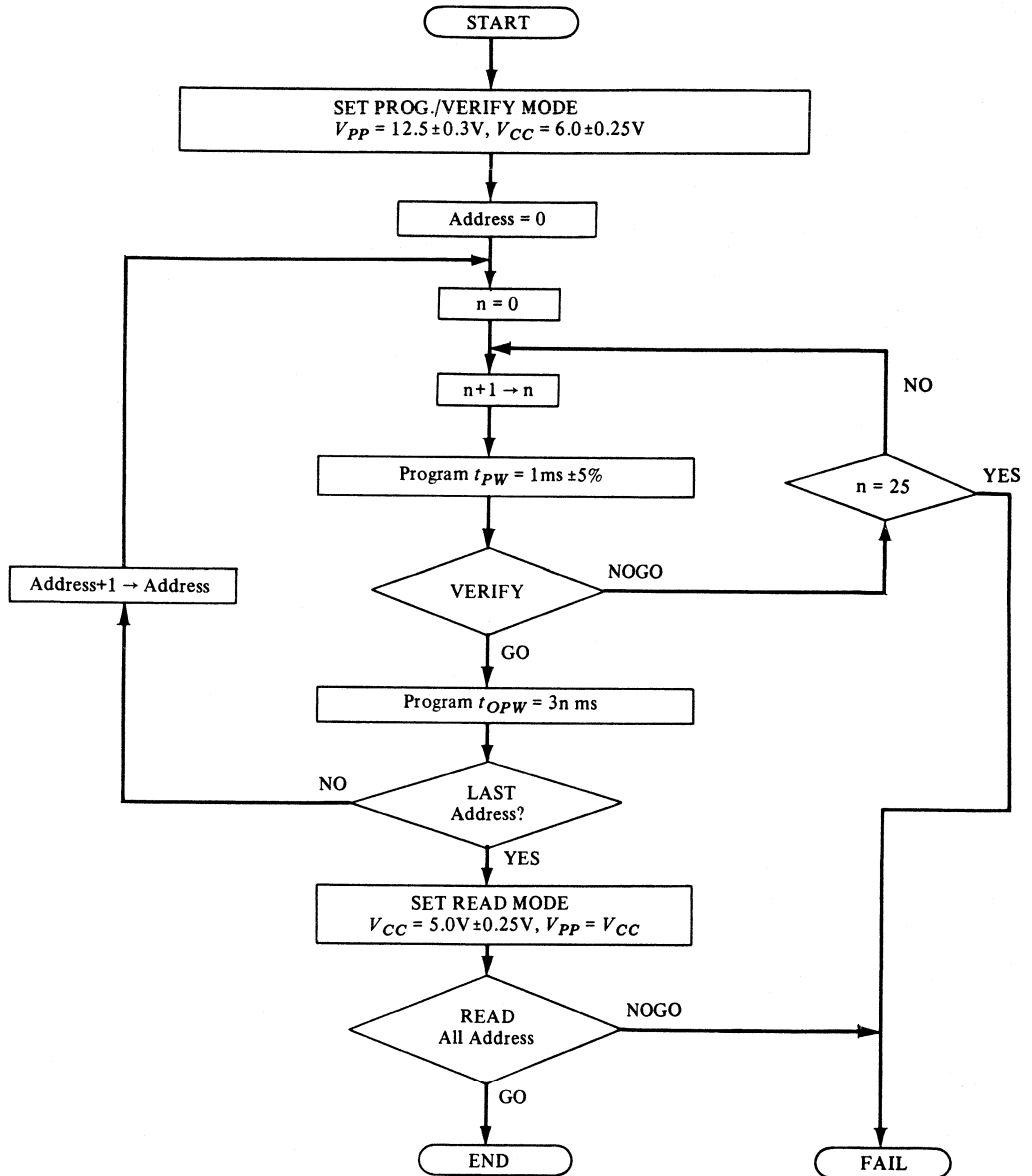


● CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

● HN27128AG SERIES IDENTIFIER CODE

Identifier \ Pins	A ₀ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	Hex Data
Manufacturer Code	V _{IL}	0	0	0	0	0	1	1	1	07
Device Code	V _{IH}	0	0	0	0	1	1	0	1	0D

Notes: 1. A₉ = 12.0V ± 0.5V
 2. A_{1~8}, A_{10~13}, CE, OE = V_{IL}, PGM = V_{IH}.

■ HIGH PERFORMANCE PROGRAMMING OPERATION
● DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V _{OL}	I _{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V _{OH}	I _{OH} = –400μA	2.4	–	–	V
V _{CC} Current (Active)	I _{CC2}		–	–	100	mA
Input Low Level	V _{IL}		–0.1*	–	0.8	V
Input High Level	V _{IH}		2.0	–	V _{CC} **	V
V _{PP} Supply Current	I _{PP2}	CE = V _{IL}	–	–	50	mA

*: DC, –0.6V AC 20ns. **: DC, V_{CC} + 0.5V AC 20ns.
 **: Mode selection is unfixed between V_{IH} = V_{CC} and V_{IH} = 11.5V.

● AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t _{AS}		2	–	–	μs
OE Setup Time	t _{OES}		2	–	–	μs
Data Setup Time	t _{DS}		2	–	–	μs
Address Hold Time	t _{AH}		0	–	–	μs
Data Hold Time	t _{DH}		2	–	–	μs
OE to Output Float Delay	t _{DF}		0	–	130	ns
V _{PP} Setup Time	t _{VPS}		2	–	–	μs
V _{CC} Setup Time	t _{VCS}		2	–	–	μs
PGM Pulse Width During Initial Programming	t _{PW}		0.95	1.0	1.05	ms
CE Pulse Width During Overprogramming	t _{OPW}		2.85	–	78.75	ms
CE Setup Time	t _{CES}		2	–	–	μs
Data Valid from OE	t _{OE}		–	–	150	ns

Notes: t_{OPW} is defined as mentioned in flow chart.

t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

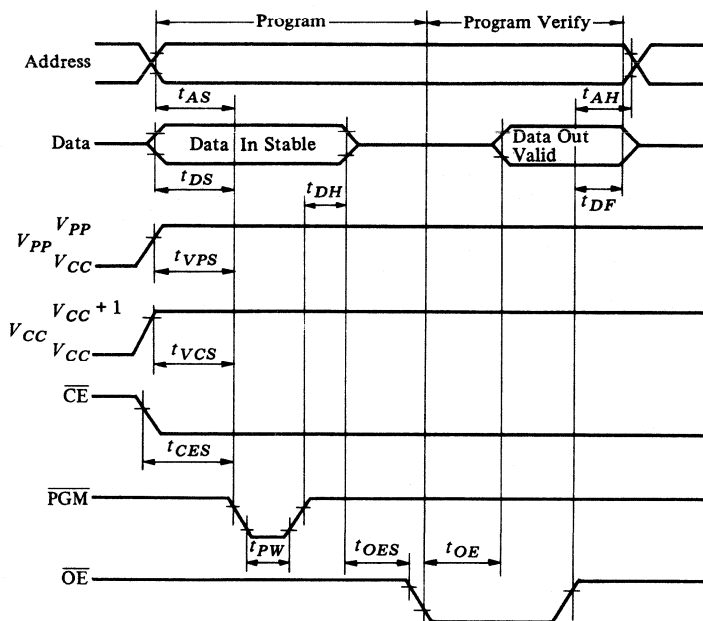
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level: 0.45V to 2.4V

Input Rise and Fall Time: $\leq 20\text{ns}$

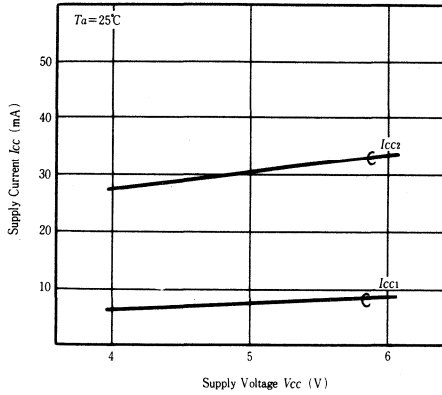
Reference Level for Measuring Timing: 0.8V and 2.0V



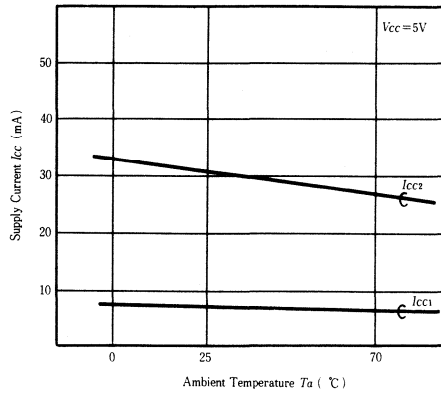
■ ERASE

Erase of HN27128AG is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W.sec/cm².

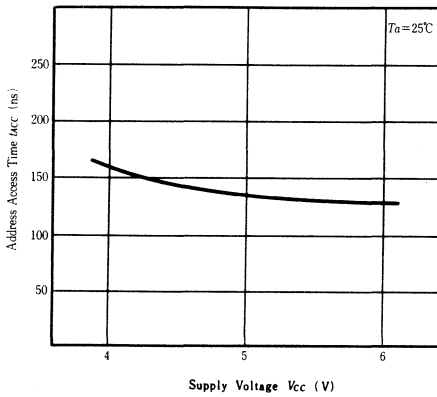
SUPPLY CURRENT VS. SUPPLY VOLTAGE



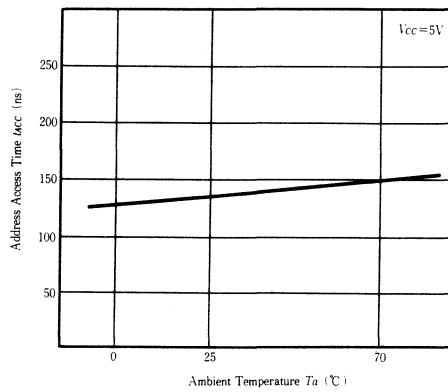
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE



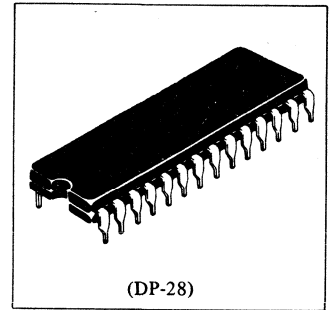
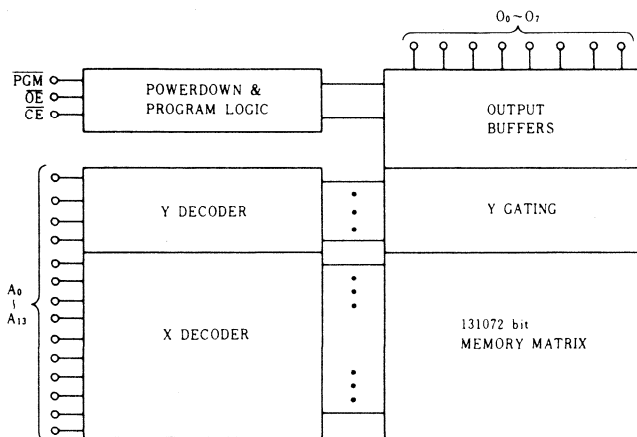
16384-word x 8-bit One Time Electrically Programmable Read Only Memory

The HN27128AP is a 16384-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27128AP are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic dual-in-line package. Therefore, this device can not be re-written.

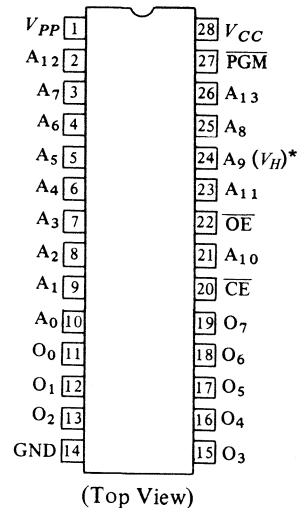
■ FEATURES

- Single Power Supply +5V ±5%
- High Performance Program Voltage: +12.5V D.C.
High Performance Programming Operations
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time HN27128AP-20: 200ns (max.)
HN27128AP-25: 250ns (max.)
HN27128AP-30: 300ns (max.)
- Absolute Max. Rating of 14.0V Max.
V_{pp} pin
- Low Stand-by Current 35mA Max. (stand-by)
- Device Identifier Mode Manufacturer Code and Device Code

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



*V_H = 12.0V ± 0.5V

(Notes) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ MODE SELECTION

MODE	Pins	\overline{CE} (20)	\overline{OE} (22)	PGM (27)	V_{PP} (1)	V_{CC} (28)	A9 (24)	Outputs (11~13, 15~19)
Read		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	×	Dout
Output Disable		V_{IL}	V_{IH}	V_{IH}	V_{CC}	V_{CC}	×	High Z
Stand by		V_{IH}	X	X	V_{CC}	V_{CC}	×	High Z
High Performance Program		V_{IL}	X	V_{IL}	V_{PP}	V_{CC}	×	Din
Program Verify		V_{IL}	V_{IL}	V_{IH}	V_{PP}	V_{CC}	×	Dout
Program Inhibit		V_{IH}	X	X	V_{PP}	V_{CC}	×	High Z
Identifier		V_{IL}	V_{IL}	V_{IH}	V_{CC}	V_{CC}	V_H^*	Code

Note) X . . . Don't care

* $V_H = 12.0\text{ V} \pm 0.5\text{ V}$

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature RAnge Under Bias	T_{bias}	-10 to +80	°C
All Input and Output Voltages*	V_{IN}, V_{out}	-0.6 to +7	V
Voltage on Pin 24 (A9)	V_{ID}	-0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5\text{ V} \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25\text{ V}$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25\text{ V}/0.45\text{ V}$	-	-	10	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.25\text{ V}$	-	-	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}$	-	-	35	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE} = \overline{OE} = V_{IL}$	-	40	100	mA
Input Low voltage	V_{IL}		-0.1*	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1^{**}$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{ mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

*: DC, 0.6V AC 20ns. **: DC, $V_{CC} + 1.5\text{ V}$ AC 20ns.

**: Mode selection is unfixed between $V_{IH} = V_{CC} + 1\text{ V}$ and $V_{IH} = 11.5\text{ V}$.

● **AC CHARACTERISTICS** $T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = V_{CC}$

Parameter	Symbol	Test Condition	HN27128AP-20		HN27128AP-25		HN27128AP-30		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	–	200	–	250	–	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	–	200	–	250	–	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	–	75	–	100	–	120	ns
\overline{OE} High Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	55	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● **SWITCHING CHARACTERISTICS**

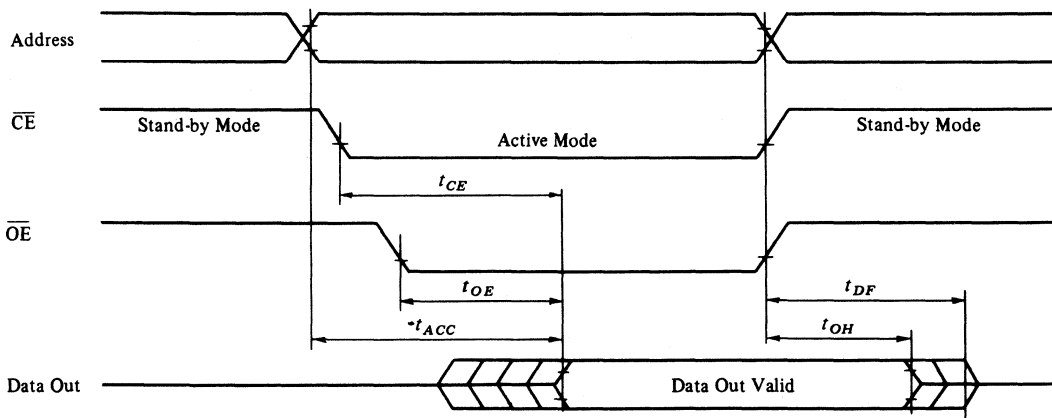
Test Condition

Input Pulse Levels: 0.45V to 2.4V

Input Rise and Fall Time: $\leq 20\text{ns}$

Output Load: 1 TTL Gate +100pF

Reference Level for Measuring Timing: 0.8V and 2.0V

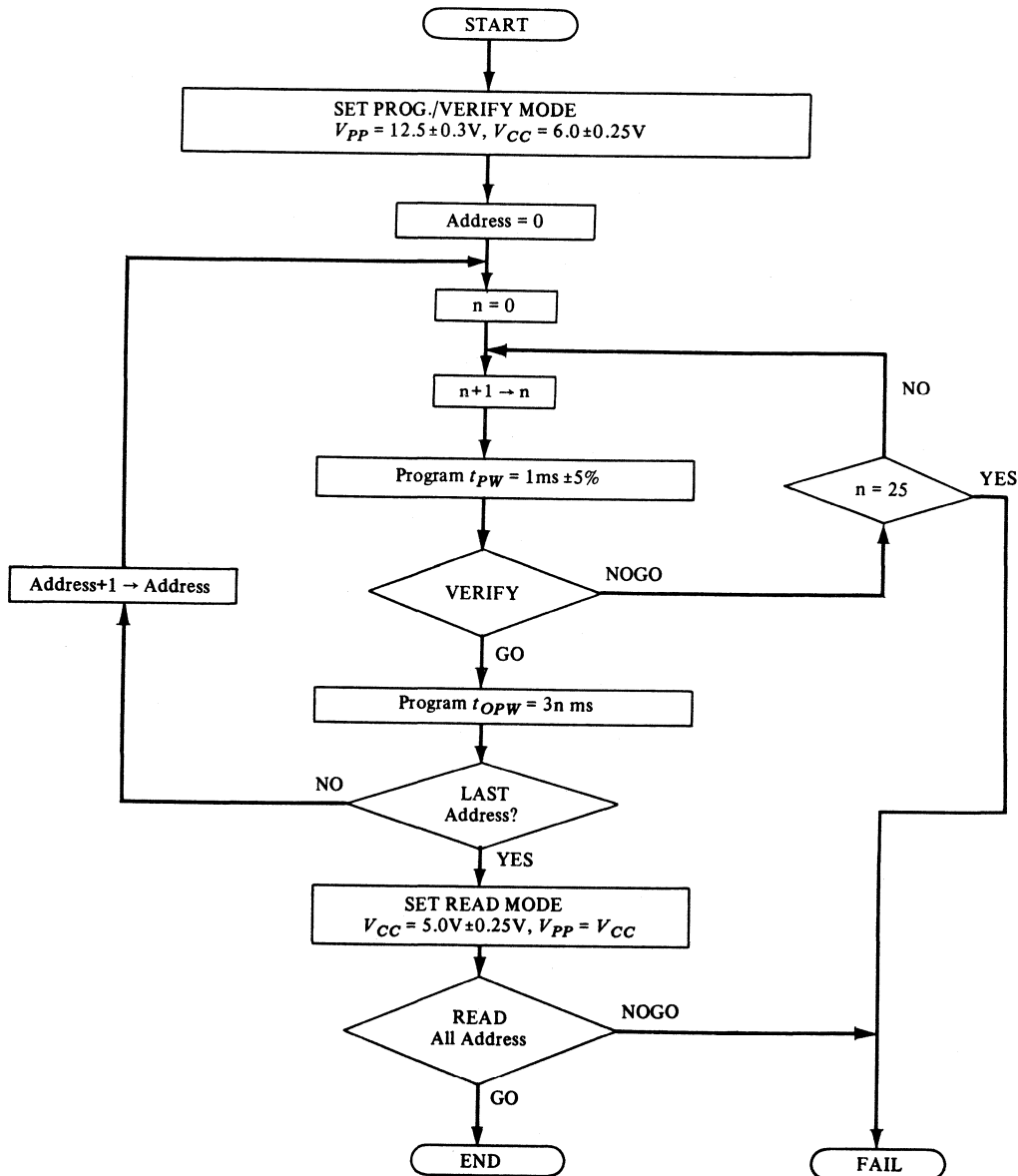


● **CAPACITANCE** ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

● HN27128AP SERIES IDENTIFIER CODE

Identifier	Pins	A ₉ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	Hex Data
Manufacturer Code		V _{IL}	0	0	0	0	0	1	1	1	07
Device Code		V _{IH}	0	0	0	0	1	1	0	1	0D

Notes: 1. A₉ = 12.0V ± 0.5V.
2. A_{1~8}, A_{10~13}, CE, OE = V_{IL}, PGM = V_{IH}.

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V _{OL}	I _{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V _{OH}	I _{OH} = –400μA	2.4	–	–	V
V _{CC} Current (Active)	I _{CC2}		–	–	100	mA
Input Low Level	V _{IL}		–0.1*	–	0.8	V
Input High Level	V _{IH}		2.0	–	V _{CC} **	V
V _{PP} Supply Current	I _{PP2}	CE = PGM = V _{IL}	–	–	50	mA

*: DC, –0.6V AC 20ns. **: DC, V_{CC} + 0.5V AC 20ns.

** : Mode selection is unfixed between V_{IH} = V_{CC} and V_{IH} = 11.5V.

● AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t _{AS}		2	–	–	μs
OE Setup Time	t _{OES}		2	–	–	μs
Data Setup Time	t _{DS}		2	–	–	μs
Address Hold Time	t _{AH}		0	–	–	μs
Data Hold Time	t _{DH}		2	–	–	μs
OE to Output Float Delay	t _{DF}		0	–	130	ns
V _{PP} Setup Time	t _{VPS}		2	–	–	μs
V _{CC} Setup Time	t _{VCS}		2	–	–	μs
PGM Pulse Width During Initial Programming	t _{PW}		0.95	1.0	1.05	ms
CE Pulse Width During Overprogramming	t _{OPW}		2.85	–	78.75	ms
CE Setup Time	t _{CES}		2	–	–	μs
Data Valid from OE	t _{OE}		–	–	150	ns

Notes: t_{OPW} is defined as mentioned in flow chart.

t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

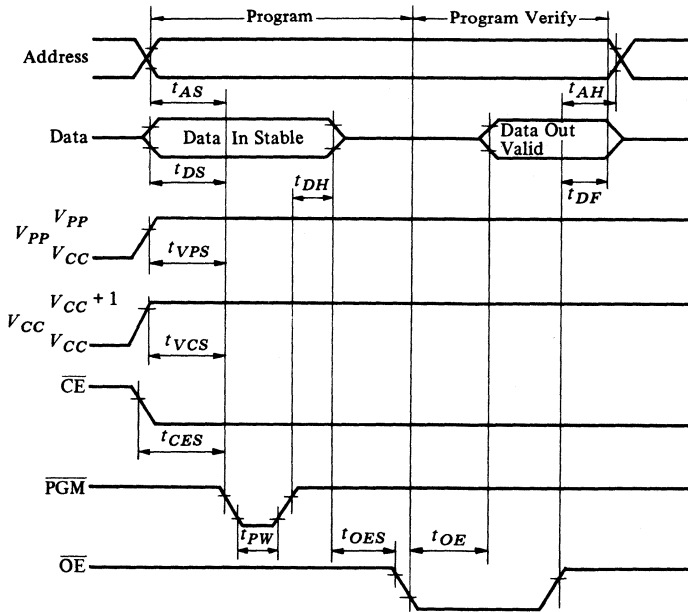
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level: 0.45V to 2.4V

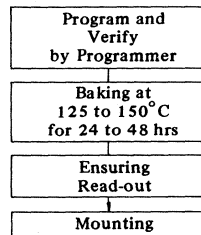
Input Rise and Fall Time: $\leq 20\text{ns}$

Reference Level for Measuring Timing: 0.8V and 2.0V



■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.



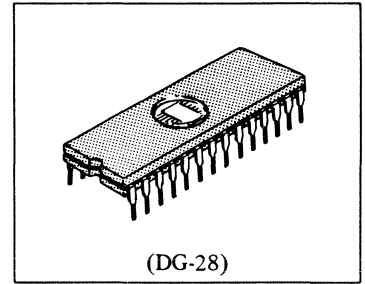
Recommended Screening conditions

HN27256G Series

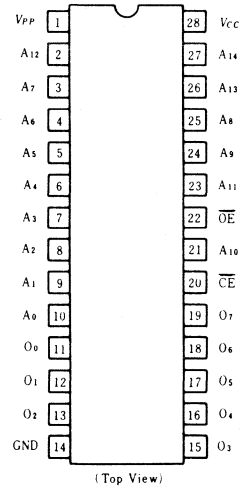
32768-word x 8-bit UV Erasable and Programmable ROM

■ FEATURES

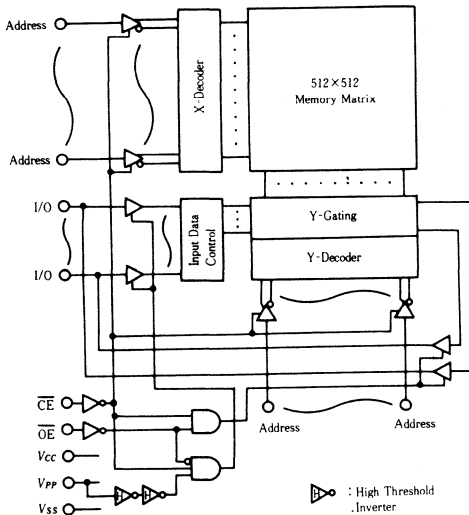
- Single Power Supply +5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V D.C.
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time HN27256G-25: 250ns(max.)
HN27256G-30: 300ns(max.)
- Absolute Max. Rating of V_{PP} pin . . 14.0V
- Low Stand-by Current 40mA (stand-by)
- Device Identifier Mode Manufacturer Code and Device Code
- Compatible with INTEL 27256



■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	Pins	\overline{CE} (20)	\overline{OE} (22)	V_{PP} (1)	V_{CC} (28)	A9 (24)	Outputs (11 ~ 13, 15 ~ 19)
Read		V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	Dout
Output Disable		V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	High Z
Standby		V_{IH}	X	V_{CC}	V_{CC}	X	High Z
High Performance Program		V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	Din
Program Verify		V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	Dout
Optional Verify		V_{IL}	V_{IL}	V_{PP}	V_{CC}	X	Dout
Program Inhibit		V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	High Z
Identifier		V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H	Code

Note) X: Don't care.
 V_H : 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	°C
All Input and Output Voltages*	V_{IN}, V_{out}	-0.6 to +7	V
A9 Input Voltage*	V_{ID}	-0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS $T_a = 0 \sim +70^\circ\text{C}$, $V_{PP} = V_{CC}$ $V_{CC} = 5\text{V} \pm 5\%$

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25\text{V}$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25\text{V}/0.45\text{V}$	-	-	10	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.5\text{V}$	-	-	5	mA
V_{CC} Current (Standby)	I_{CC1}	$\overline{\text{CE}} = V_{IH}$	-	-	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	45	100	mA
Input Low Voltage	V_{IL}		-0.1*	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1^{**}$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V
V_{PP} Voltage	V_{PP}		3.8	-	V_{CC}	V

*: V_{IL} min. = -0.6V for pulse width less than 20ns.

** : V_{IH} max. = $V_{CC} + 1.5\text{V}$ for pulse width less than 20ns.

Note: Mode selection is unfixed between $V_{IH} = V_{CC} + 1\text{V}$ and $V_{IH} = 11.5\text{V}$.

● AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

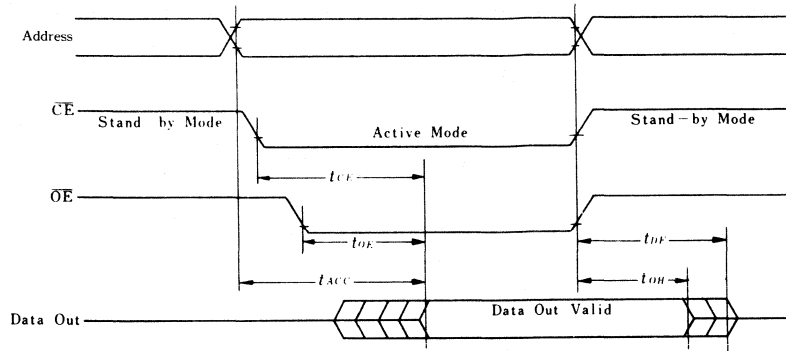
Parameter	Symbol	Test Condition	HN27256G-25		HN27256G-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	-	250	-	300	ns
$\overline{\text{CE}}$ to Output Delay	t_{CE}	$\overline{\text{OE}} = V_{IL}$	-	250	-	300	ns
$\overline{\text{OE}}$ to Output Delay	t_{OE}	$\overline{\text{CE}} = V_{IL}$	-	100	-	120	ns
$\overline{\text{OE}}$ High to Output Float	t_{DF}	$\overline{\text{CE}} = V_{IL}$	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{\text{CE}} = \overline{\text{OE}} = V_{IL}$	0	-	0	-	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
 Input rise and fall time: $\leq 20\text{ns}$
 Output load: 1 TTL Gate +100pF
 Reference level for measuring timing: 0.8V and 2V

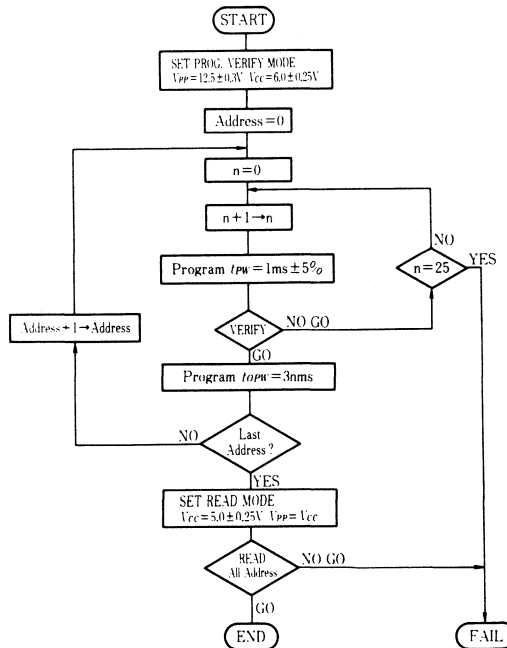


■ CAPACITANCE ($T_a=25^\circ\text{C}, f=1\text{MHz}$)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	$V_{in} = 0\text{ V}$	-	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{ V}$	-	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify Manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

● HN27256G SERIES IDENTIFIER CODE

Identifier	Pins	A ₉ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	Hex Data
Manufacturer Code	V _{IL}	0	0	0	0	0	0	1	1	1	07
Device Code	V _{IH}	0	0	0	1	0	0	0	0	0	10

Notes: 1. A₉ = 12.0V ± 0.5V.
2. A_{1~8}, A_{10~14}, CE, OE = V_{IL}.

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (T_a=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25 V	–	–	10	μA
Output Low Voltage During Verify	V _{OL}	I _{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V _{OH}	I _{OH} = -400 μA	2.4	–	–	V
V _{CC} Current (Active)	I _{CC2}		–	–	100	mA
Input Low Level	V _{IL}		-0.1	–	0.8	V
Input High Level	V _{IH}		2.0	–	V _{CC}	V
V _{PP} Supply Current	I _{PP2}	CE = V _{IL}	–	–	50	mA

● AC PROGRAMMING CHARACTERISTICS (T_a=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t _{AS}		2	–	–	μs
OE Setup Time	t _{OES}		2	–	–	μs
Data Setup Time	t _{DS}		2	–	–	μs
Address Hold Time	t _{AH}		0	–	–	μs
Data Hold Time	t _{DH}		2	–	–	μs
OE to Output Float Delay	t _{DF}		0	–	130	ns
V _{PP} Setup Time	t _{VPS}		2	–	–	μs
V _{CC} Setup Time	t _{VCP}		2	–	–	μs
PGM Pulse Width During Initial Programming	t _{PW}		0.95	1.0	1.05	ms
CE Pulse Width During Overprogramming	t _{OPW}		2.85	–	78.75	ms
Data Valid from OE	t _{OE}		–	–	150	ns

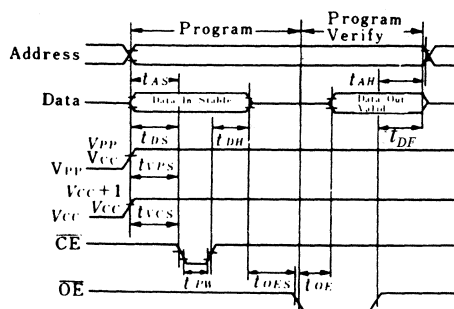
Notes: t_{OPW} is defined as mentioned in flow chart.

t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

■ SWITCHING CHARACTERISTICS

● TEST CONDITION

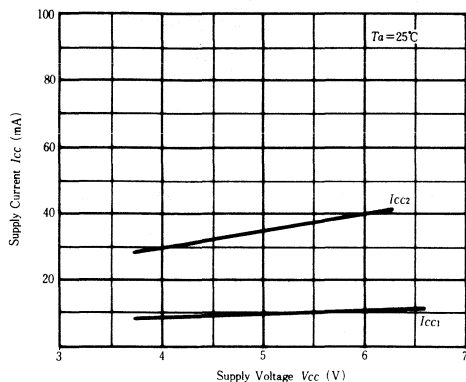
- Input pulse level: 0.45V to 2.4V
- Input rise and fall time: ≤ 20ns
- Reference level for measuring time: 0.8V and 2V



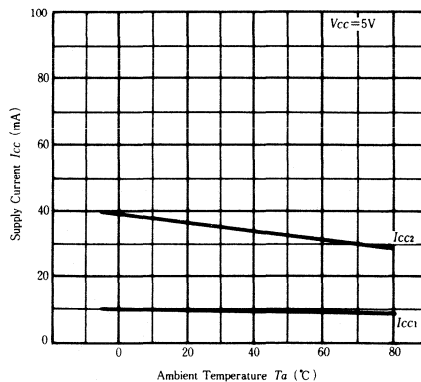
■ ERASE

Erasure of HN27256G is performed by exposure to ultraviolet light of 2537Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm²

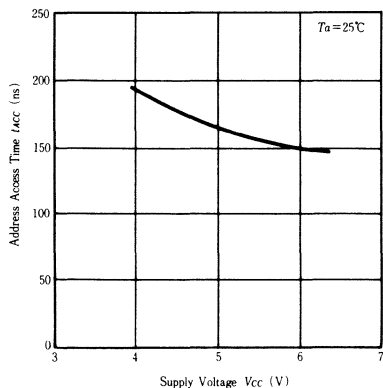
SUPPLY CURRENT VS. SUPPLY VOLTAGE



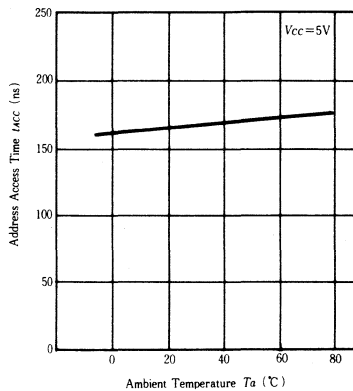
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. SUPPLY VOLTAGE



ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE

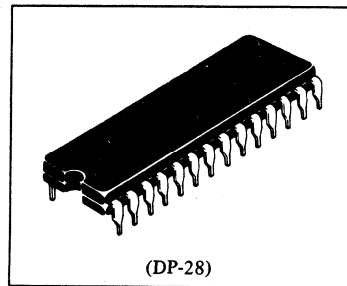


32768-word x 8-bit One Time Electrically Programmable ROM

The HN27256P is a 32768-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27256P are in the "1" state (Output High) Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28-pin, dual-in-line plastic package, therefore, this device can not be rewritten.

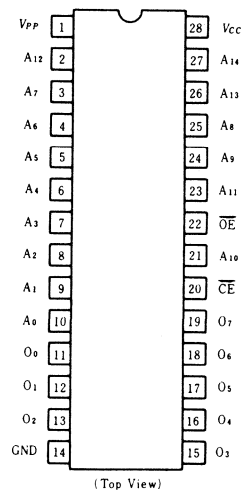
■ FEATURES

- Single Power Supply +5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V D.C.
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time HN27256P-25: 250ns (max.)
HN27256P-30: 300ns (max.)
- Absolute Max. Rating of V_{PP} pin . . 14.0V
- Low Stand-by Current 40mA (stand-by)
- Device Identifier Mode Manufacturer Code and Device Code

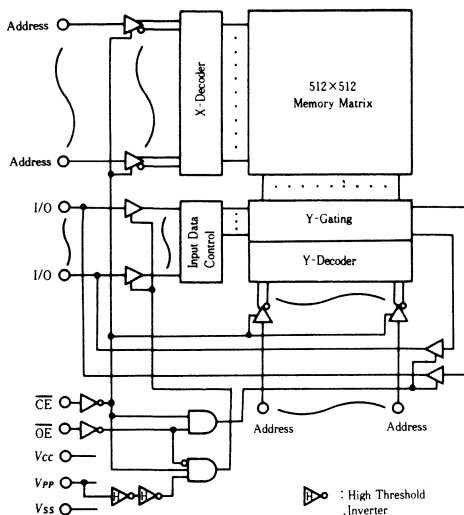


(DP-28)

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



Notes) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ MODE SELECTION

Mode	Pins	CE (20)	OE (22)	V _{PP} (1)	V _{CC} (28)	A9 (24)	Outputs (11 ~ 13, 15 ~ 19)
Read		V _{IL}	V _{IL}	V _{CC}	V _{CC}	X	Dout
Output Disable		V _{IL}	V _{IH}	V _{CC}	V _{CC}	X	High Z
Standby		V _{IH}	X	V _{CC}	V _{CC}	X	High Z
High Performance Program		V _{IL}	V _{IH}	V _{PP}	V _{CC}	X	Din
Program Verify		V _{IH}	V _{IL}	V _{PP}	V _{CC}	X	Dout
Optional Verify		V _{IL}	V _{IL}	V _{PP}	V _{CC}	X	Dout
Program Inhibit		V _{IH}	V _{IH}	V _{PP}	V _{CC}	X	High Z
Identifier		V _{IL}	V _{IL}	V _{CC}	V _{CC}	V _H	Code

Note) X: Don't care.
V_H: 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Operating Temperature Range	T _{opr}	0 to +70	°C
Storage Temperature Range	T _{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T _{bias}	-10 to +80	°C
All Input and Output Voltages*	V _{IN} , V _{out}	-0.6 to +7	V
A9 Input Voltage*	V _{ID}	-0.6 to +12.5	V
V _{PP} Voltage*	V _{PP}	-0.6 to +14.0	V
V _{CC} Voltage*	V _{CC}	-0.6 to +7	V

* with respect to GND.

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS (T_a=0~+70°C, V_{CC}=5V±5%)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25V	-	-	10	μA
Output Leakage Current	I _{LO}	V _{out} = 5.25V/0.45V	-	-	10	μA
V _{PP} Current	I _{PP1}	V _{PP} = 5.5 V	-	-	5	mA
V _{CC} Current (Standby)	I _{CC1}	$\overline{CE} = V_{IH}$	-	-	40	mA
V _{CC} Current (Active)	I _{CC2}	$\overline{CE} = \overline{OE} = V_{IL}$	-	45	100	mA
Input Low Voltage	V _{IL}		-0.1*	-	0.8	V
Input High Voltage	V _{IH}		2.0	-	V _{CC} + 1**	V
Output Low Voltage	V _{OL}	I _{OL} = 2.1 mA	-	-	0.45	V
Output High Voltage	V _{OH}	I _{OH} = -400 μA	2.4	-	-	V
V _{PP} Voltage	V _{PP}		3.8	-	V _{CC}	V

*: V_{IL} min. = -0.6V for pulse width less than 20ns.

** : V_{IH} max. = V_{CC} + 1.5V for pulse width less than 20ns.

Note: Mode selection is unfixed between V_{IH} = V_{CC} + 1V and V_{IH} = 11.5V.

● AC CHARACTERISTICS (T_a=0~70°C, V_{CC}=5V±5%)

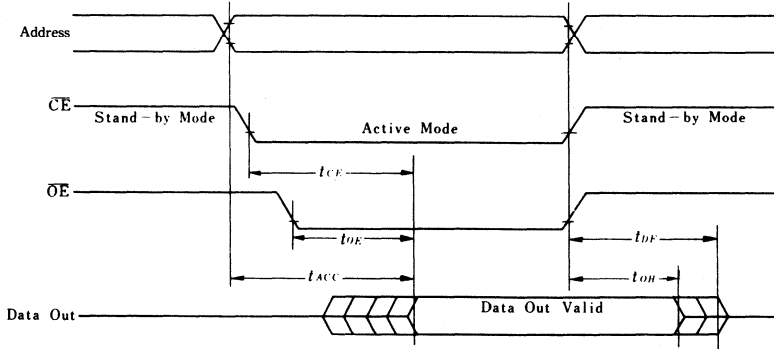
Parameter	Symbol	Test Condition	HN27256P-25		HN27256P-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t _{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	-	250	-	300	ns
\overline{CE} to Output Delay	t _{CE}	$\overline{OE} = V_{IL}$	-	250	-	300	ns
\overline{OE} to Output Delay	t _{OE}	$\overline{CE} = V_{IL}$	-	100	-	120	ns
\overline{OE} High to Output Float	t _{DF}	$\overline{CE} = V_{IL}$	0	60	0	105	ns
Address to Output Hold	t _{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	-	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
 Input rise and fall time: ≤20ns
 Output load: 1 TTL Gate +100pF
 Reference level for measuring timing: 0.8V and 2V



■ CAPACITANCE (T_a=25°C, f=1MHz)

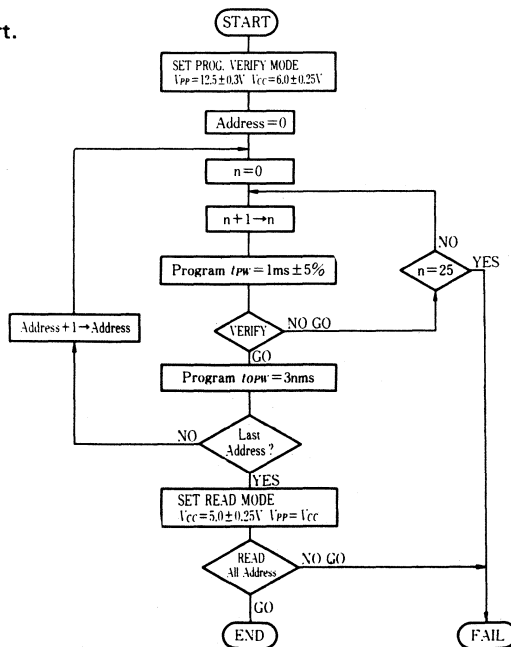
Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C _{in}	V _{in} = 0 V	—	4	6	pF
Output Capacitance	C _{out}	V _{out} = 0 V	—	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify Manufacturer and type of device from outputs EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.



High Performance Programming Flowchart

● **HN27256P SERIES IDENTIFIER CODE**

Identifier	Pins	A ₀ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	H&Lx Data
Manufacturer Code		V _{IL}	0	0	0	0	0	1	1	1	07
Device Code		V _{IH}	0	0	0	1	0	0	0	0	10

Notes: 1. A₉ = 12.0V ± 0.5V.
 2. A_{1~8}, A_{10~14}, \overline{CE} , \overline{OE} = V_{IL}.

■ **HIGH PERFORMANCE PROGRAMMING OPERATION**

● **DC PROGRAMMING CHARACTERISTICS** (T_a=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25 V	–	–	10	μA
Output Low Voltage During Verify	V _{OL}	I _{OL} = 2.1 mA	–	–	0.45	V
Output High Voltage During Verify	V _{OH}	I _{OH} = –400 μA	2.4	–	–	V
V _{CC} Current (Active)	I _{CC2}		–	–	100	mA
Input Low Level	V _{IL}		–0.1	–	0.8	V
Input High Level	V _{IH}		2.0	–	V _{CC}	V
V _{PP} Supply Current	I _{PP2}	\overline{CE} = V _{IL}	–	–	50	mA

● **AC PROGRAMMING CHARACTERISTICS** (T_a=25°C±5°C, V_{CC}=6V±0.25V, V_{PP}=12.5V±0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t _{AS}		2	–	–	μs
\overline{OE} Setup Time	t _{OES}		2	–	–	μs
Data Setup Time	t _{DS}		2	–	–	μs
Address Hold Time	t _{AH}		0	–	–	μs
Data Hold Time	t _{DH}		2	–	–	μs
\overline{OE} to Output Float Delay	t _{DF}		0	–	130	ns
V _{PP} Setup Time	t _{VPS}		2	–	–	μs
V _{CC} Setup Time	t _{VCP}		2	–	–	μs
PGM Pulse Width During Initial Programming	t _{PW}		0.95	1.0	1.05	ms
\overline{CE} Pulse Width During Overprogramming	t _{OPW}		2.85	–	78.75	ms
Data Valid from \overline{OE}	t _{OE}		–	–	150	ns

Notes: t_{OPW} is defined as mentioned in flow chart.

t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

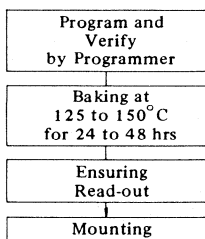
■ **SWITCHING CHARACTERISTICS**

● **TEST CONDITION**

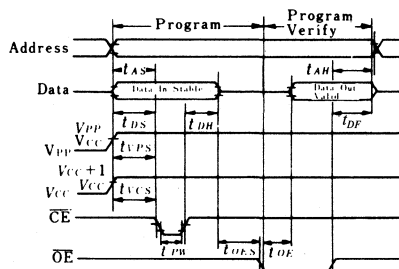
- Input pulse level: 0.45V to 2.4V
- Input rise and fall time: ≤ 20ns
- Reference level for measuring time: 0.8V and 2V

■ **RECOMMENDED SCREENING CONDITIONS**

Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

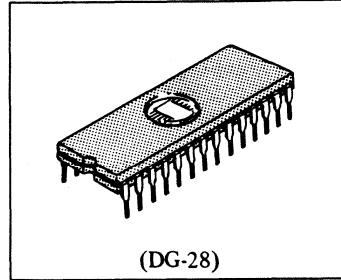


HN27C256G Series

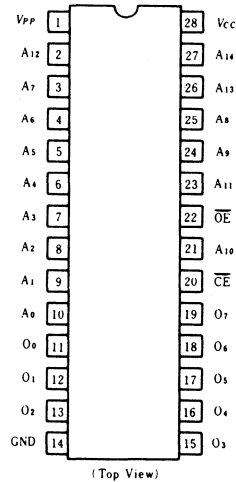
32768-word x 8-bit CMOS UV Erasable and Programmable ROM

■ FEATURES

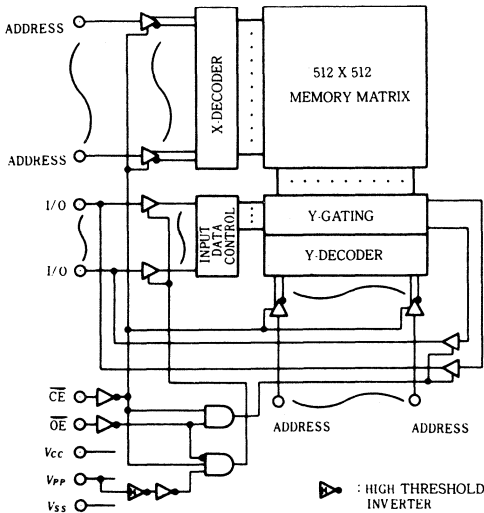
- Low Power Dissipation 20mW/MHz typ. (Active Mode)
5μW typ. (Standby Mode)
- Access Time 170ns max. (HN27C256G-17)
200ns max. (HN27C256G-20)
250ns max. (HN27C256G-25)
300ns max. (HN27C256G-30)
- Single Power Supply 5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V DC
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Absolute Max. Rating of V_{PP} pin. . . 14.0V
- Device Identifier Mode Manufacturer Code and Device Code
- Compatible with INTEL 27256



■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	Pins	\overline{CE} (20)	\overline{OE} (22)	V_{PP} (1)	V_{CC} (28)	A9 (24)	Outputs (11 ~ 13, 15 ~ 19)
Read		V_{IL}	V_{IL}	V_{CC}	V_{CC}	X	Dout
Output Disable		V_{IL}	V_{IH}	V_{CC}	V_{CC}	X	High Z
Standby		V_{IH}	X	V_{CC}	V_{CC}	X	High Z
High Performance Program		V_{IL}	V_{IH}	V_{PP}	V_{CC}	X	Din
Program Verify		V_{IH}	V_{IL}	V_{PP}	V_{CC}	X	Dout
Optional Verify		V_{IL}	V_{IL}	V_{PP}	V_{CC}	X	Dout
Program Inhibit		V_{IH}	V_{IH}	V_{PP}	V_{CC}	X	High Z
Identifier		V_{IL}	V_{IL}	V_{CC}	V_{CC}	V_H	Code

Note) X: Don't care.
 V_H : 12.0V ± 0.5V.

■ ABSOLUTE MAXIMUM RATING

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	°C
All Input and Output Voltages*	V_{IN}, V_{OUT}	-1.0** to +7	V
Voltage on Pin 24 (A9)*	V_{ID}	-0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND. ** Pulse width: 50ns, DC: V_{IL} min = -0.6V

● HN27C256G IDENTIFIER CODES

Identifier	Pins										Hex Data
	A ₀ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)		
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07	
Device Code	V_{IH}	1	0	1	1	0	0	0	0	B0	

Notes: 1. A₉ = 12.0V ± 0.5V.
2. A_{1~8}, A_{10~14}, \overline{CE} , \overline{OE} = V_{IL} .

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim +70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in} = 5.25V$	-	-	2	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25V/0.4V$	-	-	2	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.5V$	-	1	20	μA
V_{CC} Current (Standby)	I_{SB1}	$\overline{CE} = V_{IH}$	-	-	1	mA
	I_{SB2}	$\overline{CE} = V_{CC} \pm 0.3V$	-	1	20	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE} = V_{IL}, I_{out} = 0 \text{ mA}$	-	-	30	mA
	I_{CC2}	$f = 5 \text{ MHz}, I_{out} = 0 \text{ mA}$	-	-	30	mA
	I_{CC3}	$f = 1 \text{ MHz}, I_{out} = 0 \text{ mA}$	-	-	8	mA
Input Voltage	V_{IL}		-1.0*	-	0.8	V
	V_{IH}		2.2	-	$V_{CC} + 1.5^{**}$	V
Output Voltage	V_{OL}	$I_{OL} = 2.1 \text{ mA}$	-	-	0.45	V
	V_{OH1}	$I_{OH} = -400 \text{ μA}$	2.4	-	-	V
	V_{OH2}	$I_{OH} = -100 \text{ μA}$	$V_{CC} - 0.7$	-	-	V
V_{PP} Voltage	V_{PP}		3.8	-	V_{CC}	V

* Pulse width: 50ns, DC: V_{IL} min = -0.3V

** Pulse width ≤ 20ns, DC: V_{IH} max = $V_{CC} + 1.0V$.

Mode may be unfix: $V_{IH} = V_{CC} + 1 \sim 11.5V$.

● AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

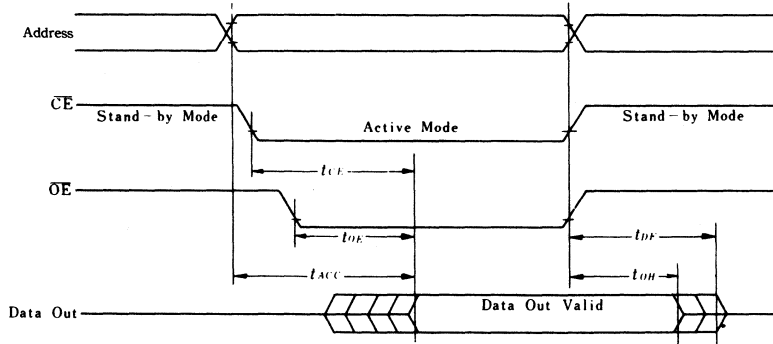
Parameter	Symbol	Test Condition	HN27C256G-17		HN27C256G-20		HN27C256G-25		HN27C256G-30		Unit
			min.	max.	min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	-	170	-	200	-	250	-	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	-	170	-	200	-	250	-	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	10	60	10	70	10	100	10	150	ns
\overline{OE} High to Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	50	0	50	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	-	0	-	0	-	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

TEST CONDITION

Input pulse levels: 0.45V to 2.4V
 Input rise and fall time: ≤20ns
 Output load: 1 TTL Gate +100pF
 Reference level for measuring timing: 0.8V and 2.0V

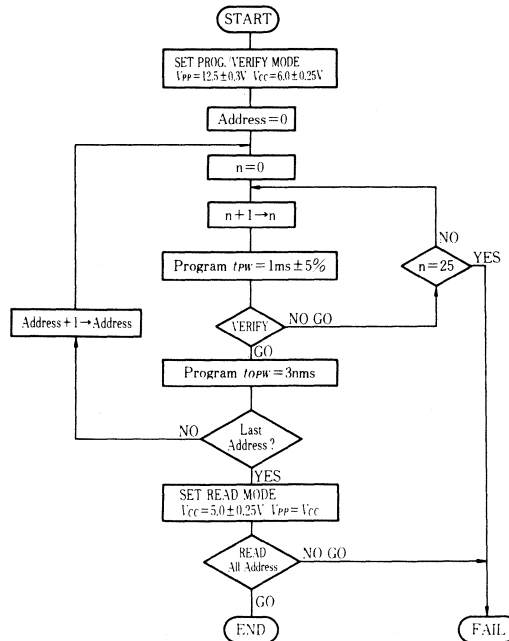


■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	$V_{in} = 0\text{ V}$	-	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{ V}$	-	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C}\pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V}\pm 0.25\text{V}$, $V_{PP}=12.5\text{V}\pm 0.3\text{V}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 6.25\text{V}/0.45\text{V}$	-	-	2	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1\text{ mA}$	-	-	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4	-	-	V
V_{CC} Current (Active)	I_{CC2}		-	-	100	mA
Input Low Level	V_{IL}		-0.1	-	0.8	V
Input High Level	V_{IH}		2.2	-	V_{CC}	V
V_{PP} Supply Current	I_{PP2}	$\overline{\text{CE}} = V_{IL}$	-	-	30	mA

- Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 2. V_{PP} must not exceed 13V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{\text{CE}} = \text{Low}$.

● AC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C}\pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V}\pm 0.25\text{V}$, $V_{PP}=12.5\text{V}\pm 0.3\text{V}$)

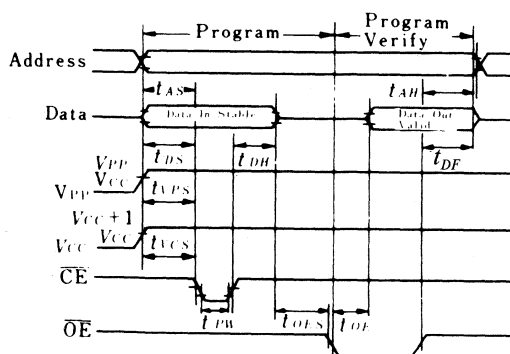
Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	-	-	μs
$\overline{\text{OE}}$ Setup Time	t_{OES}		2	-	-	μs
Data Setup Time	t_{DS}		2	-	-	μs
Address Hold Time	t_{AH}		0	-	-	μs
Data Hold Time	t_{DH}		2	-	-	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}		0	-	130	ns
V_{PP} Setup Time	t_{VPS}		2	-	-	μs
V_{CC} Setup Time	t_{VCS}		2	-	-	μs
PGM Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{\text{CE}}$ Pulse Width During Overprogramming	t_{OPW}		2.85	-	78.75	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	-	-	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		0	-	150	ns

- Notes: t_{OPW} is defined as mentioned in flow chart.
 t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

■ SWITCHING CHARACTERISTICS

● TEST CONDITION

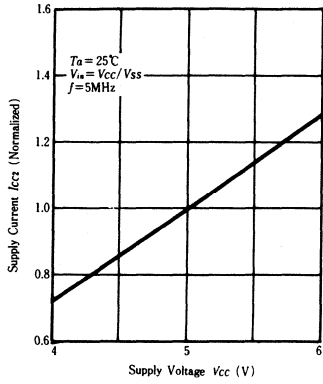
- Input pulse level: 0.45V to 2.4V
- Input rise and fall time: $\leq 20\text{ns}$
- Reference level for measuring time: 0.8V and 2V



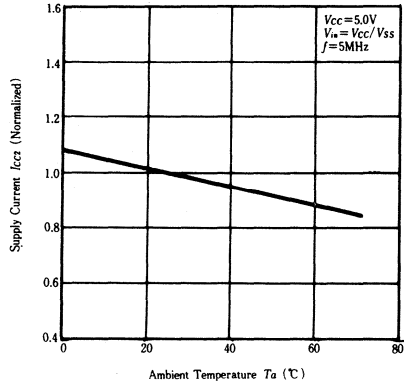
■ ERASE

Erasure of HN27C256G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm²

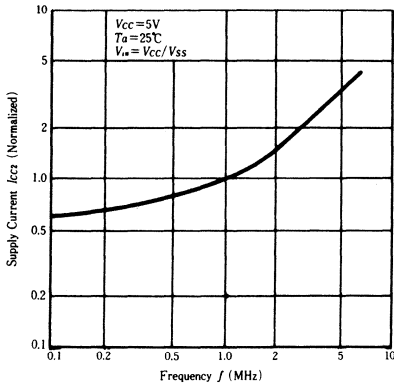
SUPPLY CURRENT VS. SUPPLY VOLTAGE



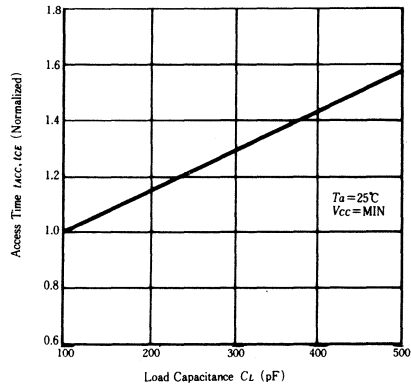
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



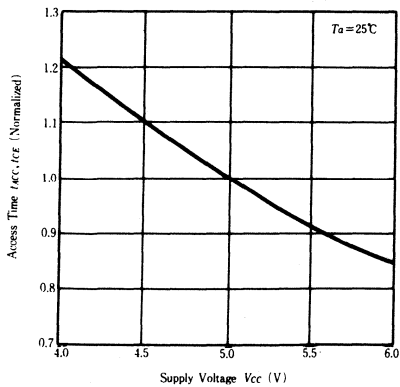
SUPPLY CURRENT VS. FREQUENCY



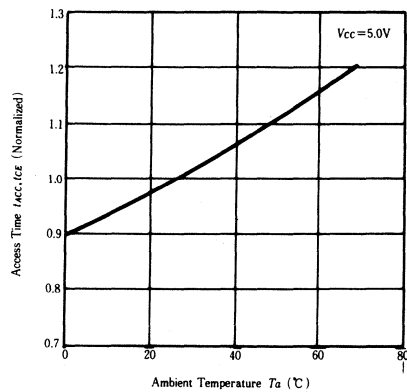
ACCESS TIME VS. LOAD CAPACITANCE



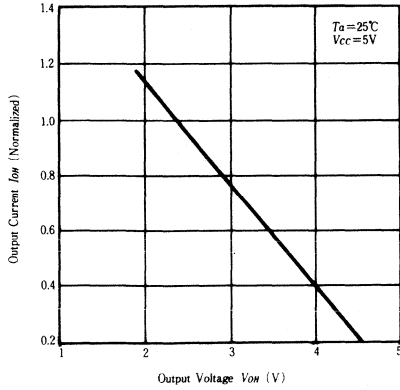
ACCESS TIME VS. SUPPLY VOLTAGE



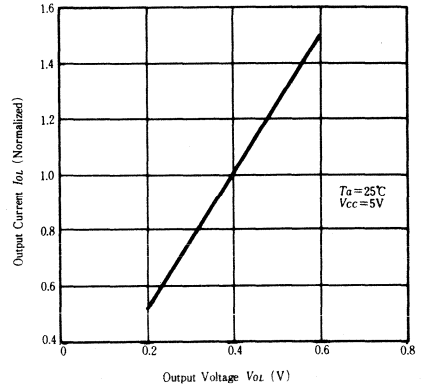
ACCESS TIME VS. AMBIENT TEMPERATURE



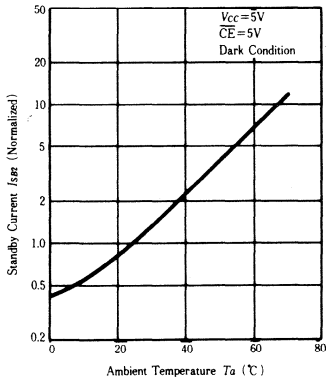
OUTPUT CURRENT VS. OUTPUT VOLTAGE



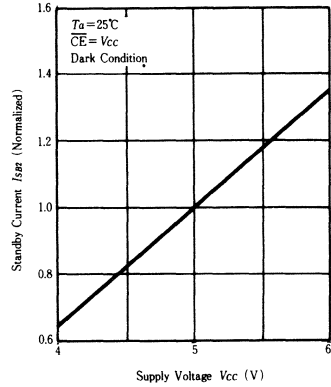
OUTPUT CURRENT VS. OUTPUT VOLTAGE



STANDBY CURRENT VS. AMBIENT TEMPERATURE



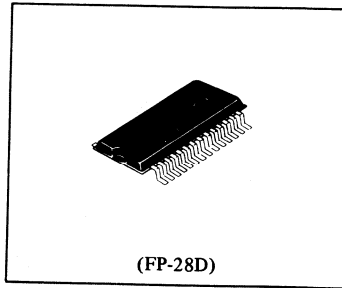
STANDBY CURRENT VS. SUPPLY VOLTAGE



HN27C256FP Series

32768-word x 8-bit CMOS UV Erasable and Programmable ROM

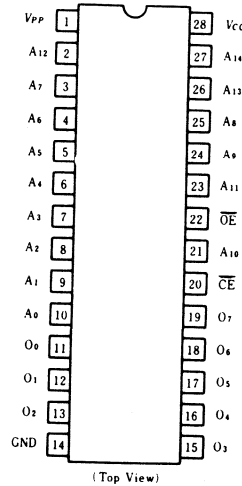
The HN27C256FP is a 32768-word by 8-bit on time electrically programmable ROM. Initially, all bits of the HN27C256FP are in the "1" State (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic flat package (SOP). Therefore, this device cannot be re-written.



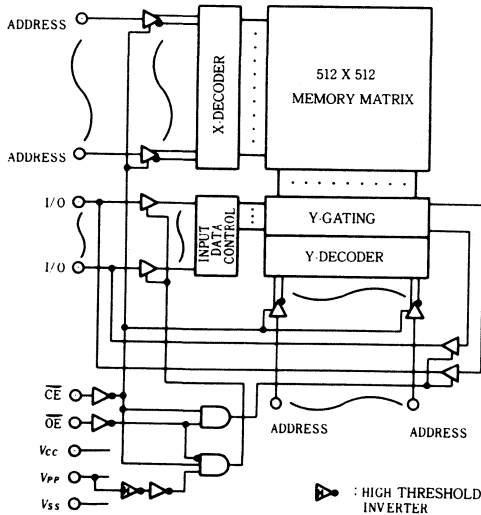
■ FEATURES

- Low Power Dissipation 20mW/MHz typ. (Active Mode)
5μW typ. (Standby Mode)
- Access Time 200ns max. (HN27C256FP-20)
250ns max. (HN27C256FP-25)
300ns max. (HN27C256FP-30)
- Single Power Supply 5V ± 5%
- High Performance Programming . . Program Voltage: +12.5V DC
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Absolute Max. Rating of V_{PP} pin . . . 14.0V
- Device Identifier Code Manufacturer Code and Device Code

■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ MODE SELECTION

Mode	Pins	\overline{CE} (20)	\overline{OE} (22)	A9 (24)	V_{PP} (1)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read		V_{IL}	V_{IL}	X	V_{CC}	V_{CC}	Dout
Output Disable		V_{IL}	V_{IH}	X	V_{CC}	V_{CC}	High Z
Standby		V_{IH}	X	X	V_{CC}	V_{CC}	High Z
High Performance Program		V_{IL}	V_{IH}	X	V_{PP}	V_{CC}	Din
Program Verify		V_{IH}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Operational Verify		V_{IL}	V_{IL}	X	V_{PP}	V_{CC}	Dout
Program Inhibit		V_{IH}	V_{IH}	X	V_{PP}	V_{CC}	High Z
Identifier		V_{IL}	V_{IL}	V_H	V_{CC}	V_{CC}	Code

Note) X: Don't care.
 V_H : $12.0 \pm 0.5V$.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	°C
All Input and Output Voltages*	V_{IN}, V_{OUT}	-1.0** to +7	V
Voltage on Pin 24 (A9)	V_{ID}	-0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND. ** Pulse width: 50ns, DC: V_{IL} min = -0.6V

● HN27C256FP IDENTIFIER CODES

Pins	A ₀	O ₇	O ₆	O ₅	O ₄	O ₃	O ₂	O ₁	O ₀	Hex Data
Identifier (10)	(10)	(19)	(18)	(17)	(16)	(15)	(13)	(12)	(11)	
Manufacturer Code	V_{IL}	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	1	0	1	1	0	0	0	0	B0

Notes: 1. A₉ = $12.0V \pm 0.5V$.
 2. A_{1~8}, A_{10~14}, \overline{CE} , \overline{OE} = V_{IL} .

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim +70^\circ C$, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{in} = 5.25V$	-	-	2	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25V/0.4V$	-	-	2	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.5V$	-	1	20	μA
V_{CC} Current (Standby)	I_{SB1}	$\overline{CE} = V_{IH}$	-	-	1	mA
	I_{SB2}	$\overline{CE} = V_{CC} \pm 0.3V$	-	1	20	μA
V_{CC} Current (Active)	I_{CC1}	$\overline{CE} = V_{IL}, I_{out} = 0 \text{ mA}$	-	-	30	mA
	I_{CC2}	$f = 5 \text{ MHz}, I_{out} = 0 \text{ mA}$	-	-	30	mA
	I_{CC3}	$f = 1 \text{ MHz}, I_{out} = 0 \text{ mA}$	-	-	8	mA
Input Voltage	V_{IL}		-1.0*	-	0.8	V
	V_{IH}		2.2	-	$V_{CC} + 1.5^{**}$	V
Output Voltage	V_{OL}	$I_{OL} = 2.1 \text{ mA}$	-	-	0.45	V
	V_{OH1}	$I_{OH} = -400 \mu A$	2.4	-	-	V
	V_{OH2}	$I_{OH} = -100 \mu A$	$V_{CC} - 0.7$	-	-	V
V_{PP} Voltage	V_{PP}		3.8	-	V_{CC}	V

* Pulse width: 50ns, DC: V_{IL} min = -0.3V

** Pulse width ≤ 20 ns, DC V_{IH} max = $V_{CC} + 1.0V$.

Mode may be unfixed: $V_{IH} = V_{CC} + 1 \sim 11.5V$.

● AC CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$, $V_{PP} = V_{CC}$)

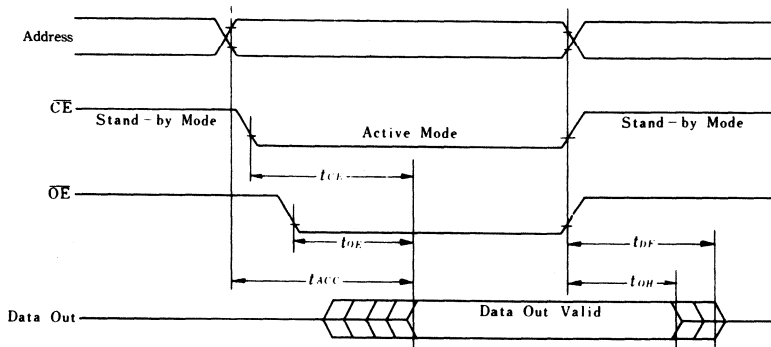
Parameter	Symbol	Test Condition	HN27C256FP-20		HN27C256FP-25		HN27C256FP-30		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	–	200	–	250	–	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	–	200	–	250	–	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	10	70	10	100	10	150	ns
\overline{OE} High to Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	50	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

■ SWITCHING CHARACTERISTICS

TEST CONDITION

- Input pulse levels: 0.45V to 2.4V
- Input rise and fall time: $\leq 20\text{ns}$
- Output load: 1 TTL Gate +100pF
- Reference level for measuring timing: 0.8V and 2.0V

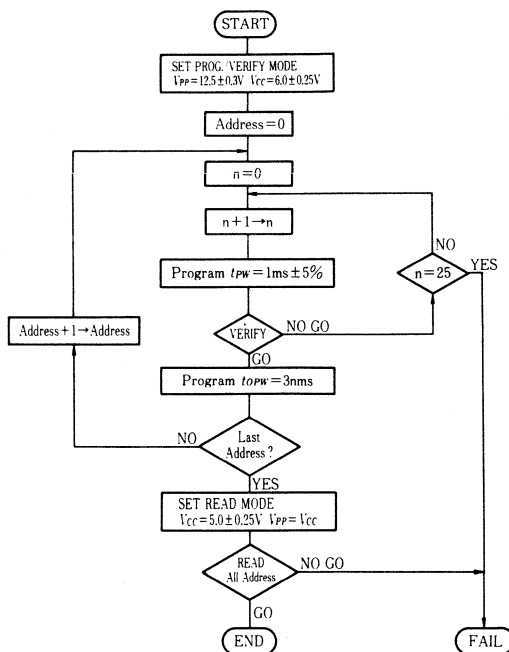


■ CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit.
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	–	4	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C}\pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V}\pm 0.25\text{V}$, $V_{PP}=12.5\text{V}\pm 0.3\text{V}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 6.25\text{V}/0.45\text{V}$	–	–	2	μA
Output Low Voltage During Verify	V_{OL}	$I_{OL} = 2.1\text{ mA}$	–	–	0.45	V
Output High Voltage During Verify	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4	–	–	V
V_{CC} Current (Active)	I_{CC2}		–	–	30	mA
Input Low Level	V_{IL}		-0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}	V
V_{PP} Supply Current	I_{PP2}	$\overline{\text{CE}} = V_{IL}$	–	–	40	mA

- Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 2. V_{PP} must not exceed 13V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{\text{CE}} = \text{Low}$.

● AC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C}\pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V}\pm 0.25\text{V}$, $V_{PP}=12.5\text{V}\pm 0.3\text{V}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	-	-	μs
$\overline{\text{OE}}$ Setup Time	t_{OES}		2	-	-	μs
Data Setup Time	t_{DS}		2	-	-	μs
Address Hold Time	t_{AH}		0	-	-	μs
Data Hold Time	t_{DH}		2	-	-	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}		0	-	130	ns
V_{PP} Setup Time	t_{VPS}		2	-	-	μs
V_{CC} Setup Time	t_{VCS}		2	-	-	μs
PGM Pulse Width During Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{\text{CE}}$ Pulse Width During Overprogramming	t_{OPW}		2.85	-	78.75	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	-	-	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		0	-	150	ns

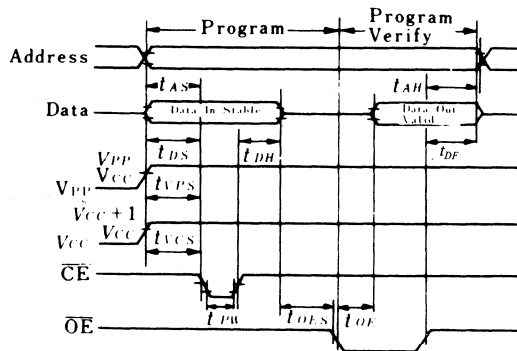
Notes: t_{OPW} is defined as mentioned in flow chart.

t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

■ SWITCHING CHARACTERISTICS

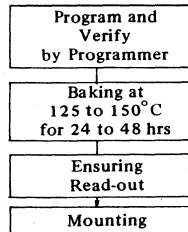
● TEST CONDITION

- Input pulse level: 0.45V to 2.4V
- Input rise and fall time: $\leq 20\text{ns}$
- Reference level for measuring timing: 0.8V and 2V



■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

HN27512G

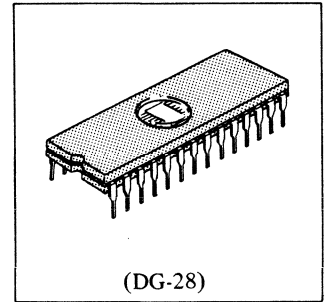
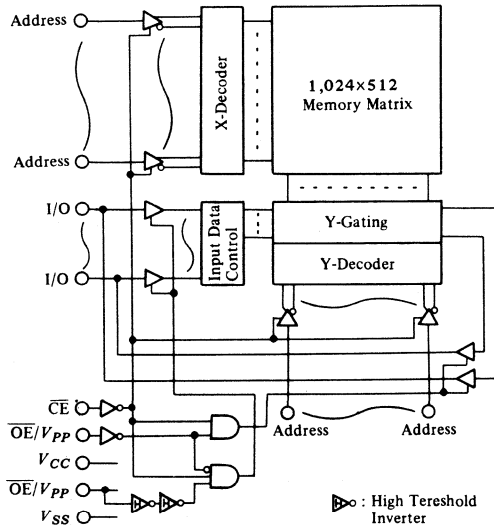
65536-word × 8-bit UV Erasable and Programmable Read Only Memory

The HN27512G is a 65536-word by 8-bit erasable and electrically programmable ROM. This device is packaged in a 28-pin, dual-in-line package with transparent window. The transparent window allows the user to expose the chip to ultraviolet light to erase the bit pattern, whereby a new pattern can then be written into the device.

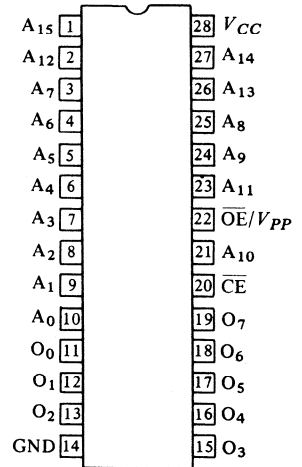
■ FEATURES

- Single Power Supply +5V ±5%
- High Performance Program Voltage: +12.5V D.C.
High Performance Programming Operations
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time HN27512G-25: 250ns (max.)
HN27512G-30: 300ns (max.)
- Absolute Max. Rating of 14.0V (max.)
V_{pp} pin
- Low Stand-by Current 40mA (max.)
- Device Identifier Mode Manufacturer Code and Device Code
- Compatible with Intel 27512

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode \ Pins	\overline{CE} (20)	\overline{OE}/V_{PP} (22)	A9 (24)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	Code

Note) X . . . Don't care
 V_H : 12.0V \pm 0.5V.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	$^{\circ}\text{C}$
Storage Temperature Range	T_{stg}	-65 to +125	$^{\circ}\text{C}$
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	$^{\circ}\text{C}$
All Input and Output Voltages*	V_{IN}, V_{out}	-0.6 to +7	V
Voltage on Pin 24 (A9)	V_{ID}	-0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND

■ READ OPERATION

● DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to +70 $^{\circ}\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25\text{V}$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25\text{V}/0.45\text{V}$	-	-	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}$	-	-	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE} = \overline{OE} = V_{IL}$	-	45	100	mA
Input Low voltage	V_{IL}		-0.1*	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1^{**}$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{mA}$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	-	-	V

*: DC, -0.6V AC 20ns. **: DC, $V_{CC} + 1.5\text{V}$ AC 20ns.

** : Mode selection is unfixed between $V_{IH} = V_{CC} + 1\text{V}$ and $V_{IH} = 11.5\text{V}$.

AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

Parameter	Symbol	Test Condition	HN27512G-25		HN27512G-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	–	250	–	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	–	250	–	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	–	100	–	120	ns
\overline{OE} High Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

SWITCHING CHARACTERISTICS

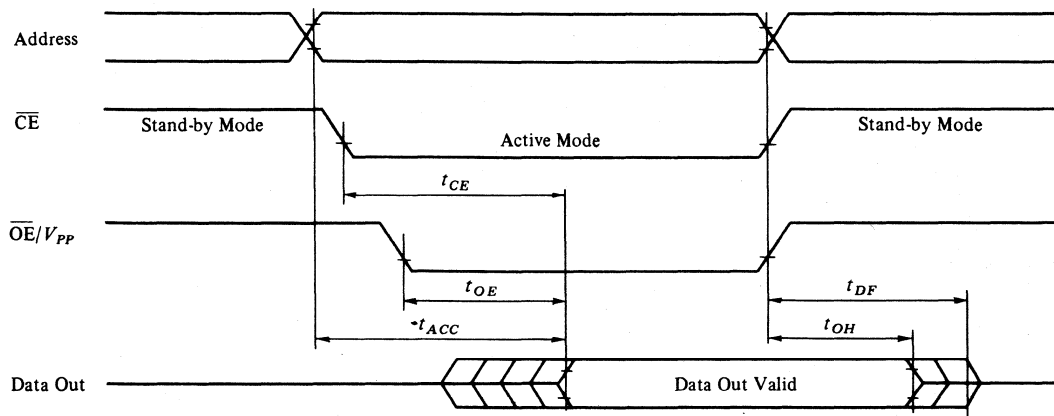
Test Condition

Input Pulse Levels: 0.45V to 2.4V

Input Rise and Fall Time: $\leq 20\text{ns}$

Output Load: 1 TTL Gate +100pF

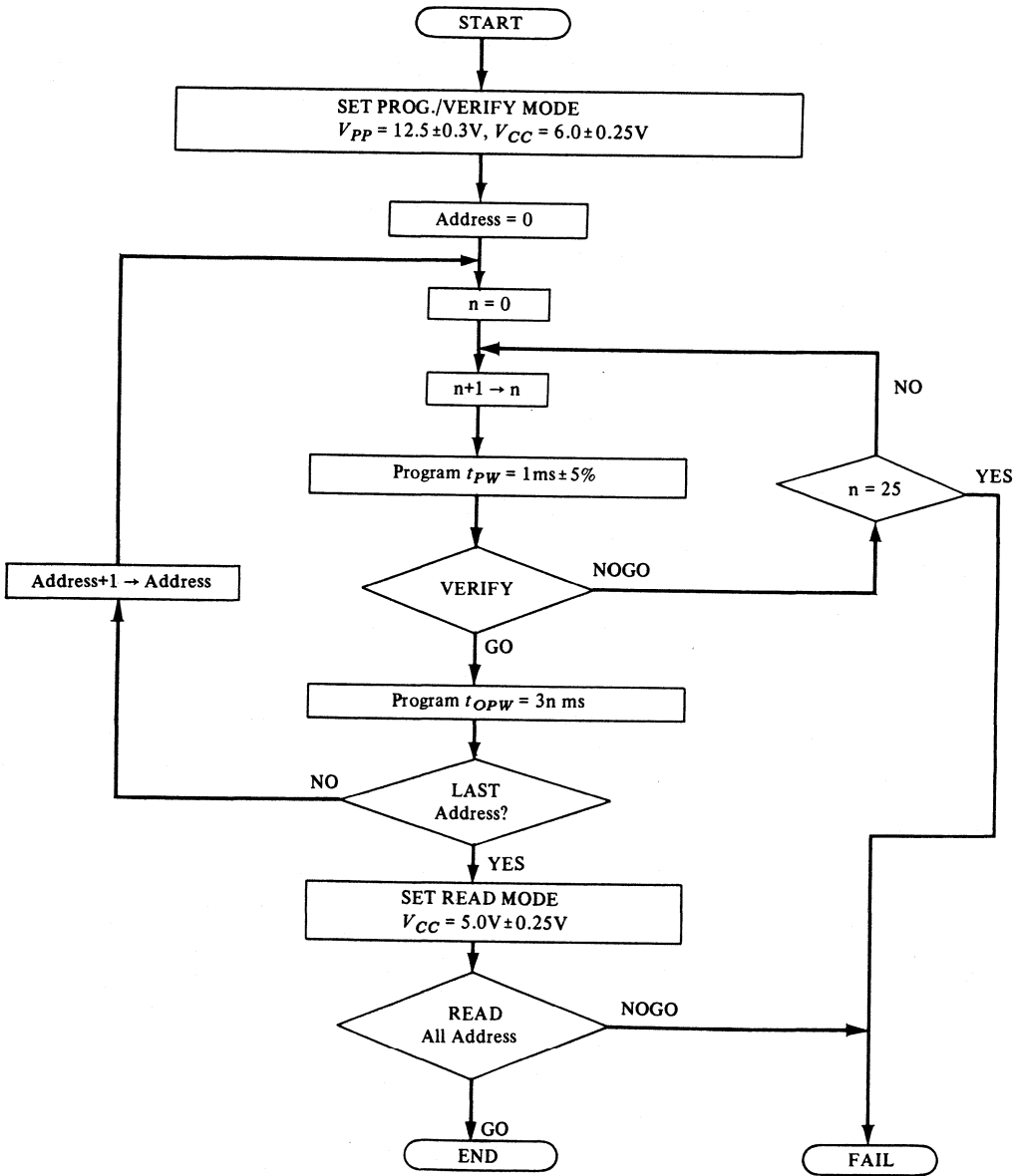
Reference Level for Measuring Timing: 0.8V and 2.0V


CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance (except \overline{OE}/V_{PP})	C_{in1}	$V_{in} = 0\text{V}$	–	4	6	pF
\overline{OE}/V_{PP} Pin	C_{in2}	$V_{in} = 0\text{V}$	–	12	20	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

● HN27512G SERIES IDENTIFIER CODE

Pins	A ₀ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	Hex Data
Identifier	V _{IL}	0	0	0	0	0	1	1	1	07
Manufacturer Code	V _{IH}	1	0	0	1	0	1	0	0	94

Notes: 1. A₉ = 12.0 ± 0.5V.
2. A_{1~8}, A_{10~15}, \overline{CE} , $\overline{OE}/V_{PP} = V_{IL}$.

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V _{OL}	I _{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V _{OH}	I _{OH} = –400μA	2.4	–	–	V
V _{CC} Current (Active)	I _{CC2}		–	–	100	mA
Input Low Level	V _{IL}		–0.1*	–	0.8	V
Input High Level	V _{IH}		2.0	–	V _{CC} **	V
V _{PP} Supply Current	I _{PP}	$\overline{CE} = V_{IL}$	–	–	50	mA

*: DC, –0.6V AC 20ns. **: DC, V_{CC} + 0.5V AC 20ns.
**: Mode Selection is unfixed between V_{IH} = V_{CC} and V_{IH} = 11.5V.

● AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t _{AS}		2	–	–	μs
Data Setup Time	t _{DS}		2	–	–	μs
Address Hold Time	t _{AH}		0	–	–	μs
Data Hold Time	t _{DH}		2	–	–	μs
\overline{OE} Hold Time	t _{OEH}		2	–	–	μs
\overline{CE} to Output Float Delay	t _{DF}		0	–	130	ns
V _{PP} Setup Time	t _{VPS}		2	–	–	μs
V _{CC} Setup Time	t _{VCS}		2	–	–	μs
\overline{CE} Pulse Width During Initial Programming	t _{PW}		0.95	1.0	1.05	ms
\overline{CE} Pulse Width During Overprogramming	t _{OPW}		2.85	–	78.75	ms
V _{PP} Recovery Time	t _{VR}		2	–	–	μs
Data Valid from \overline{CE}	t _{DV}		–	–	1	μs

Notes: t_{OPW} is defined as mentioned in flow chart.
t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

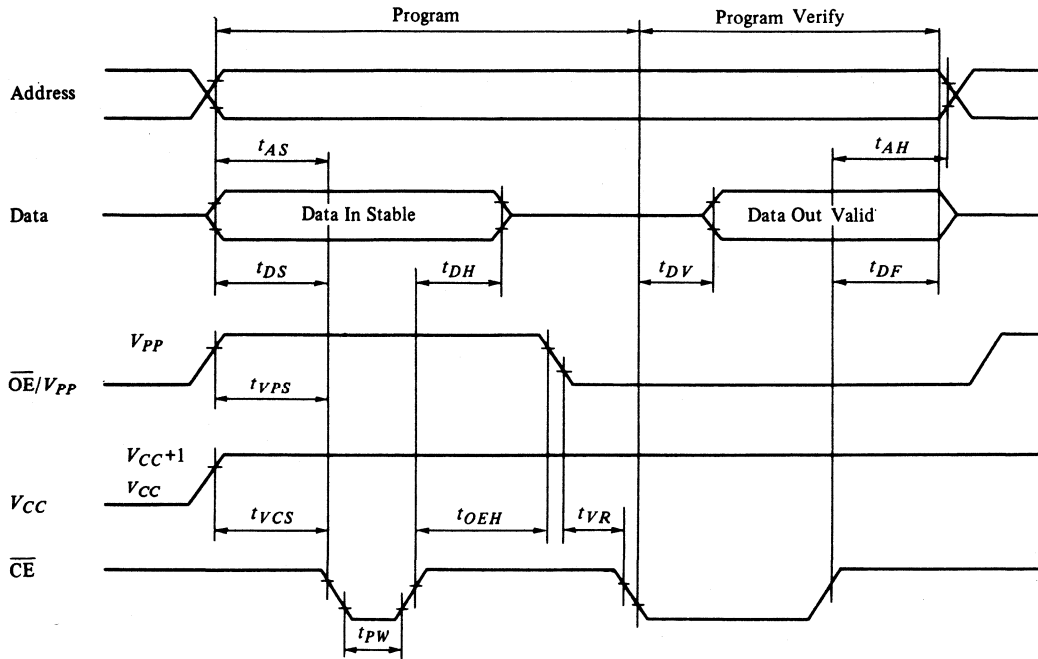
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level: 0.45V to 2.4V

Input Rise and Fall Time: $\leq 20\text{ns}$

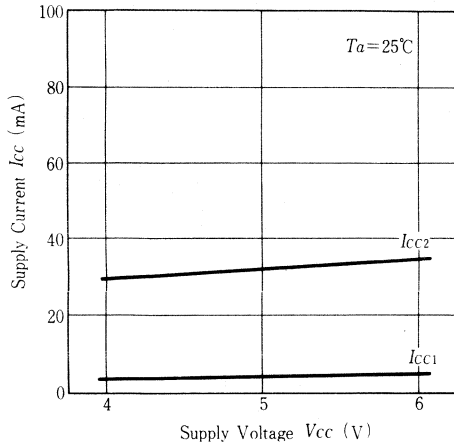
Reference Level for Measuring Timing: 0.8V and 2.0V



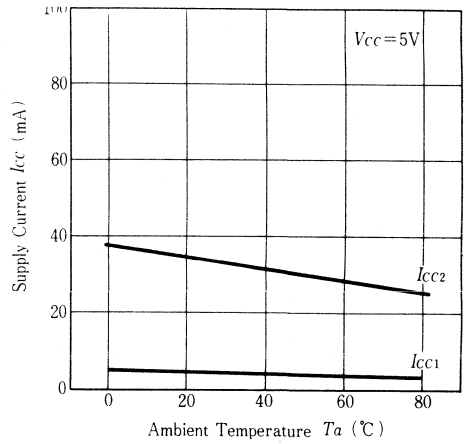
■ ERASE

Erasure of HN27512G is performed by exposure to ultraviolet light of 2537\AA and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15 W. sec/cm^2 .

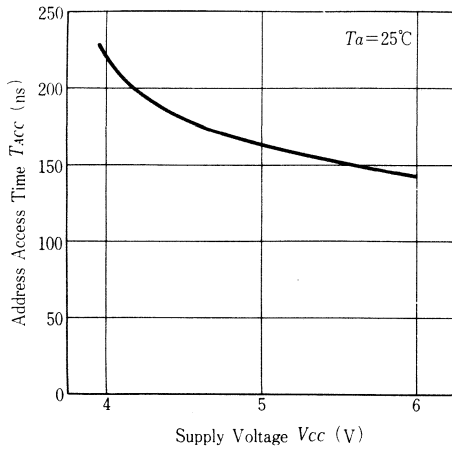
SUPPLY CURRENT VS. SUPPLY VOLTAGE



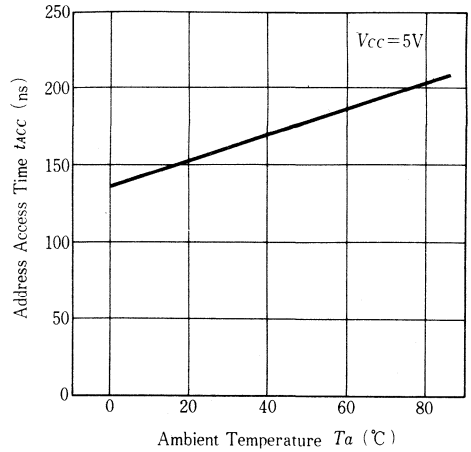
SUPPLY CURRENT VS. AMBIENT TEMPERATURE



ADDRESS ACCESS TIME VS. VOLTAGE



ADDRESS ACCESS TIME VS. AMBIENT TEMPERATURE

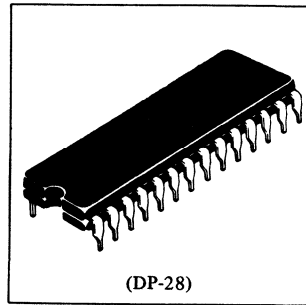


65536-word x 8-bit One Time Electrically Programmable Read Only Memory

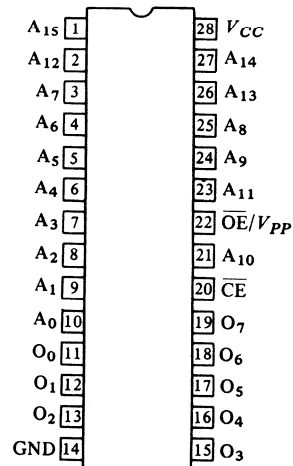
The HN27512P is a 65536-word by 8-bit one time electrically programmable ROM. Initially, all bits of the HN27512P are in the "1" state (Output High). Data is introduced by selectively programming "0" into the desired bit locations. This device is packaged in a 28 pin, plastic dual-in-line package. Therefore, this device can not be re-written.

■ FEATURES

- Single Power Supply +5V ±5%
- High Performance Program Voltage: +12.5V D.C.
High Performance Programming Operations
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time HN27512P-25: 250ns (max.)
HN27512P-30: 300ns (max.)
- Absolute Max. Rating of 14.0V (max.)
V_{pp} pin
- Low Stand-by Current 40mA (max.)
- Device Identifier Mode Manufacturer Code and Device Code.

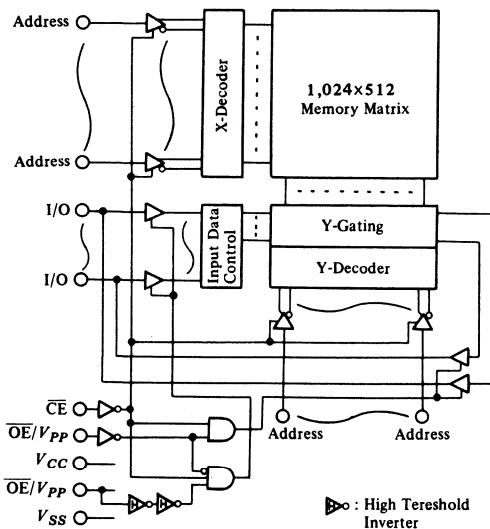


■ PIN ARRANGEMENT



(Top View)

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

MODE SELECTION

Pins	CE (20)	OE/ V_{PP} (22)	A9 (24)	V_{CC} (28)	Outputs (11 ~ 13, 15 ~ 19)
Mode					
Read	V_{IL}	V_{IL}	X	V_{CC}	Dout
Output Disable	V_{IL}	V_{IH}	X	V_{CC}	High Z
Standby	V_{IH}	X	X	V_{CC}	High Z
High Performance Program	V_{IL}	V_{PP}	X	V_{CC}	Din
Program Verify	V_{IL}	V_{IL}	X	V_{CC}	Dout
Program Inhibit	V_{IH}	V_{PP}	X	V_{CC}	High Z
Identifier	V_{IL}	V_{IL}	V_H	V_{CC}	Code

Note) X . . . Don't care
 V_H : 12.0V \pm 0.5V.

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Operating Temperature Range	T_{opr}	0 to +70	$^{\circ}$ C
Storage Temperature Range	T_{stg}	-55 to +125	$^{\circ}$ C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	$^{\circ}$ C
All Input and Output Voltages*	V_{IN} , V_{out}	-0.6 to +7	V
Voltage on Pin 24 (A9)	V_{ID}	-0.6 to +13.5	V
V_{PP} Voltage*	V_{PP}	-0.6 to +14.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7	V

* with respect to GND

READ OPERATION

DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to +70 $^{\circ}$ C, $V_{CC} = 5V \pm 5\%$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{IN} = 5.25V$	-	-	10	μ A
Output Leakage Current	I_{LO}	$V_{out} = 5.25/0.45V$	-	-	10	μ A
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}$	-	-	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE} = \overline{OE} = V_{IL}$	-	45	100	mA
Input Low voltage	V_{IL}		-0.1*	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC}+1$ **	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4	-	-	V

*: DC, -0.6V AC 20ns. **: DC, $V_{CC} + 1.5V$ AC 20ns.

** : Mode selection is unfixed between $V_{IH} = V_{CC} + 1V$ and $V_{IH} = 11.5V$.

● AC CHARACTERISTICS ($T_a = 0$ to $+70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 5\%$)

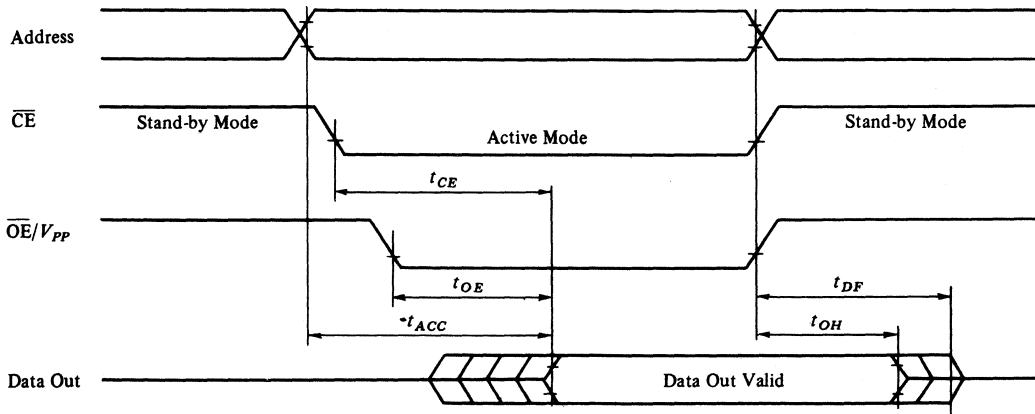
Parameter	Symbol	Test Condition	HN27512P-25		HN27512P-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	–	250	–	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	–	250	–	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	–	100	–	120	ns
\overline{OE} High Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	60	0	105	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	–	0	–	ns

Note: t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Levels: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Output Load: 1 TTL Gate +100pF
 Reference Level for Measuring Timing: 0.8V and 2.0V

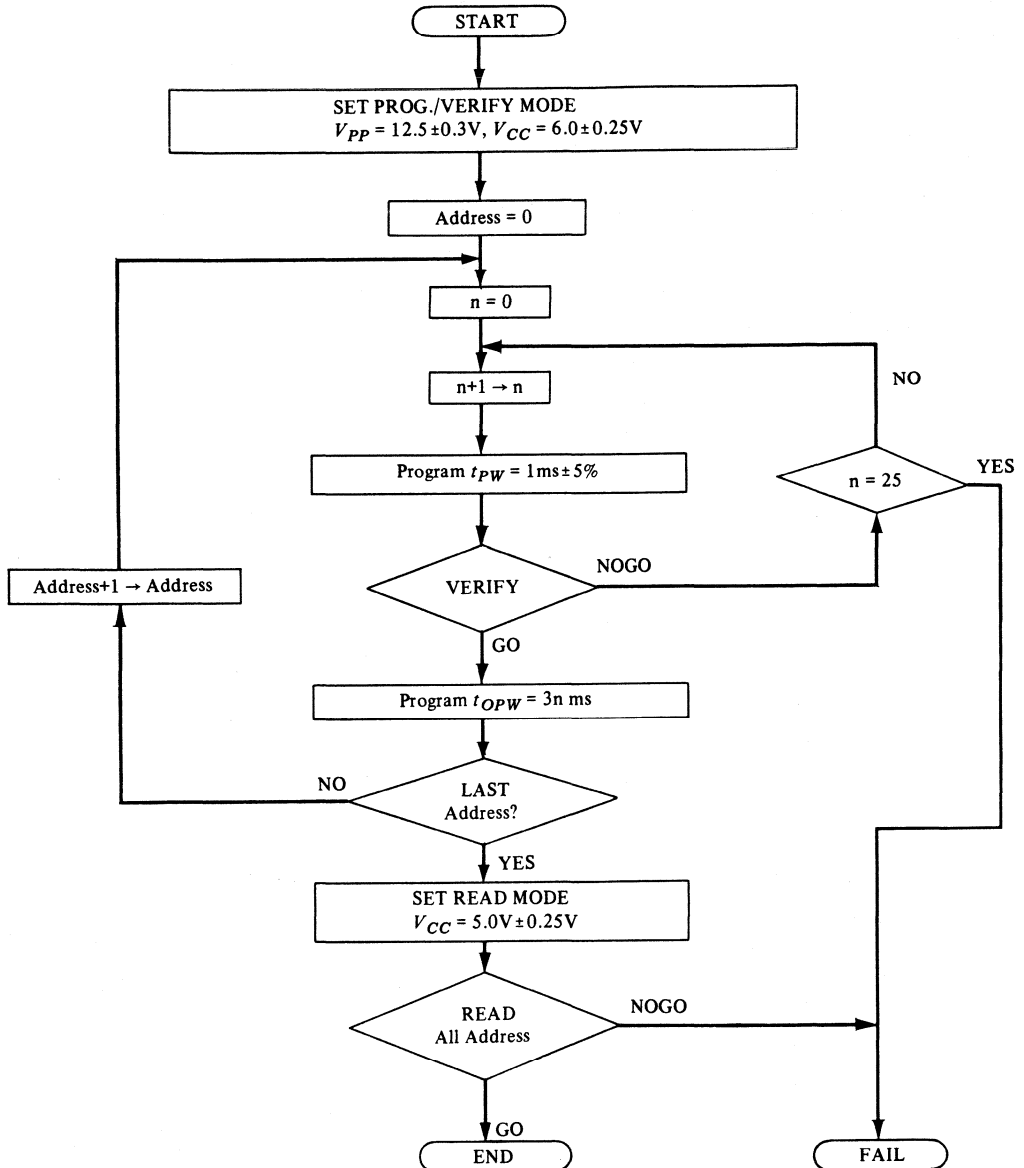


● CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance (except \overline{OE}/V_{PP})	C_{in1}	$V_{in} = 0\text{V}$	–	4	6	pF
\overline{OE}/V_{PP} Pin	C_{in2}	$V_{in} = 0\text{V}$	–	12	20	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	–	8	12	pF

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm show in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High performance Programming Flowchart

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes that identify manufacturer and type of device, from outputs of EPROM. By this Mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

● HN27512P SERIES IDENTIFIER CODE

Identifier \ Pins	A ₉ (10)	O ₇ (19)	O ₆ (18)	O ₅ (17)	O ₄ (16)	O ₃ (15)	O ₂ (13)	O ₁ (12)	O ₀ (11)	Hex Data
Manufacturer Code	V _{IL}	0	0	0	0	0	1	1	1	07
Device Code	V _{IH}	1	0	0	1	0	1	0	0	94

Notes: 1. A₉ = 12.0V ± 0.5V.
 2. A_{1~8}, A_{10~15}, \overline{CE} , \overline{OE}/V_{PP} = V_{IL}.

■ HIGH PERFORMANCE PROGRAMMING OPERATION

● DC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I _{LI}	V _{IN} = 5.25V	–	–	10	μA
Output Low Voltage During Verify	V _{OL}	I _{OL} = 2.1mA	–	–	0.45	V
Output High Voltage During Verify	V _{OH}	I _{OH} = –400μA	2.4	–	–	V
V _{CC} Current (Active)	I _{CC2}		–	–	100	mA
Input Low Level	V _{IL}		–0.1*	–	0.8	V
Input High Level	V _{IH}		2.0	–	V _{CC} **	V
V _{PP} Supply Current	I _{PP}	$\overline{CE} = V_{IL}$	–	–	50	mA

*: DC, –0.6V AC 20ns. **: DC, V_{CC} + 0.5V AC 20ns.
 **: Mode selection is unfixed between V_{CC} and V_{IH} = 11.5V.

● AC PROGRAMMING CHARACTERISTICS (T_a = 25°C ± 5°C, V_{CC} = 6V ± 0.25V, V_{PP} = 12.5V ± 0.3V)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Address Setup Time	t _{AS}		2	–	–	μs
Data Setup Time	t _{DS}		2	–	–	μs
Address Hold Time	t _{AH}		0	–	–	μs
Data Hold Time	t _{DH}		2	–	–	μs
\overline{OE} Hold Time	t _{OEH}		2	–	–	μs
\overline{CE} to Output Float Delay	t _{DF}		0	–	130	ns
V _{PP} Setup Time	t _{VPS}		2	–	–	μs
V _{CC} Setup Time	t _{VCS}		2	–	–	μs
\overline{CE} Pulse Width During Initial Programming	t _{PW}		0.95	1.0	1.05	ms
\overline{CE} Pulse Width During Overprogramming	t _{OPW}		2.85	–	78.75	ms
V _{PP} Recovery Time	t _{VR}		2	–	–	μs
Data Valid from \overline{CE}	t _{DV}		–	–	1	μs

Notes: t_{OPW} is defined as mentioned in flow chart.
 t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

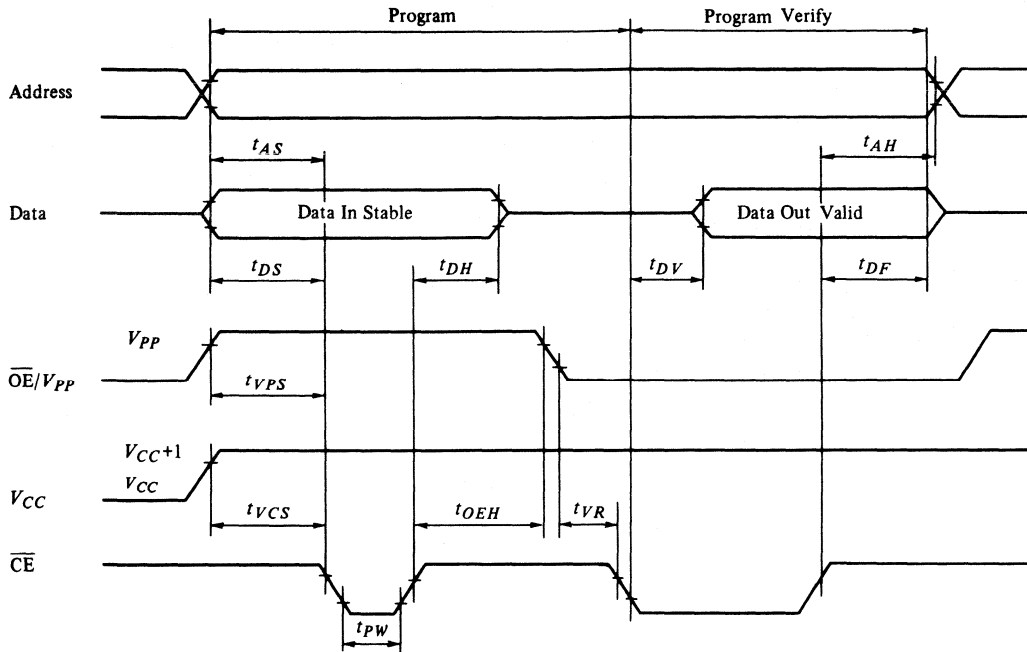
● SWITCHING CHARACTERISTICS

Test Condition

Input Pulse Level: 0.45V to 2.4V

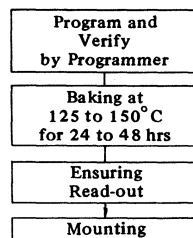
Input Rise and Fall Time: $\leq 20\text{ns}$

Reference Level for Measuring Timing: 0.8V and 2.0V



■ RECOMMENDED SCREENING CONDITIONS

Before mounting, please make the screening (baking without bias) shown in the right.



Recommended Screening conditions

HN27C1024G Series —Under Development

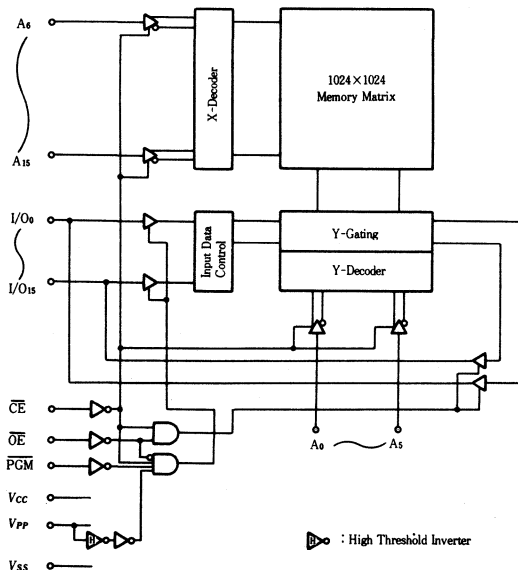
65536-word × 16-bit CMOS UV Erasable and Programmable ROM

The HN27C1024G is a 65536 word by 16-bit erasable and electrically programmable ROM. This device is packaged in a 40-pin, dual-in-line package with transparent lid. The transparent lid allows the memory content to be erased with ultraviolet light, whereby a new pattern can then be written into the device.

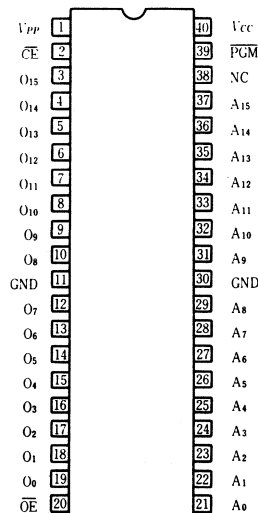
■ FEATURES

- Single Power Supply: +5V ± 5%
- High Performance Program Mode and High Performance Word Program Mode
 - Program Voltage: +12.5V DC
 - High Performance Programming Available
- Static: No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program
- Access Time: 150ns max. (HN27C1024G-15)
200ns max. (HN27C1024G-20)
- Low power Dissipation: 50mW/MHz typ. (Active Mode)
5μw typ. (Stand-by Mode)

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



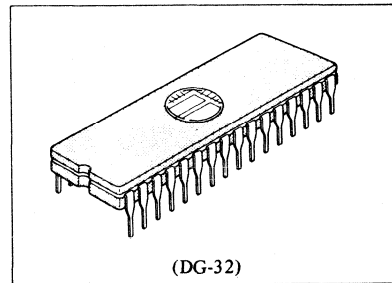
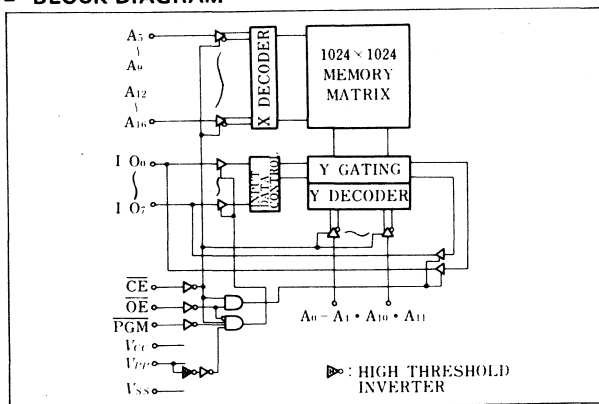
(Top View)

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

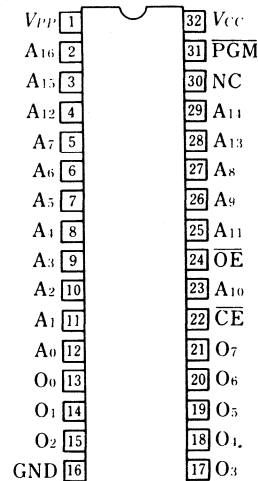
■ FEATURES

- Single Power Supply +5V ±5%
- High Performance Program Mode and High Performance Page Program Mode Program Voltage: +12.5V DC High Performance Programming Available
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time 200ns max. (HN27C101G-20)
250ns max. (HN27C101G-25)
- Low power Dissipation . . . 50mW/MHz typ. (Active Mode)
5μW typ. (Standby Mode)
- Pin Arrangement 32 Pin JEDEC Standard
- Device Identifier Maker code and Device code

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode	Pins	CE (22)	OE (24)	PGM (31)	A9 (26)	V _{PP} (1)	V _{CC} (32)	Outputs (13~15, 17~21)
Read		V _{IL}	V _{IL}	V _{IH}	X	V _{CC}	V _{CC}	Dout
Output Disable		V _{IL}	V _{IH}	V _{IH}	X	V _{CC}	V _{CC}	High Z
Standby		V _{IH}	X	X	X	V _{CC}	V _{CC}	High Z
Program		V _{IL}	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	Din
Program Verify		V _{IL}	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	Dout
Page Data Latch		V _{IH}	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	Din
Page Program		V _{IH}	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	High Z
Program Inhibit		V _{IL}	V _{IL}	V _{IL}	X	V _{PP}	V _{CC}	High Z
		V _{IL}	V _{IH}	V _{IH}				
		V _{IH}	V _{IL}	V _{IL}				
		V _{IH}	V _{IH}	V _{IH}				
Identifier		V _{IL}	V _{IL}	V _{IH}	V _H	V _{CC}	V _{CC}	Code

Note) X: Don't care

* 30 pin should be connected to 32 pin.

V_H: 12.0V±0.5V

Note)

The specifications of this device are subject to change without notice. Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*	V_{in}, V_{out}	-1.0** to +7.0	V
V_{PP} Voltage*	V_{PP}	-0.6 to +13.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7.0	V
Voltage on Pin 26 (A9)*	V_{ID}	-0.6 to +13.5	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	°C

* with respect to GND ** Pulse Width: 50ns, DC: V_{IL} min = -0.6V

■ READ OPERATION

● DC CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{in} = 5.25V$	-	-	2	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25V/0.45V$	-	-	2	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.5V$	-	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE} = V_{IH}$	-	-	1	mA
	I_{SB2}	$\overline{CE} = V_{CC} \pm 0.3V$	-	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE} = V_{IL}, I_{out} = 0mA$	-	-	30	mA
	I_{CC2}	$f = 5MHz, I_{out} = 0mA$	-	-	30	mA
	I_{CC3}	$f = 1MHz, I_{out} = 0mA$	-	-	15	mA
Input Low Voltage	V_{IL}		-1.0*	-	0.8	V
Input High Voltage	V_{IH}^{**}		2.2	-	$V_{CC} + 1$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4	-	-	V

* Pulse Width: 50ns, DC: V_{IL} min = -0.3V ** Mode may be unfixed: $V_{IH} = V_{CC} + 1 \sim 11.5V$

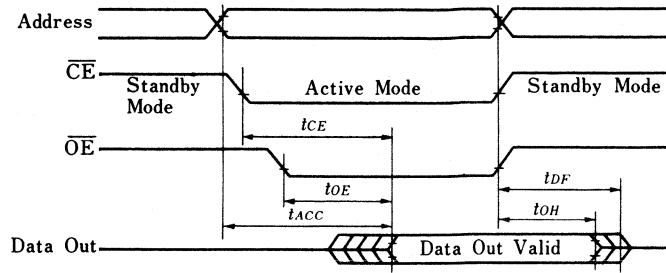
● AC CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	HN27C101G-20		HN27C101G-25		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	-	250	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	-	200	-	250	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	10	70	10	100	ns
\overline{OE} High to Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	-	ns

Note) t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

- Test Condition Input Pulse Levels: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20ns$
 Output Load: 1 TTL Gate + 100pF
 Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
 Outputs; 0.8V and 2.0V



● CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	-	10	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	-	-	15	pF

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes, that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

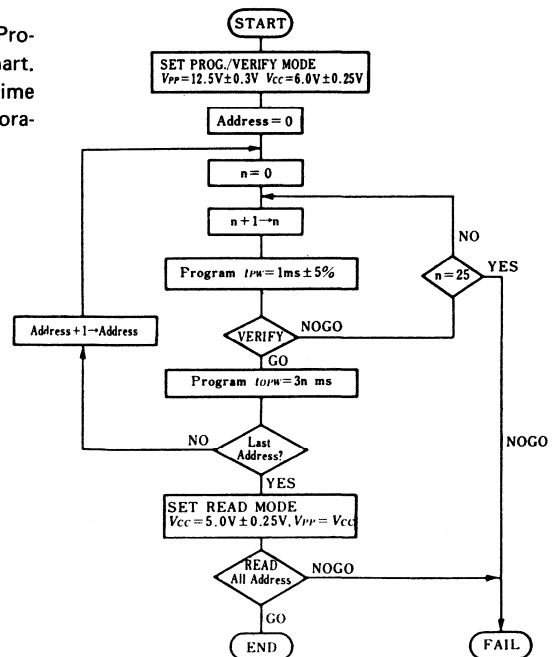
● HN27C101 IDENTIFIER CODES

Identifier	Pins	A0 (12)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	1	1	1	07
Device Code	V_{IH}	0	0	1	1	1	0	0	0	0	38

Notes: 1. $A_9 = 12.0\text{V} \pm 0.5\text{V}$
 2. $A_1 \sim A_8, A_{10} \sim A_{16}, \overline{CE}, \overline{OE} = V_{IL}, \overline{PGM} = V_{IH}$

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS ($T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=12.5\text{V} \pm 0.3\text{V}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{in} = 6.25\text{V}/0.45\text{V}$	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		-0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}} = \overline{\text{PGM}} = V_{IL}$	–	–	40	mA

Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .

2. V_{PP} must not exceed 13V including overshoot.

3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}=12.5\text{V}$.

4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{\text{CE}} = \text{Low}$.

● AC PROGRAMMING CHARACTERISTICS

($T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=12.5\text{V} \pm 0.3\text{V}$)

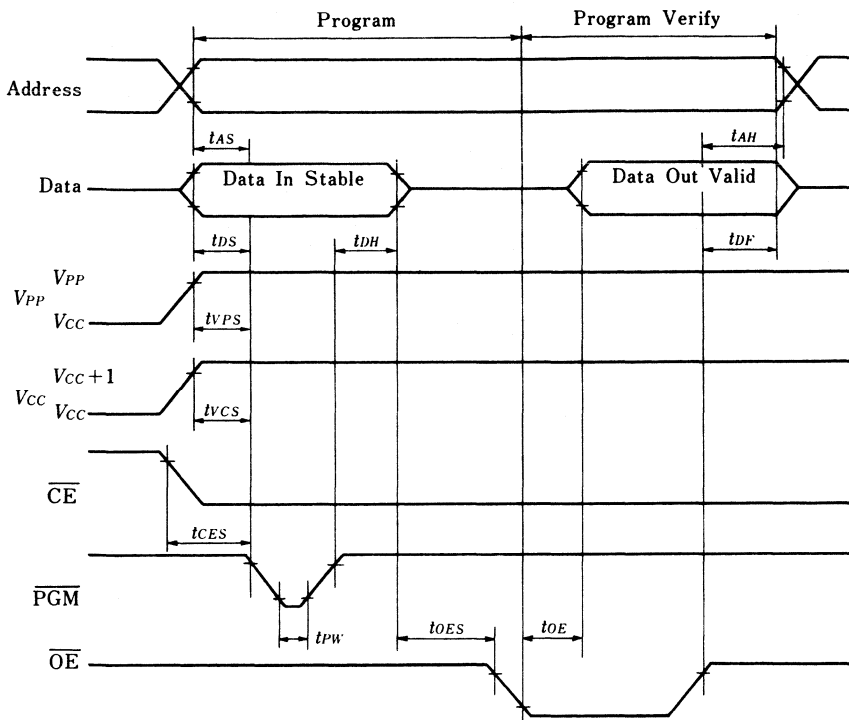
Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{\text{OE}}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}^*		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
PGM Pulse Width during Initial Programming	t_{PW}		0.95	1.0	1.05	ms
PGM Pulse Width during Overprogramming	t_{OPW}^{**}		2.85	–	78.75	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		0	–	150	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

** t_{OPW} is defined as mentioned in flowchart.

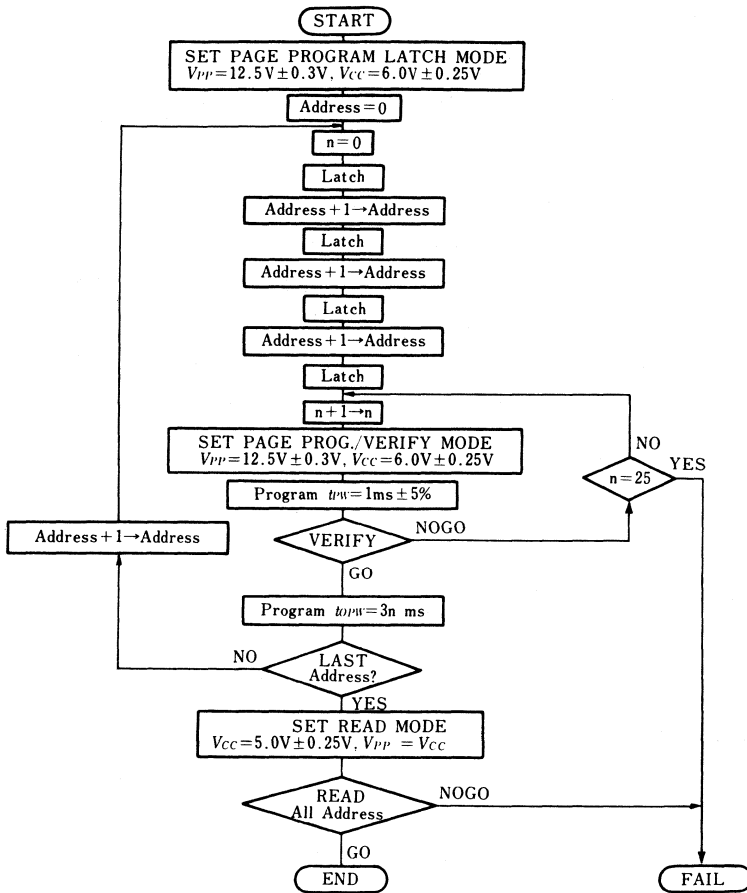
SWITCHING CHARACTERISTICS

Input Pulse Levels:	0.45V to 2.4V
Input Rise and Fall Time:	$\leq 20\text{ns}$
Reference Levels for Measurement	Inputs; 0.8V and 2.0V
Timing:	Outputs; 0.8V and 2.0V



HIGH PERFORMANCE PAGE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

• DC PROGRAMMING CHARACTERISTICS ($T_a=25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=12.5\text{V} \pm 0.3\text{V}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{in} = 6.25\text{V}/0.45\text{V}$	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		-0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}}=\text{OE}=V_{IH}$, $\text{PGM}=V_{IL}$	–	–	50	mA

- Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 2. V_{PP} must not exceed 13V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}=12.5\text{V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{\text{CE}}=\text{Low}$.

● **AC PROGRAMMING CHARACTERISTICS**

($T_a=25^{\circ}\text{C} \pm 5^{\circ}\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=12.5\text{V} \pm 0.3\text{V}$)

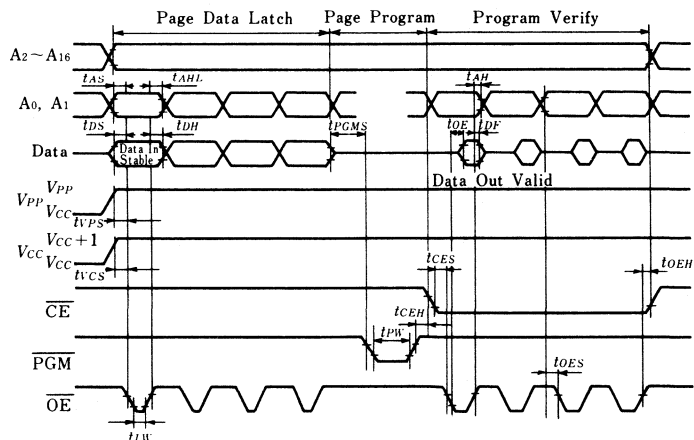
Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	—	—	μs
OE Setup Time	t_{OES}		2	—	—	μs
Data Setup Time	t_{DS}		2	—	—	μs
Adress Hold Time	t_{AH}		0	—	—	μs
	t_{AHL}		2	—	—	μs
Data Hold Time	t_{DH}		2	—	—	μs
OE to Output Float Delay	t_{DF*}		0	—	130	ns
V_{PP} Setup Time	t_{VPS}		2	—	—	μs
V_{CC} Setup Time	t_{VCS}		2	—	—	μs
PGM Pulse Width during Initial Programming	t_{PW}		0.95	1.0	1.05	ms
PGM Pulse Width during Overprogramming	t_{OPW**}		2.85	—	78.75	ms
CE Setup Time	t_{CES}		2	—	—	μs
Data Valid from OE	t_{OE}		0	—	150	ns
OE Pulse Width during Data Latch	t_{LW}		1	—	—	μs
PGM Setup Time	t_{PGMS}		2	—	—	μs
CE Hold Time	t_{CEH}		2	—	—	μs
OE Hold Time	t_{OEH}		2	—	—	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

** t_{OPW} is defined as mentioned in flowchart.

● **SWITCHING CHARACTERISTICS**

- **Test Condition** Input Pulse Levels: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
 Outputs; 0.8V and 2.0V



■ **ERASE**

Erase of HN27C101G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm²

HN27C301G Series

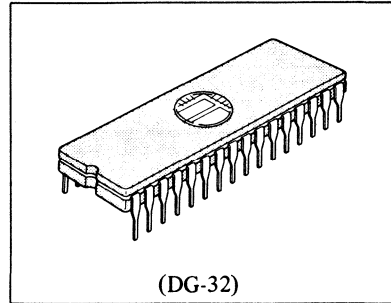
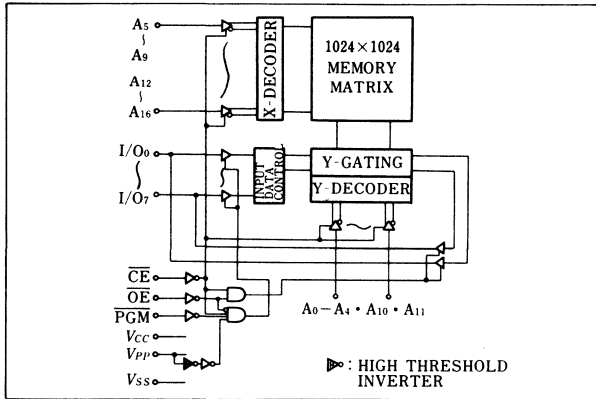
Preliminary

131072-word X 8-bit CMOS U.V. Erasable and Programmable ROM

■ FEATURES

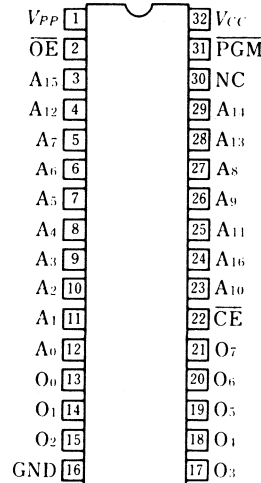
- Single Power Supply +5V ±5%
- High Performance Program Mode and High Performance Page Program Mode Program Voltage: +12.5V DC High Performance Programming Available
- Static No Clocks Required
- Inputs and Outputs TTL Compatible During Both Read and Program Modes
- Access Time 200ns max. (HN27C301G-20)
250ns max. (HN27C301G-25)
- Low power Dissipation . . . 50mW/MHz typ. (Active Mode)
5μW typ. (Standby Mode)
- Pin Compatible with 1Mbit MASK ROM (28pin type)
- Device identifier Mode Maker Code and Device code

■ BLOCK DIAGRAM



(DG-32)

■ PIN ARRANGEMENT



(Top View)

■ MODE SELECTION

Mode	Pins	CE (22)	OE (2)	PGM (31)	A9	V _{PP} (1)	V _{CC} (32, 30)*	Outputs (13~15, 17~21)
Read		V _{IL}	V _{IL}	V _{IH}	X	V _{CC}	V _{CC}	Dout
Output Disable		V _{IL}	V _{IH}	V _{IH}	X	V _{CC}	V _{CC}	High Z
Standby		V _{IH}	X	X	X	V _{CC}	V _{CC}	High Z
Program		V _{IL}	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	Din
Program Verify		V _{IL}	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	Dout
Page Data Latch		V _{IH}	V _{IL}	V _{IH}	X	V _{PP}	V _{CC}	Din
Page Program		V _{IH}	V _{IH}	V _{IL}	X	V _{PP}	V _{CC}	High Z
Program Inhibit		V _{IL}	V _{IL}	V _{IL}	X	V _{PP}	V _{CC}	High Z
		V _{IL}	V _{IH}	V _{IH}				
		V _{IH}	V _{IL}	V _{IL}				
		V _{IH}	V _{IH}	V _{IH}				
Identifier		V _{IL}	V _{IL}	V _{IH}	V _H	V _{CC}	V _{CC}	Code

Note) X: Don't care

* 30 pin should be connected to 32 pin.

V_H: 12.0V±0.5V

Note)

The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
All Input and Output Voltages*	V_{in}, V_{out}	-1.0** to +7.0	V
V_{PP} Voltage*	V_{PP}	-0.6 to +13.0	V
V_{CC} Voltage*	V_{CC}	-0.6 to +7.0	V
Voltage on Pin 26 (A9)*	V_{ID}	-0.6~+13.5	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-65 to +125	°C
Storage Temperature Range Under Bias	T_{bias}	-10 to +80	°C

* with respect to GND ** Pulse Width: 50ns, DC: V_{IL} min = -0.6V

■ READ OPERATION

● DC CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{in} = 5.25V$	-	-	2	μA
Output Leakage Current	I_{LO}	$V_{out} = 5.25V/0.45V$	-	-	2	μA
V_{PP} Current	I_{PP1}	$V_{PP} = 5.5V$	-	1	20	μA
V_{CC} Current	I_{SB1}	$\overline{CE} = V_{IH}$	-	-	1	mA
	I_{SB2}	$\overline{CE} = V_{CC} \pm 0.3V$	-	1	20	μA
V_{CC} Current	I_{CC1}	$\overline{CE} = V_{IL}, I_{out} = 0mA$	-	-	30	mA
	I_{CC2}	$f = 5MHz, I_{out} = 0mA$	-	-	30	mA
	I_{CC3}	$f = 1MHz, I_{out} = 0mA$	-	-	15	mA
Input Low Voltage	V_{IL}		-1.0*	-	0.8	V
Input High Voltage	V_{IH}^{**}		2.2	-	$V_{CC} + 1$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.45	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4	-	-	V

* Pulse Width: 50ns, DC: V_{IL} min = -0.3V ** Mode may be unfixed: $V_{IH} = V_{CC} + 1 \sim 11.5V$

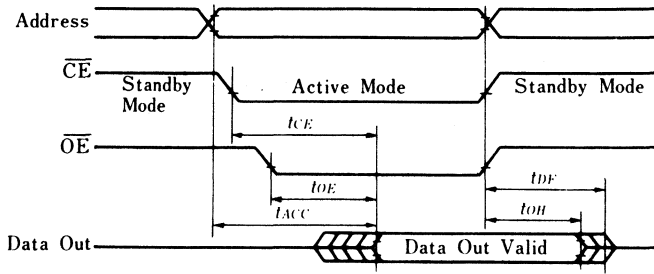
● AC CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 5\%$, $V_{PP} = V_{CC}$)

Parameter	Symbol	Test Conditions	HN27C301G-20		HN27C301G-25		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}$	-	200	-	250	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE} = V_{IL}$	-	200	-	250	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}$	10	70	10	100	ns
\overline{OE} High to Output Float	t_{DF}	$\overline{CE} = V_{IL}$	0	50	0	60	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}$	0	-	0	-	ns

Note) t_{DF} defines the time at which the Output achieves the open circuit condition and Data is no longer driven.

● SWITCHING CHARACTERISTICS

● Test Condition	Input Pulse Levels:	0.45V to 2.4V
	Input Rise and Fall Time:	$\leq 20ns$
	Output Load:	1 TTL Gate + 100pF
	Reference Levels for Measuring Timing:	Inputs: 0.8V and 2.0V
		Outputs: 0.8V and 2.0V



● CAPACITANCE ($T_a=25^\circ\text{C}$, $f=1\text{MHz}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	-	10	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	-	-	15	pF

■ DEVICE IDENTIFIER MODE

The Identifier Mode allows the reading out of binary codes, that identify manufacturer and type of device, from outputs of EPROM. By this mode, the device will be automatically matched its own corresponding programming algorithm, using programming equipment.

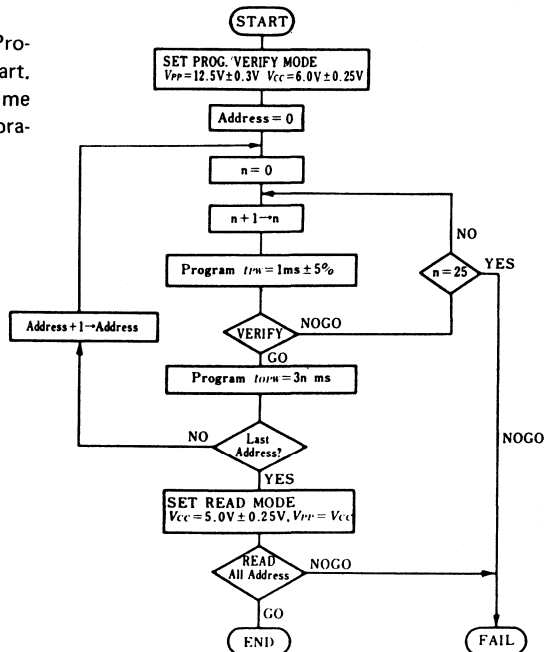
● HN27C301 IDENTIFIER CODES

Identifier	Pins	A0 (12)	O7 (21)	O6 (20)	O5 (19)	O4 (18)	O3 (17)	O2 (15)	O1 (14)	O0 (13)	Hex Data
Manufacturer Code	V_{IL}	0	0	0	0	0	0	1	1	1	O7
Device Code	V_{IH}	1	0	1	1	1	1	0	0	1	B9

Notes: 1. $A_9=12.0\text{V} \pm 0.5\text{V}$
 2. $A_1 \sim A_8, A_{10} \sim A_{16}, \overline{CE}, \overline{OE}=V_{IL}, \overline{PGM}=V_{IH}$

■ HIGH PERFORMANCE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Programming Flowchart

● DC PROGRAMMING CHARACTERISTICS ($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{In} = 6.25\text{V}/0.45\text{V}$	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	$I_{OL} = 2.1\text{mA}$	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	$I_{OH} = -400\mu\text{A}$	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		-0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}} = \text{PGM} = V_{IL}$	–	–	40	mA

- Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 2. V_{PP} must not exceed 13V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP} = 12.5\text{V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{\text{CE}} = \text{Low}$.

● AC PROGRAMMING CHARACTERISTICS

($T_a = 25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC} = 6\text{V} \pm 0.25\text{V}$, $V_{PP} = 12.5\text{V} \pm 0.3\text{V}$)

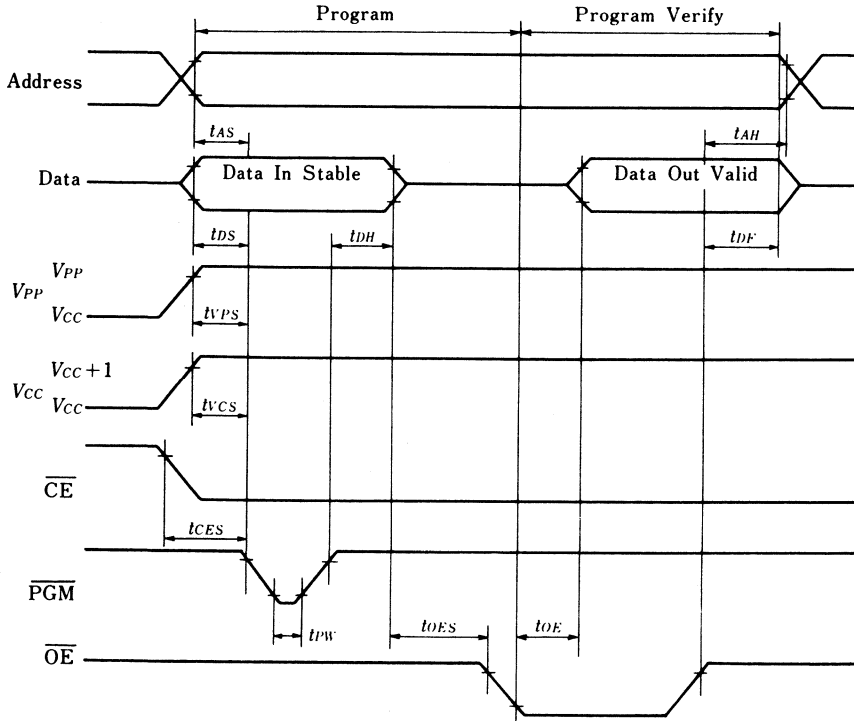
Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
$\overline{\text{OE}}$ Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}^*		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
PGM Pulse Width during Initial Programming	t_{PW}		0.95	1.0	1.05	ms
PGM Pulse Width during Overprogramming	t_{OPW}^{**}		2.85	–	78.75	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		0	–	150	ns

* t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

** t_{OPW} is defined as mentioned in flowchart.

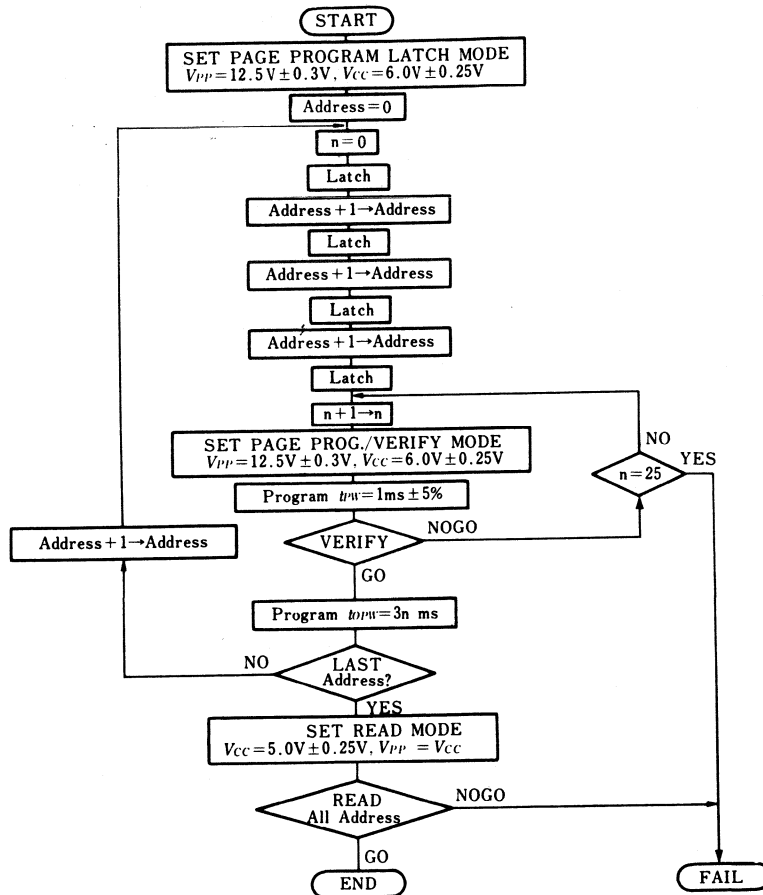
■ SWITCHING CHARACTERISTICS

Input Pulse Levels: 0.45V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Reference Levels for Measurement Inputs; 0.8V and 2.0V
 Outputs; 0.8V and 2.0V



■ HIGH PERFORMANCE PAGE PROGRAMMING

This device can be applied the High Performance Programming algorithm shown in following flowchart. This algorithm allows to obtain faster programming time without any voltage stress to the device nor deterioration in reliability of programmed data.



High Performance Page Programming Flowchart

● **DC PROGRAMMING CHARACTERISTICS** ($T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=12.5\text{V} \pm 0.3\text{V}$)

Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{in}=6.25\text{V}/0.45\text{V}$	–	–	2	μA
Output Low Voltage during Verify	V_{OL}	$I_{OL}=2.1\text{mA}$	–	–	0.45	V
Output High Voltage during Verify	V_{OH}	$I_{OH}=-400\mu\text{A}$	2.4	–	–	V
V_{CC} Current (Active)	I_{CC}		–	–	30	mA
Input Low Level	V_{IL}		-0.1	–	0.8	V
Input High Level	V_{IH}		2.2	–	V_{CC}	V
V_{PP} Supply Current	I_{PP}	$\overline{\text{CE}}=\overline{\text{OE}}=V_{IH}$, $\overline{\text{PGM}}=V_{IL}$	–	–	50	mA

- Notes) 1. V_{CC} must be applied before V_{PP} and removed after V_{PP} .
 2. V_{PP} must not exceed 13V including overshoot.
 3. An influence may be had upon device reliability if the device is installed or removed while $V_{PP}=12.5\text{V}$.
 4. Do not alter V_{PP} either V_{IL} to 12.5V or 12.5V to V_{IL} when $\overline{\text{CE}}=\text{Low}$.

● **AC PROGRAMMING CHARACTERISTICS (High Performance Page Programming)**

($T_a=25^\circ\text{C} \pm 5^\circ\text{C}$, $V_{CC}=6\text{V} \pm 0.25\text{V}$, $V_{PP}=12.5\text{V} \pm 0.3\text{V}$)

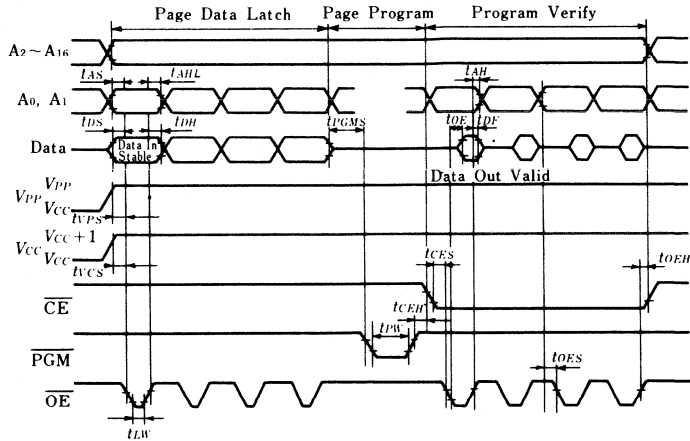
Parameter	Symbol	Test Conditions	min.	typ.	max.	Unit
Address Setup Time	t_{AS}		2	–	–	μs
OE Setup Time	t_{OES}		2	–	–	μs
Data Setup Time	t_{DS}		2	–	–	μs
Address Hold Time	t_{AH}		0	–	–	μs
	t_{AHL}		2	–	–	μs
Data Hold Time	t_{DH}		2	–	–	μs
$\overline{\text{OE}}$ to Output Float Delay	t_{DF}^*		0	–	130	ns
V_{PP} Setup Time	t_{VPS}		2	–	–	μs
V_{CC} Setup Time	t_{VCS}		2	–	–	μs
$\overline{\text{PGM}}$ Pulse Width during Initial Programming	t_{PW}		0.95	1.0	1.05	ms
$\overline{\text{PGM}}$ Pulse Width during Overprogramming	t_{OPW}^{**}		2.85	–	78.75	ms
$\overline{\text{CE}}$ Setup Time	t_{CES}		2	–	–	μs
Data Valid from $\overline{\text{OE}}$	t_{OE}		0	–	150	ns
$\overline{\text{OE}}$ Pulse Width during Data Latch	t_{LW}		1	–	–	μs
$\overline{\text{PGM}}$ Setup Time	t_{PGMS}		2	–	–	μs
$\overline{\text{CE}}$ Hold Time	t_{CEH}		2	–	–	μs
$\overline{\text{OE}}$ Hold Time	t_{OEH}		2	–	–	μs

* t_{DF} defines the time at which the output achieves the open circuit condition and data is no longer driven.

** t_{OPW} is defined as mentioned in flowchart.

● **SWITCHING CHARACTERISTICS**

- **Test Condition** Input Pulse Levels: 0.45V to 2.4V
- Input Rise and Fall Time: $\leq 20\text{ns}$
- Reference Levels for Measuring Timing: Inputs; 0.8V and 2.0V
- Outputs; 0.8V and 2.0V



■ **ERASE**

Erase of HN27C301G is performed by exposure to ultraviolet light of 2537 Å and all the output data are changed to "1" after this erasure procedure. The minimum integrated dose (i.e. UV intensity x exposure time) for erasure is 15W. sec/cm²

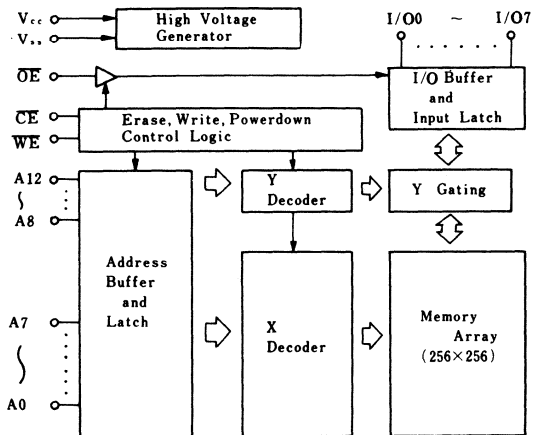
HN58064P Series

8192-word x 8-bit Electrically Erasable and Programmable ROM.

■ FEATURES

- Single 5V Supply
- Address, Data, \overline{CE} , \overline{OE} Latches
- Byte Erase / Byte Write Time. 10 ms typ.
- Chip Erase Time 20 ms typ.
- Fast Access Time. 250 ns max. / 300 ns max.
- Low Power Dissipation. 300 mW typ. (Active)
. 125 mW typ. (Standby)
- Comforms to JEDEC Byte-Wide Standard
- Reliable N-channel MNOS Technology
- 10000 Erase/Write Cycles

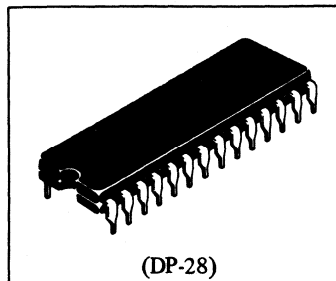
■ BLOCK DIAGRAM



■ MODE SELECTION

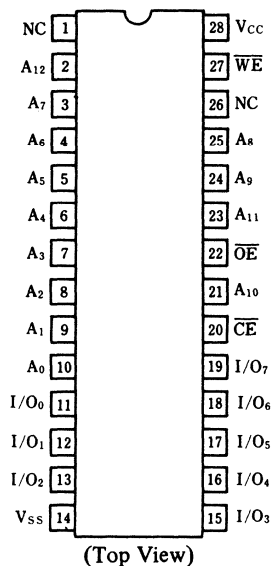
MODE	PINS			
	\overline{CE} (20)	\overline{OE} (22)	\overline{WE} (27)	I/O (11~13, 15~19)
Read	V_{IL}	V_{IL}	V_{IH}	Dout
Standby	V_{IH}	X	X	High Z
Byte Erase	V_{IL}	V_{IH}	V_{IL}	Din = V_{IH}
Byte Write	V_{IL}	V_{IH}	V_{IL}	Din
Chip Erase	V_{IL}	V_{IL}	V_{IL}	Din = V_{IH}
Deselect	V_{IL}	V_{IH}	V_{IH}	High Z

X: V_{IH} or V_{IL}



(DP-28)

■ PIN ARRANGEMENT



(Top View)

A0 ~ A12	Address Input
I/O0 ~ I/O7	Data in / Data out
\overline{OE}	Output Enable
\overline{CE}	Chip Enable
\overline{WE}	Write Enable
V_{cc}	Power (+5V)
V_{ss}	GND
NC	No connect

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.6 to +7.0	V
Input Voltage*	V_{in}	-0.6 to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

* With Respect to V_{SS}

■ RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min	typ	max	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	-0.1	-	0.8	V
	V_{IH}	2.0	-	$V_{CC} + 1$	V
Operating Temperature	T_{opr}	0	-	70	°C

■ DC AND OPERATING CHARACTERISTICS ($T_a = 0 \sim 70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Leakage Current	I_{LI}	$V_{CC} = 5.5\text{V}$, $V_{in} = 5.5\text{V}$	-	-	10	μA
Output Leakage Current	I_{LO}	$V_{CC} = 5.5\text{V}$, $V_{out} = 5.5/0.4\text{V}$	-	-	10	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{\text{CE}} = V_{IH}$	-	25	40	mA
V_{CC} Current (Active)	I_{CC2}	$\overline{\text{CE}} = V_{IL}$	-	60	100	mA
Input Low Voltage	V_{IL}		-0.1	-	0.8	V
Input High Voltage	V_{IH}		2.0	-	$V_{CC} + 1$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1\text{ mA}$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -400\ \mu\text{A}$	2.4	-	-	V

■ CAPACITANCE ($T_a = 25^\circ\text{C}$, $f = 1\text{MHz}$)

Parameter	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}	$V_{in} = 0\text{V}$	-	-	6	pF
Output Capacitance	C_{out}	$V_{out} = 0\text{V}$	-	-	12	pF

■ AC TEST CONDITIONS

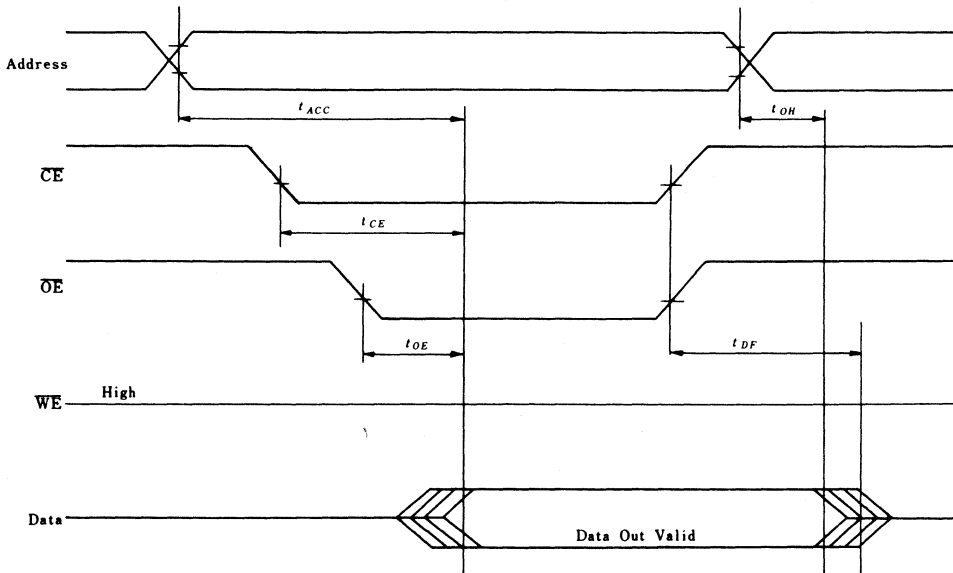
Input Pulse Levels:	0.4V to 2.4V
Input Rise and Fall Time:	$\leq 20\text{ns}$
Output Load:	1TTL Gate + 100pF
Reference Level for Measuring Timing:	0.8V and 2.0V

■ AC CHARACTERISTICS ($T_a = 0 \sim +70^\circ\text{C}$, $V_{CC} = 5\text{V} \pm 10\%$)

● READ OPERATION

Parameter	Symbol	Test Condition	HN58064P-25		HN58064P-30		Unit
			min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	–	250	–	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	–	250	–	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	–	100	–	150	ns
Address to Output Hold	t_{OH}	$\overline{CE} = \overline{OE} = V_{IL}, \overline{WE} = V_{IH}$	0	–	0	–	ns
\overline{OE} High to Output Float	t_{DF}	$\overline{CE} = V_{IL}, \overline{WE} = V_{IH}$	0	90	0	130	ns

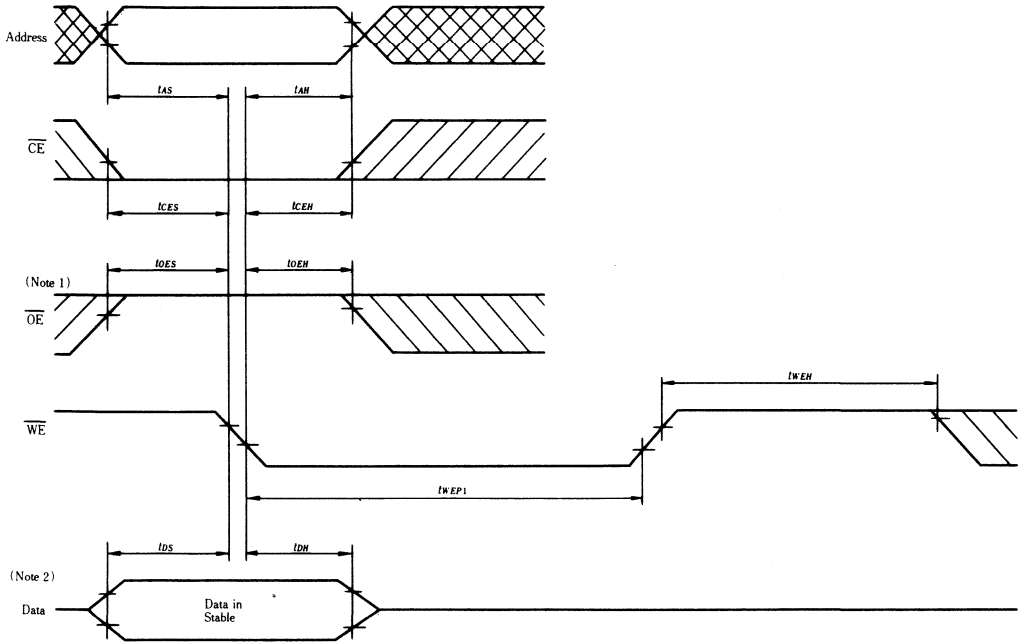
● WAVE FORM READ CYCLE



● BYTE ERASE AND BYTE WRITE OPERATION

Parameter	Symbol	Test Condition	min	typ	max	Unit
Address Setup Time	t_{AS}		0	—	—	ns
Address Hold Time	t_{AH}		100	—	—	ns
\overline{CE} Setup Time	t_{CES}		0	—	—	ns
\overline{CE} Hold Time	t_{CEH}		100	—	—	ns
\overline{OE} Setup Time	t_{OES}		0	—	—	ns
\overline{OE} Hold Time	t_{OEH}		100	—	—	ns
\overline{WE} Pulse Width	t_{WEP1}		8	10	15	ms
\overline{WE} High Time	t_{WEH}		1000	—	—	ns
Data Setup Time	t_{DS}		0	—	—	ns
Data Hold Time	t_{DH}		100	—	—	ns

● WAVE FORM ERASE AND WRITE CYCLE

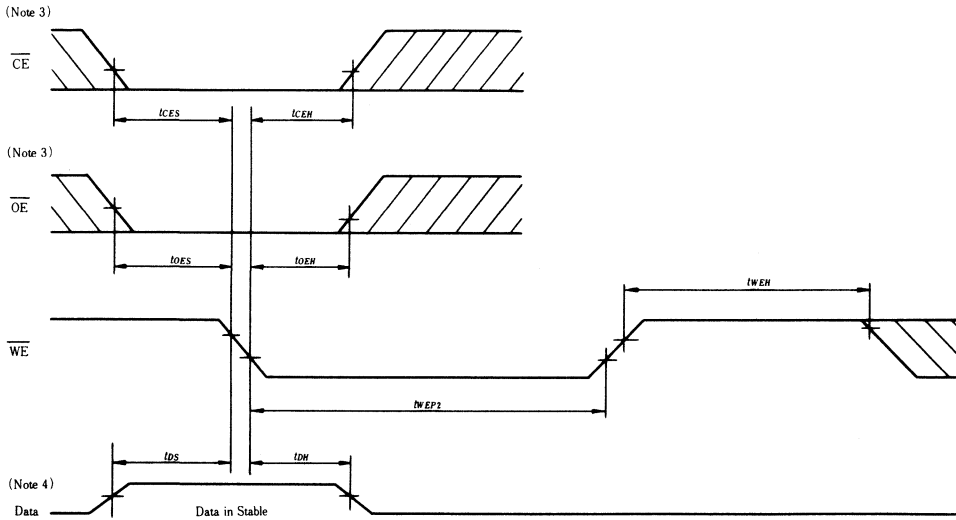


Note 1) \overline{CE} or \overline{OE} should be "1" and in Standby Mode or Deselect Mode before Write/Erase operation.
 Note 2) $I/O_{\overline{O}}$ to $I/O_{\overline{O}}$, must be "1" in Byte Erase.

● CHIP ERASE OPERATION I

Parameter	Symbol	Test Condition	min	typ	max	Unit
CE Setup Time	t_{CES}		0	—	—	ns
CE Hold Time	t_{CEH}		100	—	—	ns
OE Setup Time	t_{OES}		0	—	50	ns
OE Hold Time	t_{OEH}		100	—	—	ns
WE Pulse Width	t_{WEP2}		15	20	25	ms
WE High Time	t_{WEH}		1000	—	—	ns
Data Setup Time	t_{DS}		0	—	—	ns
Data Hold Time	t_{DH}		100	—	—	ns

● WAVE FORM CHIP ERASE I



Note 3) \overline{CE} or \overline{OE} should be "1" and in Standby Mode or Deselect Mode before Chip Erase operation.

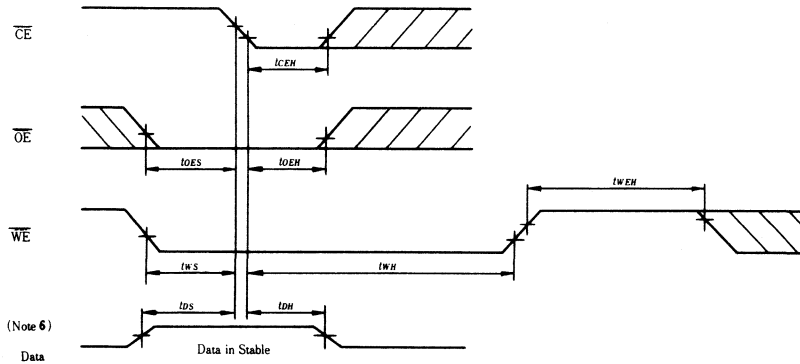
Note 4) I/O_0 to I/O_7 must be "1" in Chip Erase operation.

Note 5) Don't Care about Address.

● CHIP ERASE OPERATION II

Parameter	Symbol	Test Condition	min	typ	max	Unit
\overline{CE} Hold Time	t_{CEH}		100	—	—	ns
\overline{OE} Setup Time	t_{OES}		0	—	—	ns
\overline{OE} Hold Time	t_{OEH}		100	—	—	ns
\overline{WE} Setup Time	t_{WS}		0	—	—	ns
\overline{WE} Pulse Width	t_{WH}		15	20	25	ms
\overline{WE} High Time	t_{WEH}		1000	—	—	ns
Data Setup Time	t_{DS}		0	—	—	ns
Data Hold Time	t_{DH}		100	—	—	ns

● WAVE FORM CHIP ERASE II

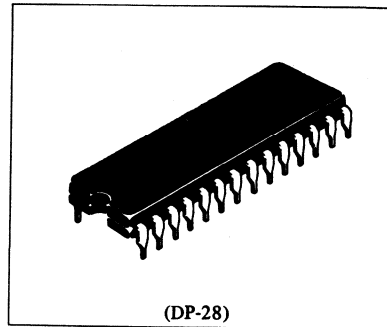


Note 6) I/O 0 ~ 7 must be "1" in Chip Erase Operation.
 Note 7) Don't Care about Address.

8192-word x 8-bit Electrically Erasable and Programmable CMOS ROM

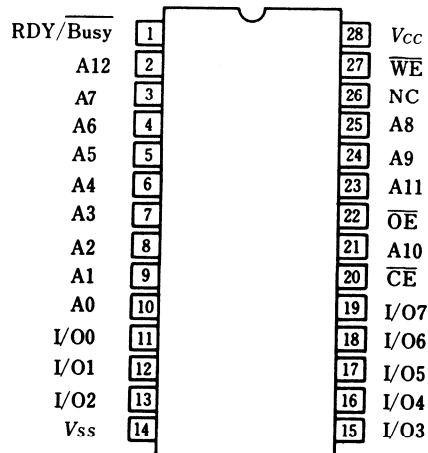
■ FEATURES

- Single 5V Supply
- On Chip Latches; Address, Data, \overline{CE} , \overline{OE} , \overline{WE}
- Automatic Byte Write 10ms typ.
- Automatic Page Write (32byte) 10ms typ.
- Fast Access Time 200/250/300ns max.
- Low Power Dissipation . . . 20mW/MHz typ. (Active) . . . 5 μ W typ. (Standby)
- \overline{Data} Polling and Ready/ \overline{Busy}
- Data Protection Circuitry on Power On/Power Off
- Conforms to JEDEC Byte-Wide Standard
- Reliable CMOS with MNOS Cell Technology
- 10000 Erase/Write Cycles and 10 year Data Retention



(DP-28)

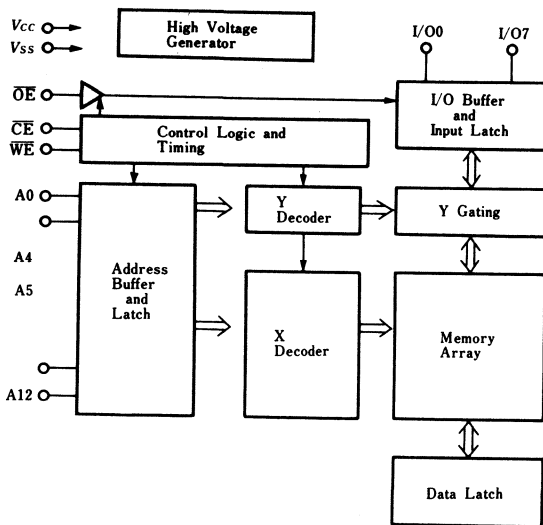
■ PIN ARRANGEMENT



(Top View)

A_0 to A_{12}	Address Input
$I/O1$ ~ $I/O7$	Data in/Data out
\overline{OE}	Output Enable
\overline{CE}	Chip Enable
\overline{WE}	Write Enable
V_{CC}	Power (+5V)
V_{SS}	GND
NC	No connect

■ BLOCK DIAGRAM



Note) The specifications of this device are subject to change without notice.
Please contact your nearest Hitachi's Sales Dept. regarding specifications.

MODE SELECTION

MODE	PINS	\overline{CE} (20)	\overline{OE} (22)	\overline{WE} (27)	RDY/Busy (1)	I/O (11 - 13, 15 - 19)
Read		V_{IL}	V_{IL}	V_{IH}	High Z	Dout
Standby		V_{IH}	x	x	High Z	High Z
Write		V_{IL}	V_{IH}	V_{IL}	High Z → V_{OL}	Din
Deselect		V_{IL}	V_{IH}	V_{IH}	High Z	High Z
Write Inhibit		x	x	V_{IH}	High Z	-
Write Inhibit		x	V_{IL}	x	High Z	-
Data Polling		V_{IL}	V_{IL}	V_{IH}	V_{OL}	Data Out (I/O7)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Value	Unit
Supply Voltage*	V_{CC}	-0.6 to +7.0	V
Input Voltage*	V_{in}	-0.5** to +7.0	V
Operating Temperature Range	T_{opr}	0 to +70	°C
Storage Temperature Range	T_{stg}	-55 to +125	°C

* With Respect to V_{SS}

** Pulse Width = 50ns : -3.0V

RECOMMENDED DC OPERATING CONDITIONS

Item	Symbol	min.	typ.	max.	Unit
Supply Voltage	V_{CC}	4.5	5.0	5.5	V
Input Voltage	V_{IL}	-0.3	-	0.8	V
	V_{IH}	2.2	-	$V_{CC}+1$	V
Operating Temperature	T_{opr}	0	-	70	°C

DC AND OPERATING CHARACTERISTICS ($T_a = 0$ to +70°C, $V_{CC} = 5V \pm 10\%$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Leakage Current	I_{LI}	$V_{CC} = 5.5V$ $V_{in} = 5.5V$	-	-	2	μA
Output Leakage Current	I_{LO}	$V_{CC} = 5.5V$ $V_{out} = 5.5/0.4V$	-	-	2	μA
V_{CC} Current (Standby)	I_{CC1}	$\overline{CE} = V_{IH}$	-	-	1	mA
		$\overline{CE} = V_{CC}$	-	-	100	μA
V_{CC} Current (Active)	I_{CC2}	$\overline{CE} = \overline{OE} = V_{IL}, I_{out} = 0mA, f = 1MHz$	-	-	8	mA
		200ns cycle	-	-	30	mA
		250ns cycle	-	-	25	
		300ns cycle	-	-	20	
Input Low Voltage	V_{IL}		-1.0*	-	0.8	V
Input High Voltage	V_{IH}		2.2	-	$V_{CC}+1$	V
Output Low Voltage	V_{OL}	$I_{OL} = 2.1mA$	-	-	0.4	V
Output High Voltage	V_{OH}	$I_{OH} = -400\mu A$	2.4	-	-	V

*Pulse Width: 50ns, DC: V_{IL} min = -0.3V

CAPACITANCE ($T_a = 25^\circ C, f = 1MHz$)

Parameter	Symbol	Test Condition	min.	typ.	max.	Unit
Input Capacitance	C_{in}	$V_{in} = 0V$	-	-	6	pF
Output Capacitance	C_{out}	$V_{out} = 0V$	-	-	12	pF

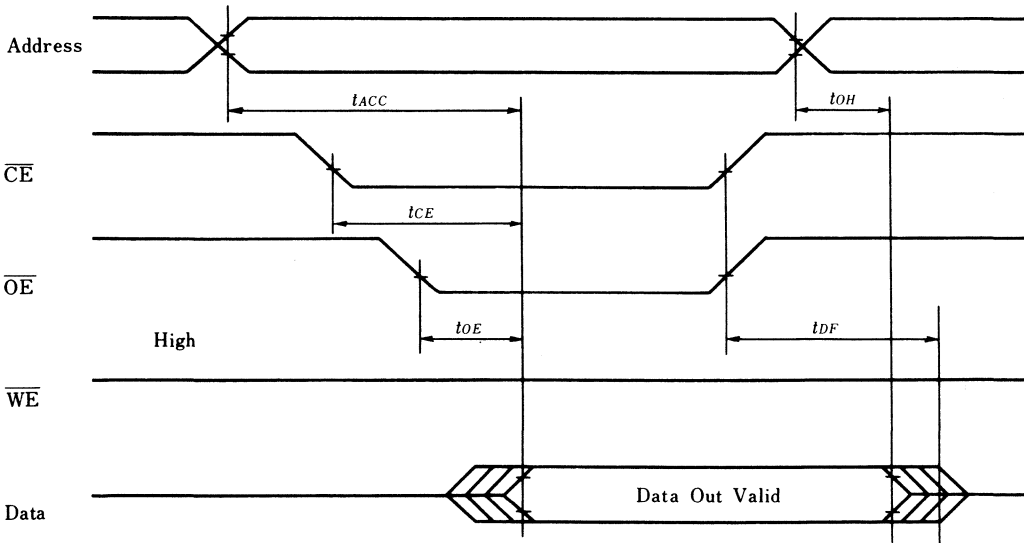
■ AC CHARACTERISTICS ($T_a=0$ to $+70^{\circ}\text{C}$, $V_{CC}=5\text{V}\pm 10\%$)

● AC Test Conditions

Input Pulse Levels: 0.40V to 2.4V
 Input Rise and Fall Time: $\leq 20\text{ns}$
 Output Load: 1TTL Gate + 100pF
 Reference Levels for Measuring Timing Inputs Outputs: 0.8V and 2.2V

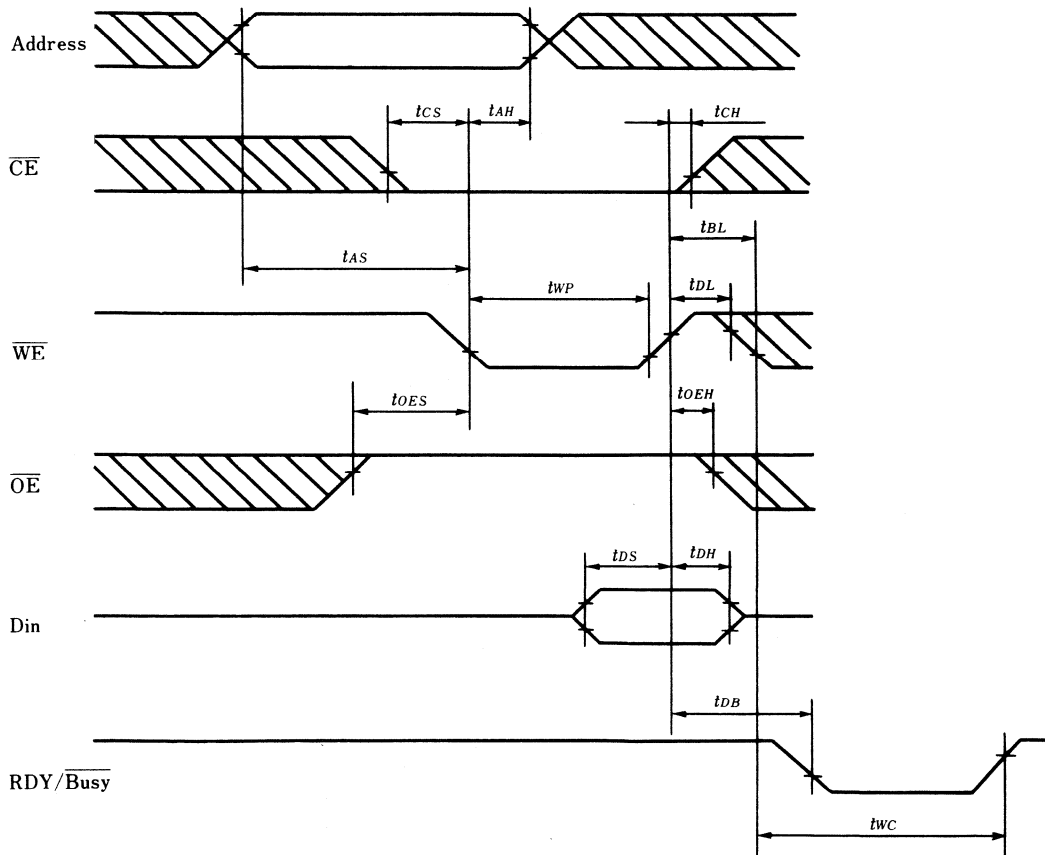
● Read Operation

Parameter	Symbol	Test Condition	HN58C65P-20		HN58C65P-25		HN58C65P-30		Unit
			min.	max.	min.	max.	min.	max.	
Address to Output Delay	t_{ACC}	$\overline{CE}=\overline{OE}=V_{IL}$ $\overline{WE}=V_{IH}$	-	200	-	250	-	300	ns
\overline{CE} to Output Delay	t_{CE}	$\overline{OE}=V_{IL}$ $\overline{WE}=V_{IH}$	-	200	-	250	-	300	ns
\overline{OE} to Output Delay	t_{OE}	$\overline{CE}=V_{IL}$ $\overline{WE}=V_{IH}$	10	70	10	100	10	150	ns
Address to Output Hold	t_{OH}	$\overline{CE}=\overline{OE}=V_{IL}$ $\overline{WE}=V_{IH}$	0	-	0	-	0	-	ns
\overline{OE} High to Output Float	t_{DF}	$\overline{CE}=V_{IL}$ $\overline{WE}=V_{IH}$	0	60	0	90	0	130	ns



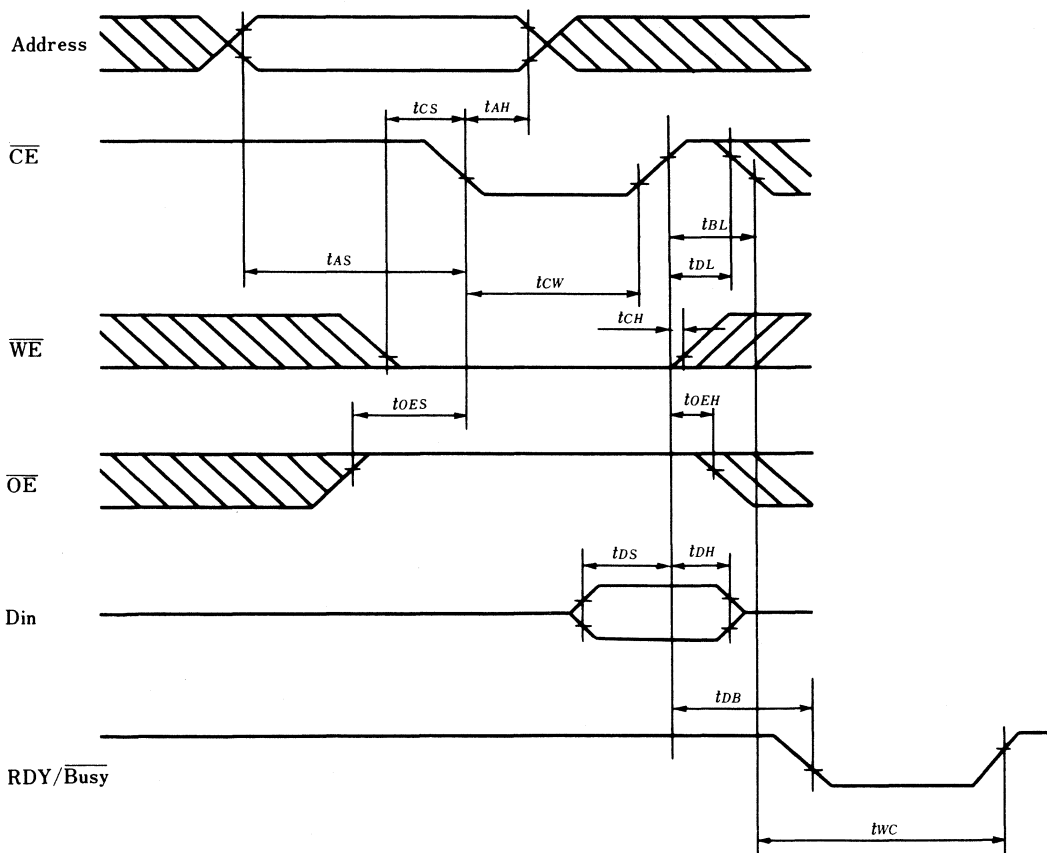
■ Byte Erase and Byte Write Operation (\overline{WE} Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	-	-	ns
\overline{CE} to Write Setup Time	t_{CS}	0	-	-	ns
Write Pulse Width	t_{WP}	200	-	-	ns
Address Hold Time	t_{AH}	150	-	-	ns
Data Setup Time	t_{DS}	100	-	-	ns
Data Hold Time	t_{DH}	20	-	-	ns
\overline{CE} Hold Time	t_{CH}	0	-	-	ns
\overline{OE} to Write Setup Time	t_{OES}	0	-	-	ns
\overline{OE} Hold Time	t_{OEH}	0	-	-	ns
Data Latch Time	t_{DL}	100	-	-	ns
Time to Device Busy	t_{DB}	120	-	-	ns
Write Cycle Time	t_{WC}	-	-	15	ms
Byte Load Window	t_{BL}	30	-	100	μ s



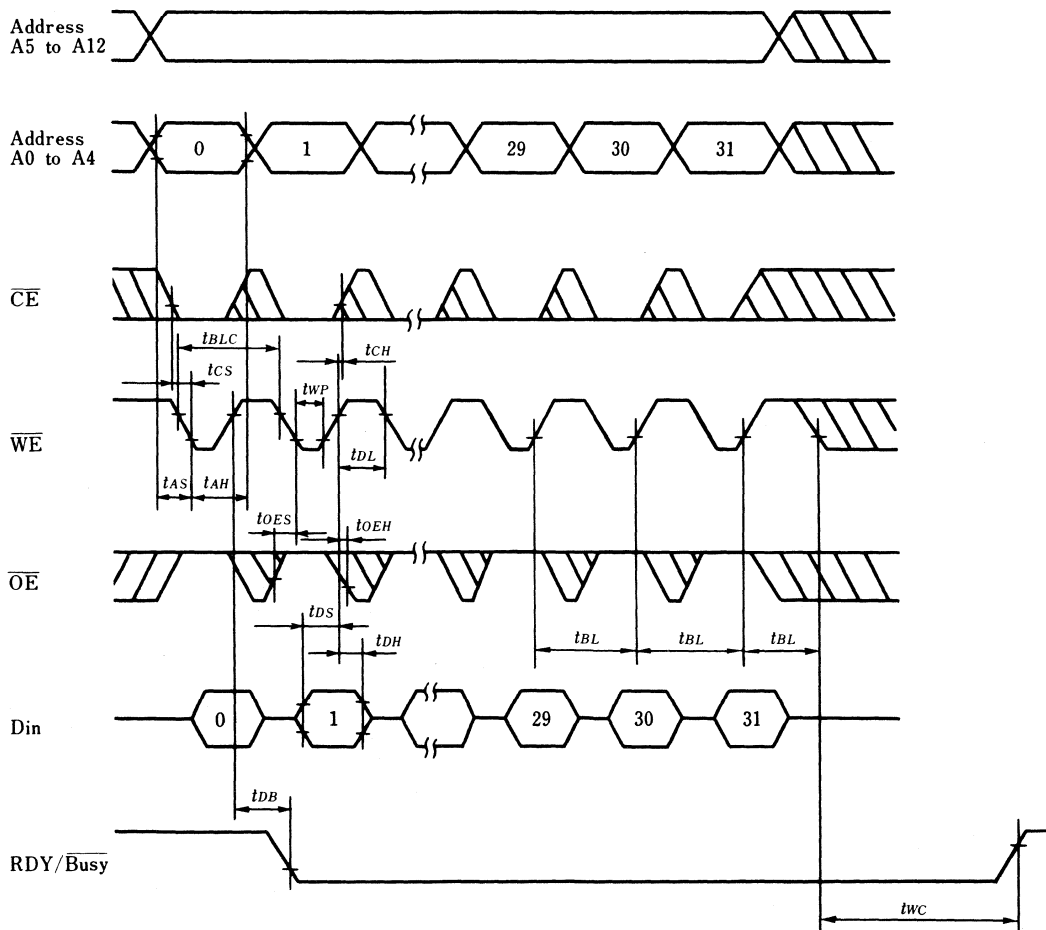
■ Byte Erase and Byte Write Operation (\overline{CE} Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	—	—	ns
\overline{CE} to Write Setup Time	t_{CS}	0	—	—	ns
\overline{CE} Pulse Width	t_{CW}	200	—	—	ns
Address Hold Time	t_{AH}	150	—	—	ns
Data Setup Time	t_{DS}	100	—	—	ns
Data Hold Time	t_{DH}	20	—	—	ns
\overline{CE} Hold Time	t_{CH}	0	—	—	ns
\overline{OE} to Write Setup Time	t_{OES}	0	—	—	ns
\overline{OE} Hold Time	t_{OEH}	0	—	—	ns
Data Latch Time	t_{DL}	100	—	—	ns
Time to Device Busy	t_{DB}	120	—	—	ns
Write Cycle Time	t_{WC}	—	—	15	ms
Byte Load Window	t_{BL}	30	—	100	μ s



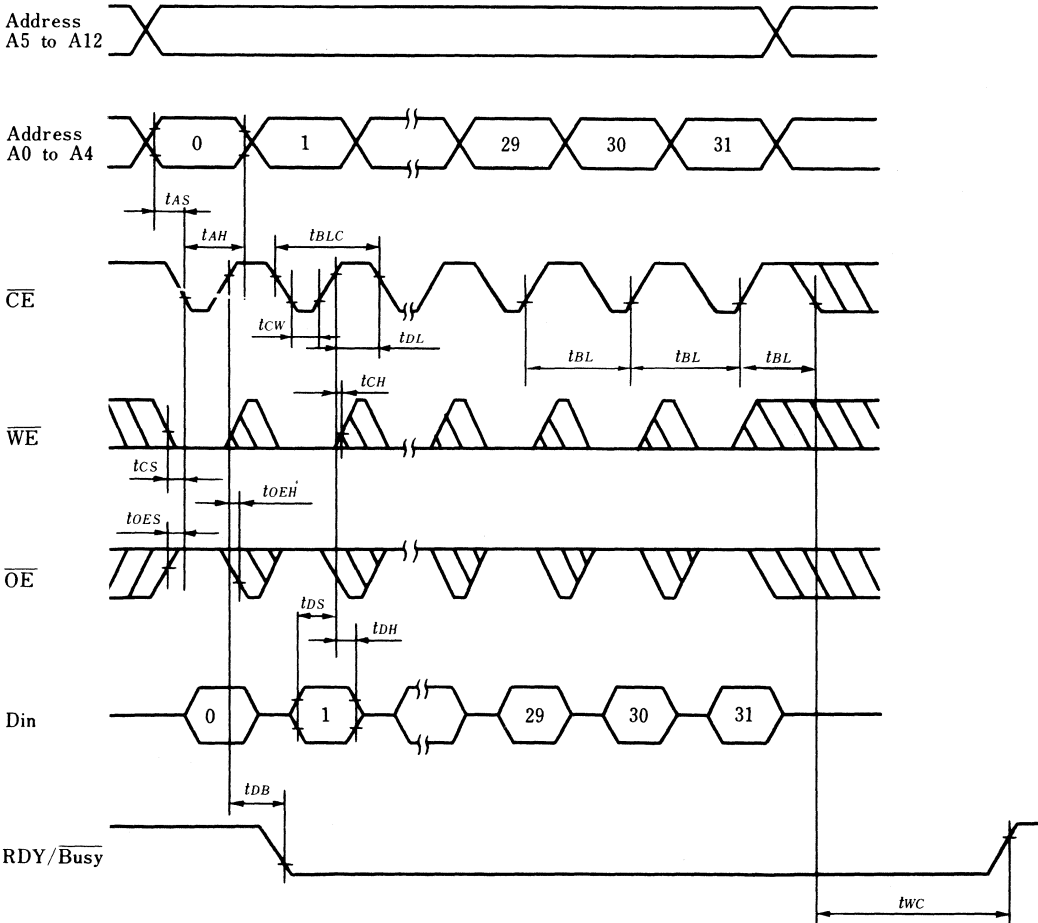
■ Page Erase and Page Write Operation (\overline{WE} Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	—	—	ns
CE to Write Setup Time	t_{CS}	0	—	—	ns
Write Pulse Width	t_{WP}	200	—	—	ns
Address Hold Time	t_{AH}	150	—	—	ns
Data Setup Time	t_{DS}	100	—	—	ns
Data Hold Time	t_{DH}	20	—	—	ns
\overline{CE} Hold Time	t_{CH}	0	—	—	ns
\overline{OE} to Write Setup Time	t_{OES}	0	—	—	ns
\overline{OE} Hold Time	t_{OEH}	0	—	—	ns
Data Latch Time	t_{DL}	100	—	—	ns
Time to Device Busy	t_{DB}	120	—	—	ns
Write Cycle Time	t_{WC}	—	—	15	ms
Byte Load Window	t_{BL}	30	—	100	μ s
Byte Load Cycle	t_{BLC}	0.3	—	30	μ s



■ Page Erase and Page Write Operation ($\overline{\text{CE}}$ Controlled Write Cycle)

Parameter	Symbol	min.	typ.	max.	Unit
Address Setup Time	t_{AS}	0	—	—	ns
$\overline{\text{CE}}$ to Write Setup Time	t_{CS}	0	—	—	ns
$\overline{\text{CE}}$ Pulse Width	t_{CW}	200	—	—	ns
Address Hold Time	t_{AH}	150	—	—	ns
Data Setup Time	t_{DS}	100	—	—	ns
Data Hold Time	t_{DH}	20	—	—	ns
$\overline{\text{CE}}$ Hold Time	t_{CH}	0	—	—	ns
$\overline{\text{OE}}$ to Write Setup Time	t_{OES}	0	—	—	ns
$\overline{\text{OE}}$ Hold Time	t_{OEH}	0	—	—	ns
Data Latch Time	t_{DL}	100	—	—	ns
Time to Device Busy	t_{DB}	120	—	—	ns
Write Cycle Time	t_{WC}	—	—	15	ms
Byte Load Window	t_{BL}	30	—	100	μs
Byte Load Cycle	t_{BLC}	0.3	—	30	μs



- **Automatic Page Write**

Page-mode write feature allows 1 to 32 bytes of data to be written into the EEPROM in a single write cycle. Following the initial byte cycle, an additional 1 to 31 bytes can be written in the same manner as the first byte was written. Each additional byte load cycle must be started within 30 μ s of the preceding rising edge of the \overline{WE} .

- **Data Polling**

Data polling allows comparison operation to determine the status of the EEPROM. During a write cycle, an attempted read of the last byte written in the EEPROM results in the complement data of that byte at I/O7.

- **Ready/Busy Signal**

RDY/Busy signal also allows to determine the status of the EEPROM, RDY/Busy signal has high impedance except in a write cycle and is lowered to V_{OL} after the first write signal. At the end of a write cycle, RDY/Busy signal changes its state to high impedance.

- **Write Protection**

There are four features that protect the data from an inadvertent write.

- 1) Noise Protection : A write cycle will not be initiated with a \overline{WE} pulse of less than 20ns.
- 2) V_{CC} Sense : When the V_{CC} is approximately 3.0 volt, Write and Erase functions are not initiated.
- 3) Write Inhibit : Holding \overline{OE} low, \overline{WE} high, or \overline{CE} high, inhibits a write cycle during power-on and power-off.
- 4) Write Inhibit : Holding \overline{OE} low, \overline{WE} low and \overline{CE} low, inhibits a write cycle during power-on and power-off.

- **\overline{WE} Pins Operation**

During a write cycle, addresses are latched on the falling edge of \overline{WE} : data are latched on the rising edge of \overline{WE} .

BIPOLAR RAM

HM10414, HM10414-1

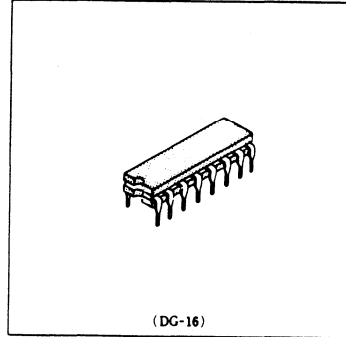
256-word × 1-bit Fully Decoded Random Access Memory

The HM10414 is ECL 10K compatible, 256-word x 1-bit, read write, random access memory developed for high speed systems such as scratch pad and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10414 is encapsulated in cerdip-16pin package, compatible with Fairchild's F10414.

- Fully compatible with 10K ECL level
- Address access time: HM10414: 10ns (max.)
HM10414-1: 8ns (max.)
- Write pulse width: 6ns (min.)
- Three chip select pins
- Output obtainable by wired-OR (open emitter)



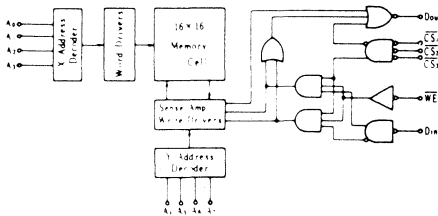
TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
any one H	×	×	L	Not Selected
all L	L	L	L	Write "0"
all L	L	H	L	Write "1"
all L	H	×	Dout *	Read

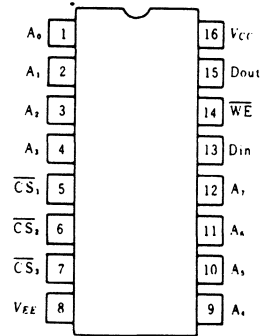
× : Don't care

* : Read out non-inverted

BLOCK DIAGRAM



PIN ARRANGEMENT



(Top View)

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	°C

* Under Bias

ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min (B)	typ	max (A)	Unit		
Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	0°C	-1000	-	-840	mV	
			+25°C	-960	-	-810		
			+75°C	-900	-	-720		
	V_{OL}		0°C	-1870	-	-1665		
			+25°C	-1850	-	-1650		
			+75°C	-1830	-	-1625		
Output Threshold Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	0°C	-1020	-	-	mV	
			+25°C	-980	-	-		
			+75°C	-920	-	-		
	V_{OL}		0°C	-	-	-1645		
			+25°C	-	-	-1630		
			+75°C	-	-	-1605		
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	-1145	-	-840	mV	
			+25°C	-1105	-	-810		
			+75°C	-1045	-	-720		
	V_{IL}		0°C	-1870	-	-1490		
			+25°C	-1850	-	-1475		
			+75°C	-1830	-	-1450		
Input Current	I_{IH}	$V_{IN} = V_{IH}$	0 to +75°C	-	-	220	μA	
	I_{IL}	CS	$V_{IN} = V_{IL}$	0 to +75°C	0.5	-		170
		Other			-50	-		-
Supply Current	I_{EF}	All Input and Output Open, Test Pin 8	+75°C	-	-130	-	mA	
			0°C	-180	-140	-		

AC CHARACTERISTICS

($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM10414			HM10414-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACK}		-	3	6	-	3	6	ns
Chip Select Recovery Time	t_{RCS}		-	3	6	-	3	6	ns
Address Access Time	t_{AA}		-	7	10	-	6	8	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10414			HM10414-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_w	$t_{WSA} = 2ns$	6	4	-	6	4	-	ns
Data Setup Time	t_{WSD}		1	0	-	1	0	-	ns
Data Hold Time	t_{WHD}		1	0	-	1	0	-	ns
Address Setup Time	t_{WSA}	$t_w = 6ns$	2	0	-	2	0	-	ns
Address Hold Time	t_{WHA}		2	0	-	2	0	-	ns
Chip Select Setup Time	t_{WSCS}		1	0	-	1	0	-	ns
Chip Select Hold Time	t_{WHCS}		1	0	-	1	0	-	ns
Write Disable Time	t_{WSD}		-	-	5	-	-	5	ns
Write Recovery Time	t_{WR}		-	-	12	-	-	10	ns

3. RISE/FALL TIME

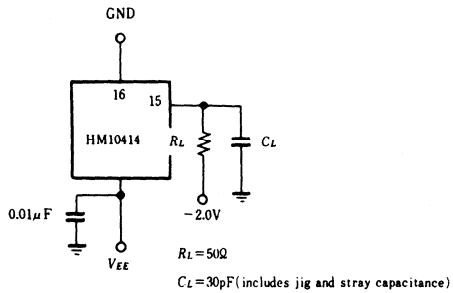
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		-	1.5	2.5	ns
Output Fall Time	t_f		-	1.5	2.5	ns

4. CAPACITANCE

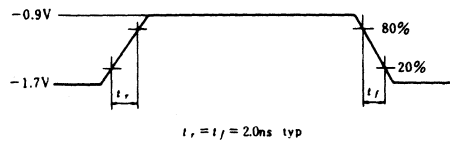
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		-	3	5	pF
Output Capacitance	C_{out}		-	5	8	pF

TEST CIRCUIT AND WAVEFORMS

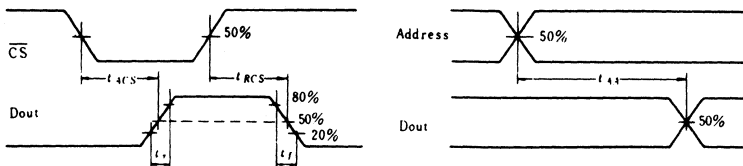
1. LOADING CONDITIONS



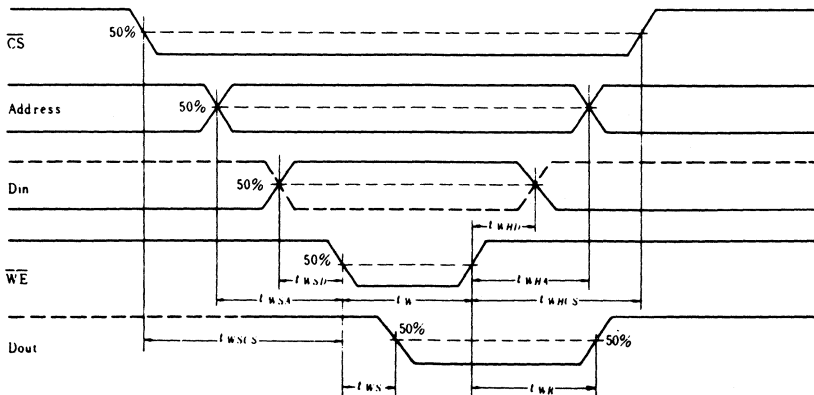
2. INPUT PULSE



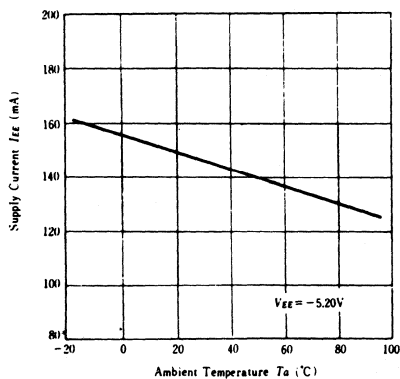
3. READ MODE



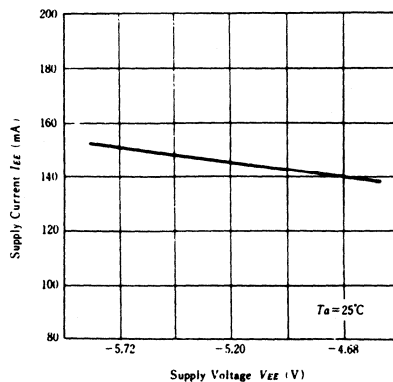
4. WRITE MODE



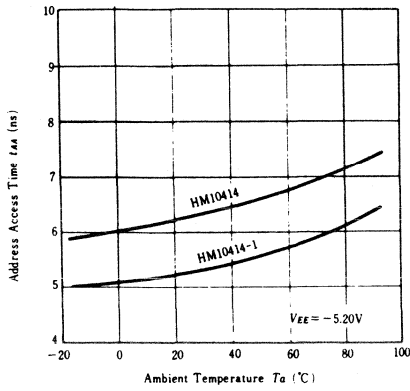
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



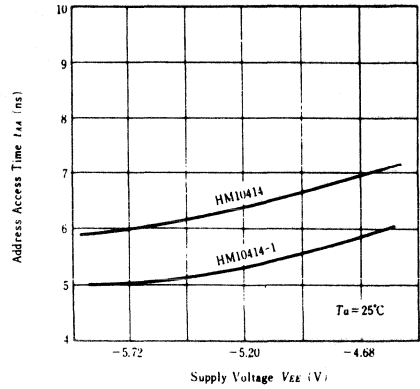
SUPPLY CURRENT vs. SUPPLY VOLTAGE



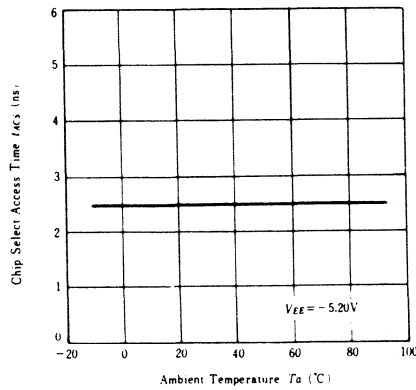
**ADDRESS ACCESS TIME
vs. AMBIENT TEMPERATURE**



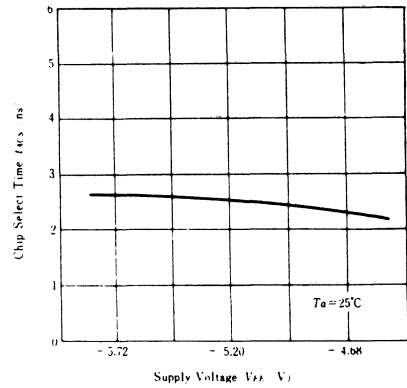
**ADDRESS ACCESS TIME
vs. SUPPLY VOLTAGE**



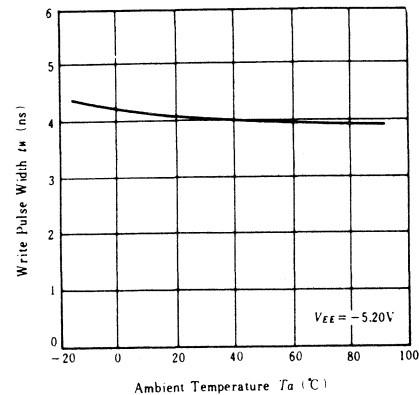
**CHIP SELECT ACCESS TIME
vs. AMBIENT TEMPERATURE**



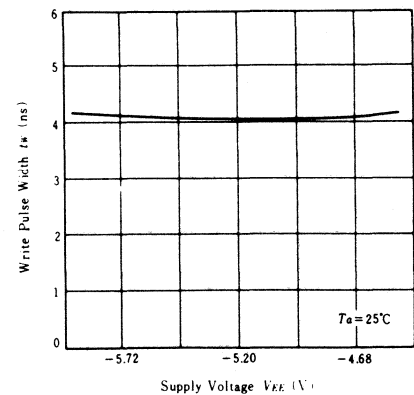
**CHIP SELECT ACCESS TIME
vs. SUPPLY VOLTAGE**



**WRITE PULSE WIDTH
vs. AMBIENT TEMPERATURE**



**WRITE PULSE WIDTH
vs. SUPPLY VOLTAGE**



HM10422

256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

■ FEATURES

- 256-word x 4 bit organization.
- Fully compatible with 10K ECL level
- Address access time: 10ns (max)
- Write pulse width: 6ns (min)
- Power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

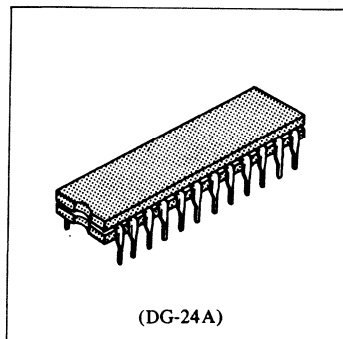
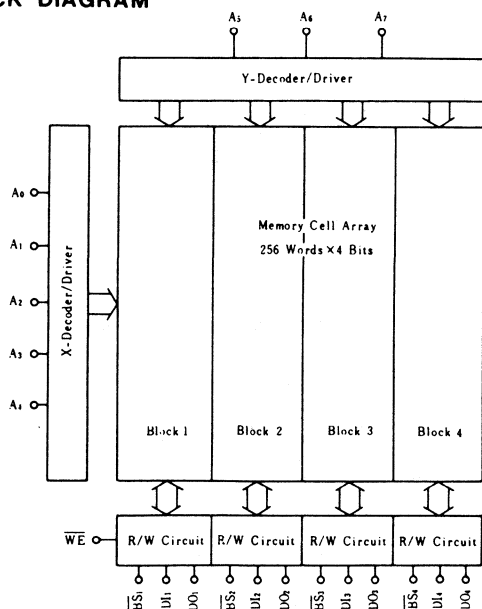
■ TRUTH TABLE

Input			Output	Mode
BS	WE	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

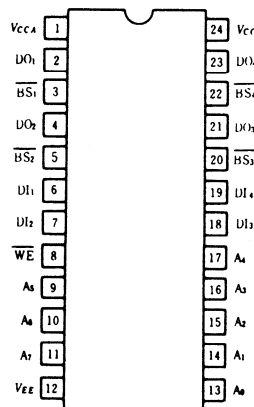
Notes) X : Irrelevant

* : Read out noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

($V_{EE} = -5.2\text{V}$, $R_L = 50\Omega$ to -2.0V , $T_a = 0$ to $+75^\circ\text{C}$, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit		
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1000	—	-840	mV	
			+25°C	-960	—	-810		
			+75°C	-900	—	-720		
	V_{OL}		0°C	-1870	—	-1665		
			+25°C	-1850	—	-1650		
			+75°C	-1830	—	-1625		
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	-1020	—	—	mV	
			+25°C	-980	—	—		
			+75°C	-920	—	—		
	V_{OLC}		0°C	—	—	-1645		
			+25°C	—	—	-1630		
			+75°C	—	—	-1605		
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	-1145	—	-840	mV	
			+25°C	-1105	—	-810		
			+75°C	-1045	—	-720		
	V_{IL}		0°C	-1870	—	-1490		
			+25°C	-1850	—	-1475		
			+75°C	-1830	—	-1450		
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA	
	I_{IL}	BS	$V_{IN} = V_{ILB}$	0 to +75°C	0.5	—		170
		Other		—	—	—		
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	$T_a = 0^\circ\text{C}$	-200	-160	—	mA	
			$T_a = 75^\circ\text{C}$	—	-145	—		

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{WSA} = 2\text{ns}$	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}	$t_w = 6\text{ns}$	2	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WS}		—	4	5	ns
Write Recovery Time	t_{WR}		—	4.5	12	ns

3. RISE/FALL TIME

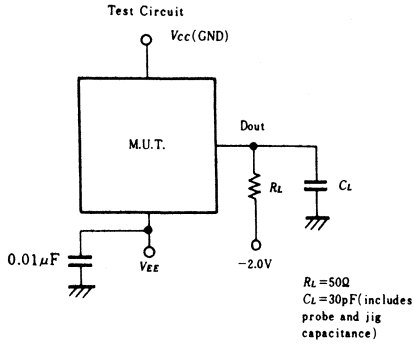
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

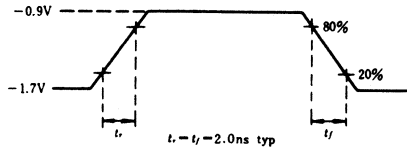
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

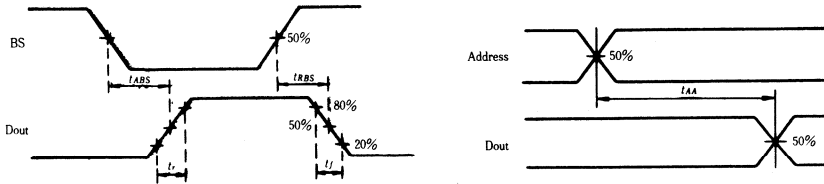
1. LOADING CONDITION



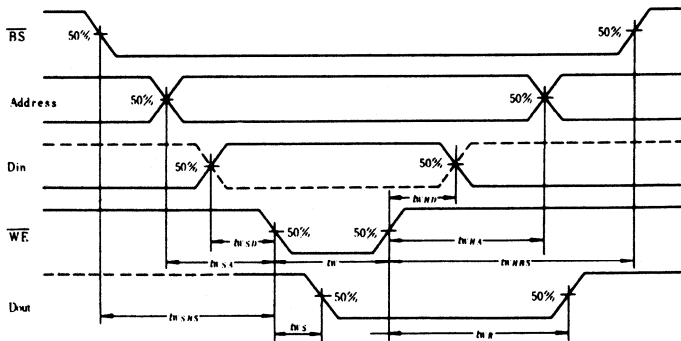
2. INPUT PULSE



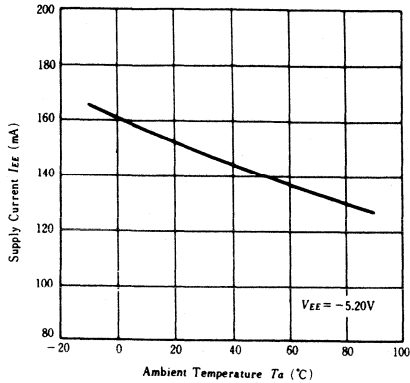
3. READ MODE



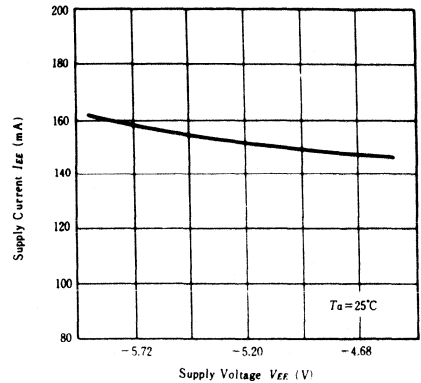
4. WRITE MODE



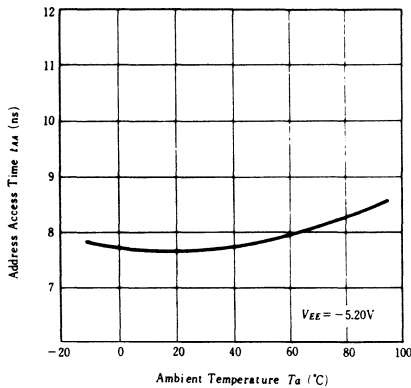
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



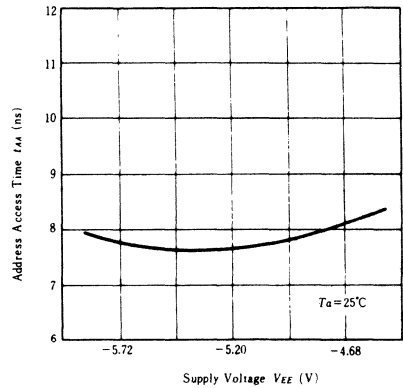
SUPPLY CURRENT vs. SUPPLY VOLTAGE



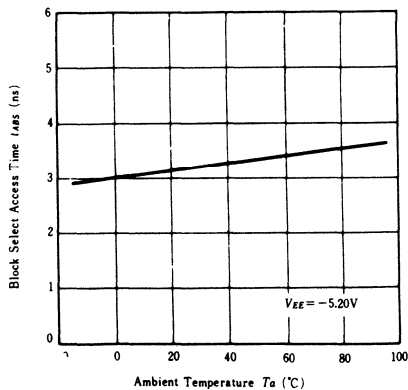
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



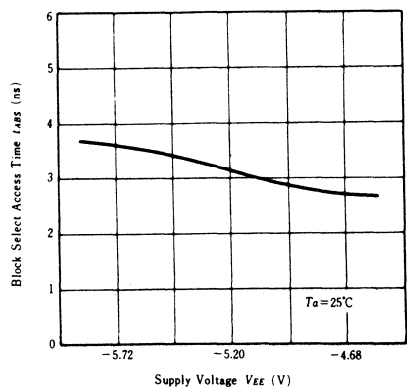
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



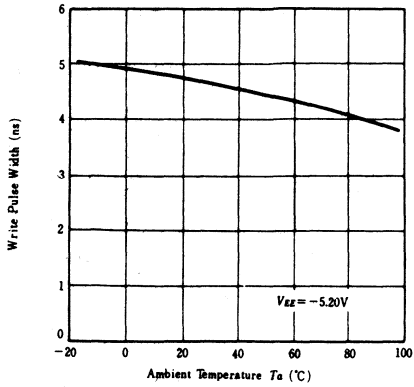
BLOCK SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



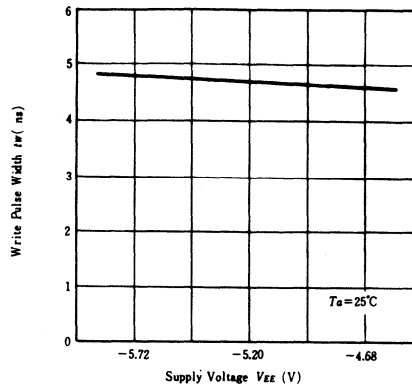
BLOCK SELECT ACCESS TIME vs. SUPPLY VOLTAGE



**WRITE PULSE WIDTH vs.
AMBIENT TEMPERATURE**



**WRITE PULSE WIDTH vs.
SUPPLY VOLTAGE**



HM10422-7

256-word × 4-bit Fully Decoded Random Access Memory

The HM10422 is ECL 10K compatible, 256-word x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10422 is encapsulated in cerdip-24 pin package, compatible with Fairchild's F10422.

■ FEATURES

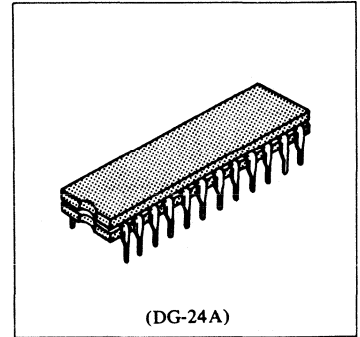
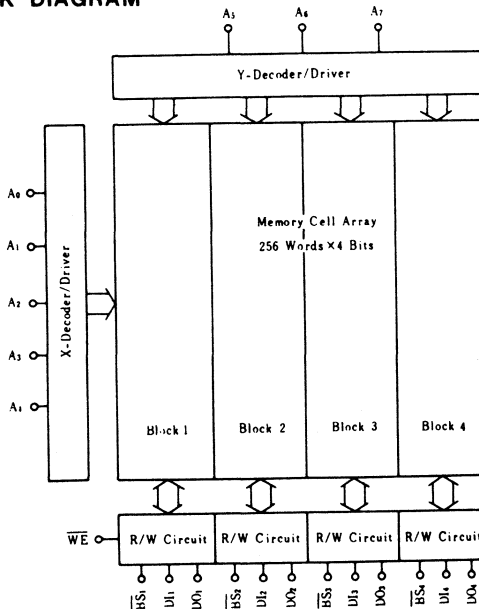
- 256-word x 4 bit organization
- Fully compatible with 10K ECL level
- Address access time: 7ns (max)
- Write pulse width: 4ns (min)
- Power dissipation: 1.0 mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

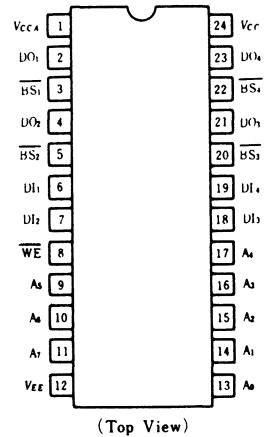
Input			Output	Mode
\overline{BS}	\overline{WE}	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant
* : Read out noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

($V_{EE} = -5.2\text{V}$, $R_L = 50\Omega$ to -2.0V , $T_a = 0$ to $+75^\circ\text{C}$, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}	0°C	-1000	—	-840	mV
			+25°C	-960	—	-810	
			+75°C	-900	—	-720	
	V_{OL}		0°C	-1870	—	-1665	
			+25°C	-1850	—	-1650	
			+75°C	-1830	—	-1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILA}	0°C	-1020	—	—	mV
			+25°C	-980	—	—	
			+75°C	-920	—	—	
	V_{OLC}		0°C	—	—	-1645	
			+25°C	—	—	-1630	
			+75°C	—	—	-1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	-1145	—	-840	mV
			+25°C	-1105	—	-810	
			+75°C	-1045	—	-720	
	V_{IL}		0°C	-1870	—	-1490	
			+25°C	-1850	—	-1475	
			+75°C	-1830	—	-1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C	—	—	220	μA
	I_{IL}	$\overline{\text{BS}}$	$V_{IN} = V_{ILB}$	0 to +75°C	0.5	—	
Other		—		—	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12	$T_a = 0^\circ\text{C}$	-240	-200	—	mA
			$T_a = 75^\circ\text{C}$	—	-180	—	

● AC CHARACTERISTICS

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	5	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	4	7	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit	
Write Pulse Width	t_w	$t_{WSA} = 2\text{ns}$	4	3	—	ns	
Data Setup Time	t_{WSD}	$t_w = 4\text{ns}$	1	—	—	ns	
Data Hold Time	t_{WHD}		1	—	—	ns	
Address Setup Time	t_{WSA}		2	—	—	ns	
Address Hold Time	t_{WHA}		1	—	—	ns	
Block Select Setup Time	t_{WBS}		1	—	—	ns	
Block Select Hold Time	t_{WBS}		1	—	—	ns	
Write Disable Time	t_{WS}		—	3	5	ns	
Write Recovery Time	t_{WR}		—	—	3	8	ns
			—	—	3	8	ns

3. RISE/FALL TIME

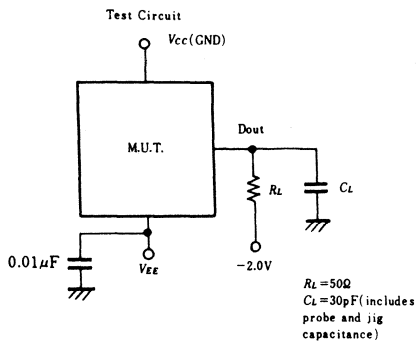
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

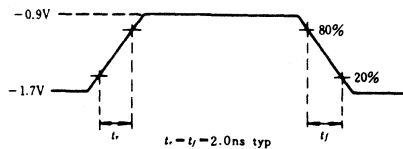
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

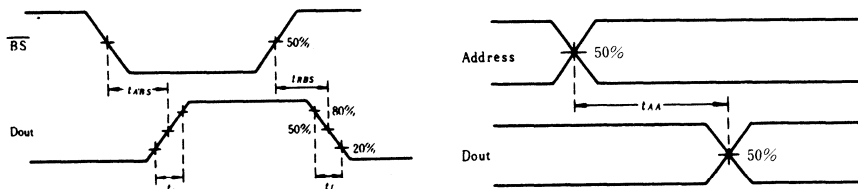
1. LOADING CONDITION



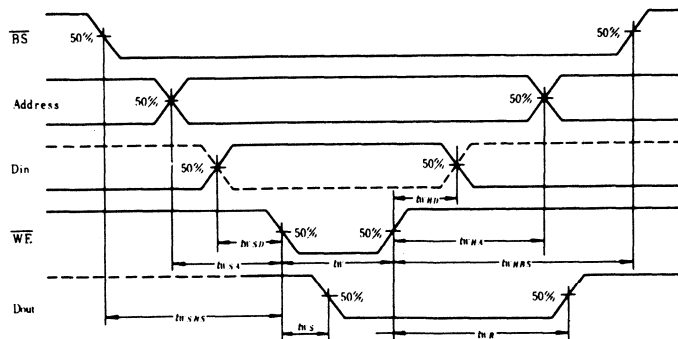
2. INPUT PULSE



3. READ MODE



4. WRITE MODE

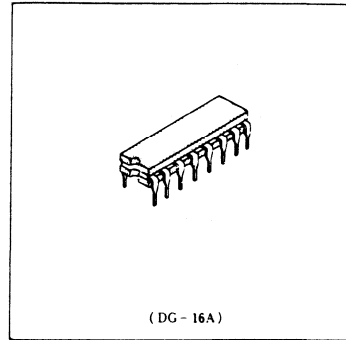


HM2110, HM2110-1

1024-word × 1-bit Fully Decoded Random Access Memory

The HM2110 Series item is an ECL compatible, 1024-word × 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

- It is compatible with 10K ECL logic.
- Chip select access time 10ns (max.)
- Address access time HM2110: 35ns (max.)
HM2110-1: 25ns (max.)
- Power consumption , 0.5mW/bit (typ)
- Output obtainable by Wired-OR (open emitter).



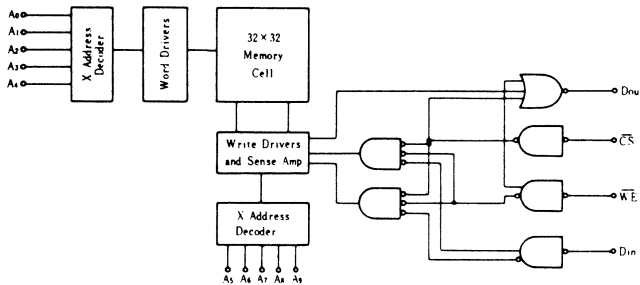
TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

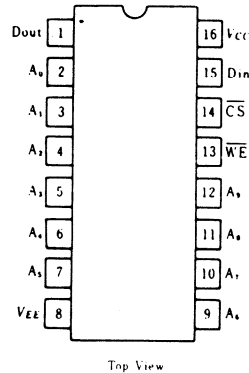
× : irrelevant

* : Read out noninverted

BLOCK DIAGRAM



PIN ARRANGEMENT



Top View

ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2110 Series	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit			
Output Voltage	V_{OH}	$V_{IN} = V_{IHA}$ or V_{ILB}		0°C	—	-840	mV			
				+25°C	—	-810				
				+75°C	—	-720				
	V_{OL}			0°C	—	-1665				
				+25°C	—	-1650				
				+75°C	—	-1625				
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IHB}$ or V_{ILB}		0°C	—	—	mV			
				+25°C	—	—				
				+75°C	—	—				
	V_{OLC}			0°C	—	-1645				
				+25°C	—	-1630				
				+75°C	—	-1605				
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	—	-840	mV			
				+25°C	—	-810				
				+75°C	—	-720				
	V_{IL}			Guaranteed Input Voltage Low for All Inputs		0°C		—	-1490	
						+25°C		—	-1475	
						+75°C		—	-1450	
Input Current	I_{IH}	$V_{IN} = V_{IHA}$	0 to +75°C			—	—	220	μA	
						I_{IL}	Other	$V_{IN} = V_{ILB}$		0 to +75°C
	\overline{CS}		0.5							—
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8		$0 \leq T_a < 25^\circ C$	-150	-100	mA			
				$T_a \geq 25^\circ C$	-125	-90				

● AC CHARACTERISTICS

($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec, see test circuit and waveforms)

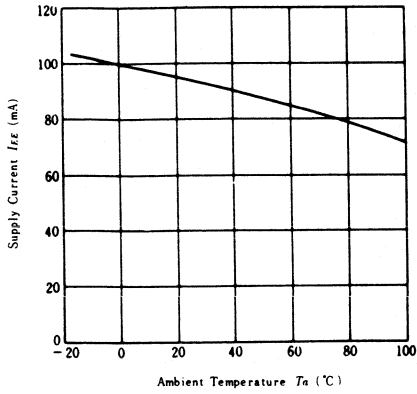
1. READ MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	7	10	—	7	10	ns
Chip Select Recovery Time	t_{RCS}		—	7	10	—	7	10	ns
Address Access Time	t_{AA}		—	20	35	—	15	25	ns

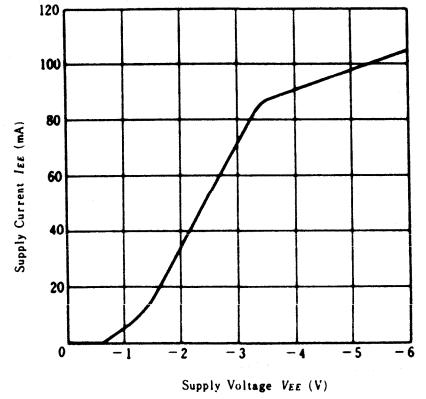
2. WRITE MODE

Item	Symbol	Test Condition	HM2110			HM2110-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA} = 8ns$	25	—	—	25	—	—	ns
Data Setup Time	t_{WSD}	$t_W = 25ns$	5	—	—	5	—	—	ns
Data Hold Time	t_{WHD}		5	—	—	5	—	—	ns
Address Setup Time	t_{WSA}		8	—	—	8	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSDS}		5	—	—	5	—	—	ns
Chip Select Hold Time	t_{WMCS}		5	—	—	5	—	—	ns
Write Disable Time	t_{WS}		—	—	10	—	—	10	ns
Write Recovery Time	t_{WR}		—	—	37	—	—	37	ns

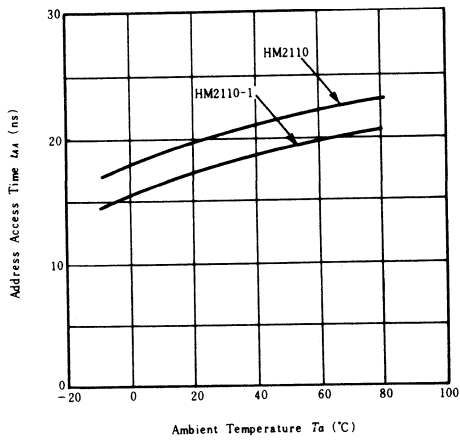
**SUPPLY CURRENT vs.
AMBIENT TEMPERATURE**



**SUPPLY CURRENT vs.
SUPPLY VOLTAGE**



**ADDRESS ACCESS TIME vs.
AMBIENT TEMPERATURE**



HM2112, HM2112-1

1024-word × 1-bit Fully Decoded Random Access Memory

The HM2112 is an ECL compatible, 1024-word x 1-bit, read/write, random access memory developed for application to scratch pads, control and buffer memories, etc. which require high speeds.

■ FEATURES

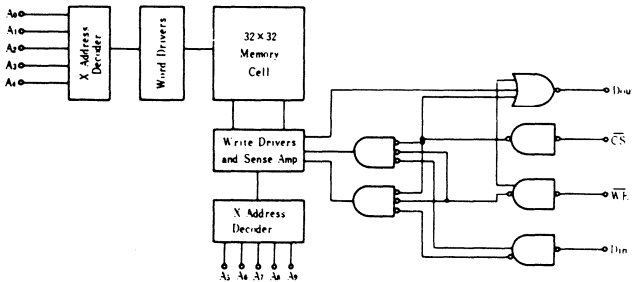
- Level 10k ECL Compatible
- Construction 1024-word by 1-bit
- Address Access Time HM2112 10ns (max.)
HM2112-1 8ns (max.)
- Chip Select Access Time 5ns (max.)
- Power Consumption 0.8mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Fully Pin Compatible with F10415

■ TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

× : Irrelevant
* : Read out noninverted

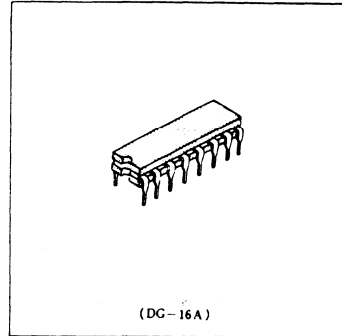
■ BLOCK DIAGRAM



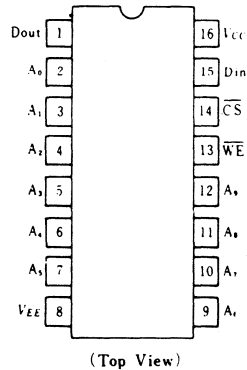
■ ABSOLUTE MAXIMUM RATINGS

Item	Symbol	HM2112	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(Bias)^*$	-55 to +125	°C

* Under Bias



■ PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

● DC CHARACTERISTICS

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{IN} = V_{IH(A)}$ or $V_{IL(B)}$	0°C	-1000	—	-840	mV
			+25°C	-960	—	-810	
			+75°C	-900	—	-720	
	V_{OL}		0°C	-1870	—	-1665	
			+25°C	-1850	—	-1650	
			+75°C	-1830	—	-1625	
Output Threshold Voltage	$V_{OH(C)}$	$V_{IN} = V_{IH(B)}$ or $V_{IL(A)}$	0°C	-1020	—	—	mV
			+25°C	-980	—	—	
			+75°C	-920	—	—	
	$V_{OL(C)}$		0°C	—	—	-1645	
			+25°C	—	—	-1630	
			+75°C	—	—	-1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	-1145	—	-840	mV
			+25°C	-1105	—	-810	
			+75°C	-1045	—	-720	
	V_{IL}		0°C	-1870	—	-1490	
			+25°C	-1850	—	-1475	
			+75°C	-1830	—	-1450	
Input Current	I_{IL}	$V_{IN} = V_{IH(A)}$	0 to +75°C	—	—	220	μA
		CS	$V_{IN} = V_{IL(B)}$	0 to +75°C	0.5	—	
	Other			—	—	—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 8		$T_a = 0^\circ C$	-240	—	—
			$T_a = 75^\circ C$	-200	—	—	

● AC CHARACTERISTICS

($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec, see test circuit and waveforms)

1. READ MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		1	3	6	1	3	6	ns
Chip Select Recovery Time	t_{RCS}		1	3	5	1	3	5	ns
Address Access Time	t_{AA}		3	6.5	8	3	7.5	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM2112-1			HM2112			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_w	$t_{WSA} = 3ns$	7	2	—	7	2	—	ns
Data Setup Time	t_{WSD}	$t_w = 7ns$	1	0	—	1	0	—	ns
Data Hold Time	t_{WHD}		1	0	—	1	0	—	ns
Address Setup Time	t_{WSA}		3	0	—	3	0	—	ns
Address Hold Time	t_{WHA}		2	0	—	2	0	—	ns
Chip Select Setup Time	t_{WSCS}		1	0	—	1	0	—	ns
Chip Select Hold Time	t_{WNCS}		1	0	—	1	0	—	ns
Write Disable Time	t_{WS}		1	3	5	1	3	5	ns
Write Recovery Time	t_{WR}		1	3	10	1	3	12	ns

3. RISE/FALL TIME

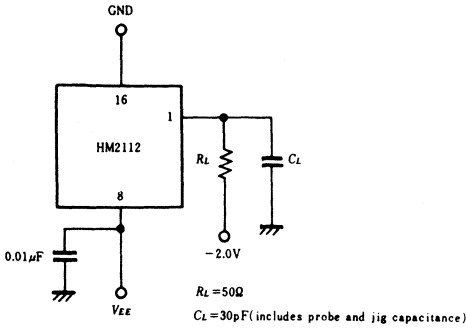
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		0.8	1.5	2.5	ns
Output Fall Time	t_f		0.8	1.5	2.5	ns

4. CAPACITANCE

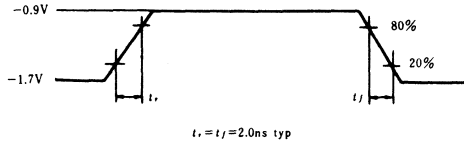
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		1	3	5	pF
Output Capacitance	C_{out}		3	5	8	pF

■ TEST CIRCUIT AND WAVEFORMS

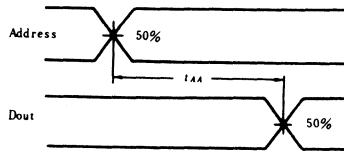
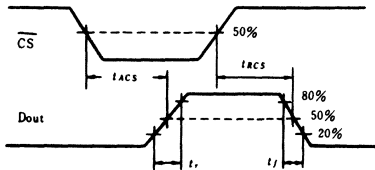
1. LOADING CONDITION



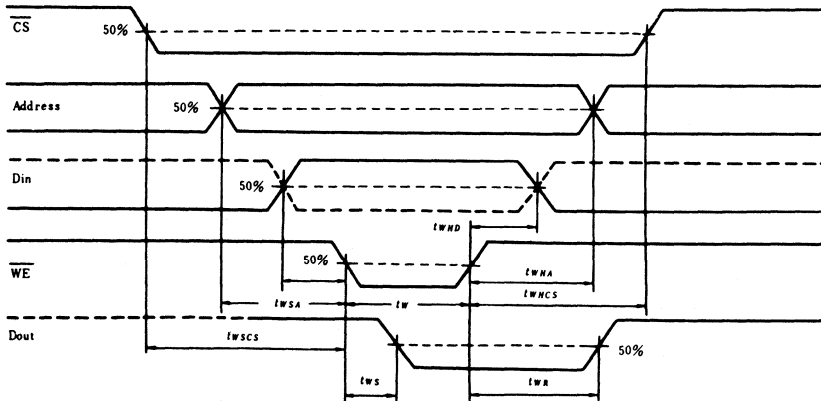
2. INPUT PULSE



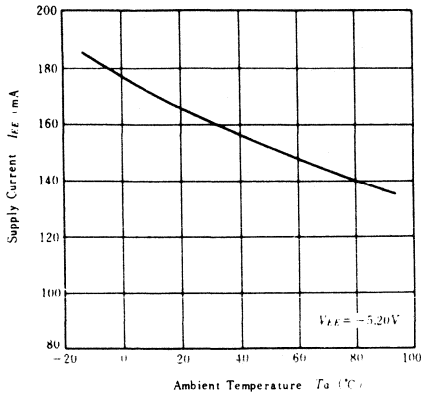
3. READ MODE



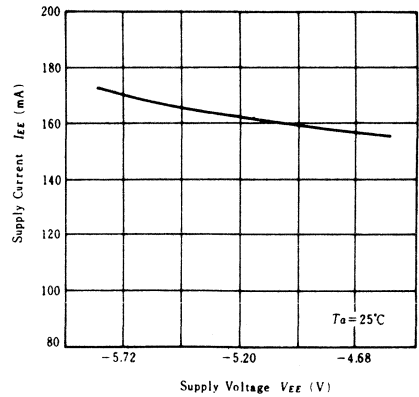
4. WRITE MODE



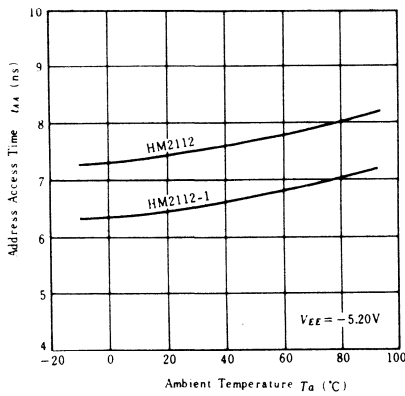
**SUPPLY CURRENT
vs. AMBIENT TEMPERATURE**



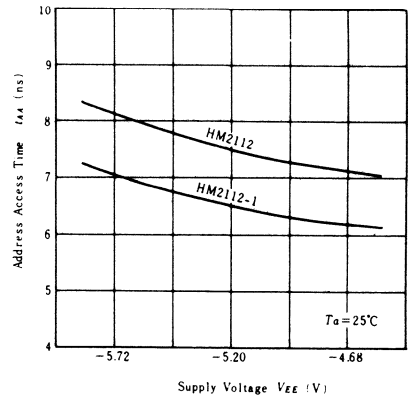
**SUPPLY CURRENT
vs. SUPPLY VOLTAGE**



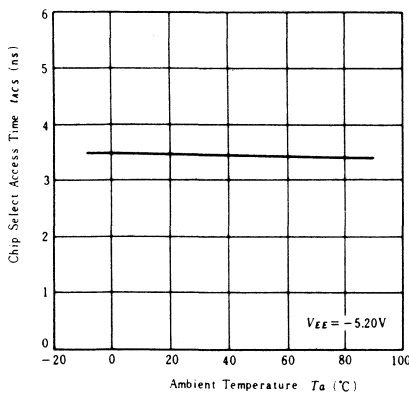
**ADDRESS ACCESS TIME
vs. AMBIENT TEMPERATURE**



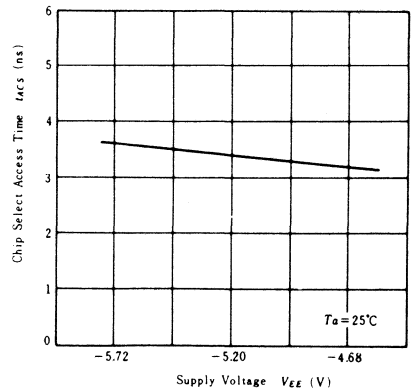
**ADDRESS ACCESS TIME
vs. SUPPLY VOLTAGE**



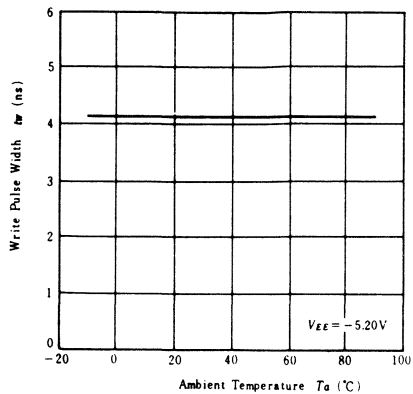
**CHIP SELECT ACCESS TIME
vs. AMBIENT TEMPERATURE**



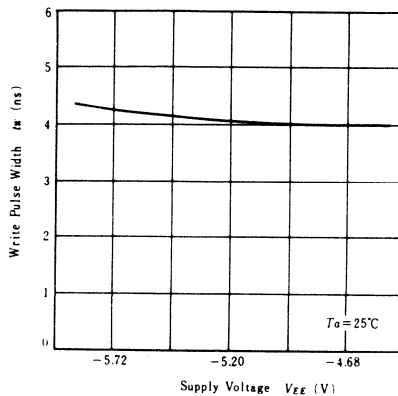
**CHIP SELECT ACCESS TIME
vs. SUPPLY VOLTAGE**



**WRITE PULSE WIDTH
vs. AMBIENT TEMPERATURE**



**WRITE PULSE WIDTH
vs. SUPPLY VOLTAGE**



HM10474

1024-word × 4-bit Fully Decoded Random Access Memory

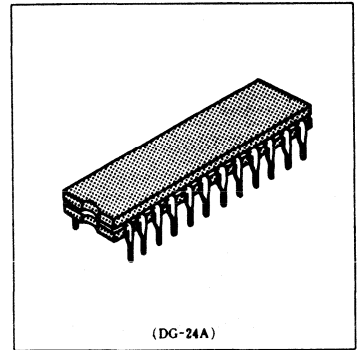
The HM10474 is ECL 10k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

■ FEATURES

- 1024-word x 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)



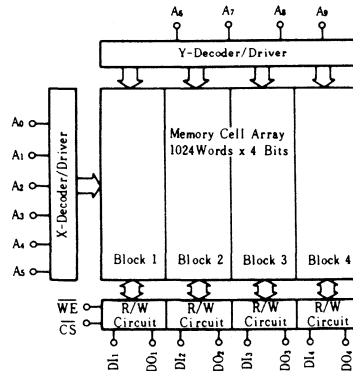
(DG-24A)

■ TRUTH TABLE

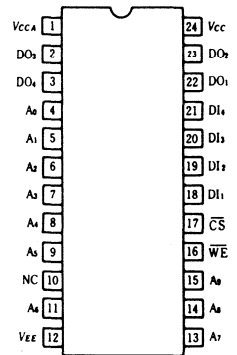
Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM



■ PIN ARRANGEMENT



(Top View)

■ ABSOLUTE MAXIMUM RATINGS (T_a = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V _{EE} to V _{CC}	+0.5 to -7.0	V
Input Voltage	V _{in}	+0.5 to V _{EE}	V
Output Current	I _{out}	-30	mA
Storage Temperature	T _{stg}	-65 to +150	°C
Storage Temperature	T _{stg} (Bias)*	-55 to +125	°C

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit			
Output Voltage	V_{OH}	$V_{IN} = V_{IH\bar{A}}$ or $V_{IL\bar{B}}$		0°C	-1000	-	-840	mV		
				+25°C	-960	-	-810			
				+75°C	-900	-	-720			
	V_{OL}			0°C	-1870	-	-1665			
				+25°C	-1850	-	-1650			
				+75°C	-1830	-	-1625			
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\bar{B}}$ or $V_{IL\bar{A}}$		0°C	-1020	-	-	mV		
				+25°C	-980	-	-			
				+75°C	-920	-	-			
	V_{OLC}			0°C	-	-	-1645			
				+25°C	-	-	-1630			
				+75°C	-	-	-1605			
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	-1145	-	-840	mV		
				+25°C	-1105	-	-810			
				+75°C	-1045	-	-720			
	V_{IL}			0°C	-1870	-	-1490			
				+25°C	-1850	-	-1475			
				+75°C	-1830	-	-1450			
Input Current	I_{IN}	$V_{IN} = V_{IH\bar{A}}$		0 to +75°C	-	-	220	μA		
				I_{IL}	CS	$V_{IN} = V_{IL\bar{B}}$	0 to +75°C		0.5	-
	Others				0 to +75°C		-50		-	-
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12		$T_a = 0^\circ C$	-200	-160	-	mA		
				$T_a = 75^\circ C$	-	-145	-			

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		-	-	10	ns
Chip Select Recovery Time	t_{RCS}		-	-	10	ns
Address Access Time	t_{AA}		-	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA} = 3ns$	25	15	-	ns
Data Setup Time	t_{WSD}		2	-	-	ns
Data Hold Time	t_{WHD}		2	-	-	ns
Address Setup Time	t_{WSA}	$t_W = t_{W\bar{A}}$	3	-	-	ns
Address Hold Time	t_{WHA}		2	-	-	ns
Chip Select Setup Time	t_{WSCS}		2	-	-	ns
Chip Select Hold Time	t_{WHCS}		2	-	-	ns
Write Disable Time	t_{WS}		-	-	10	ns
Write Recovery Time	t_{WR}		-	-	27	ns

3. RISE/FALL TIME

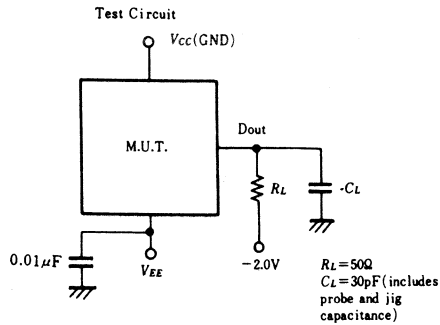
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

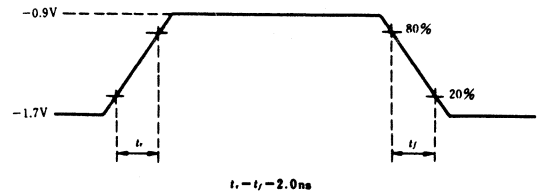
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

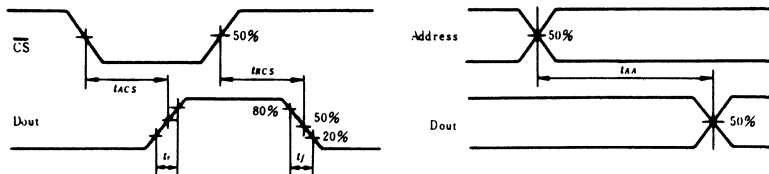
1. LOADING CONDITION



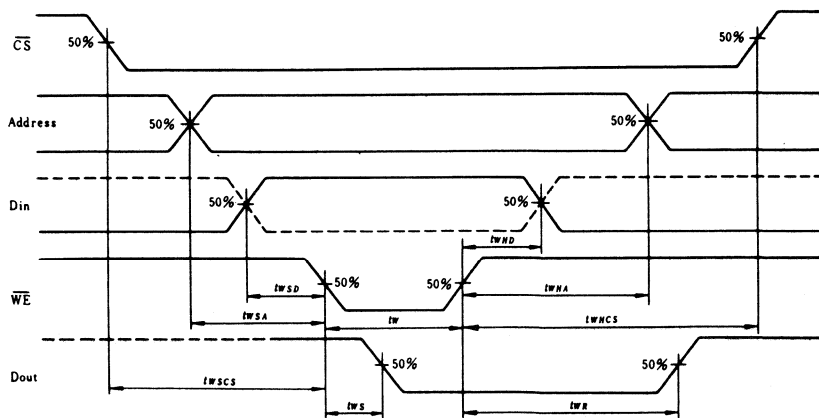
2. INPUT PULSE



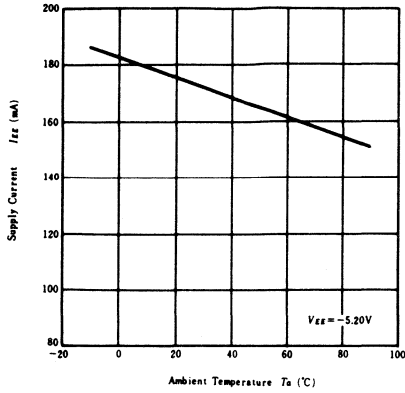
3. READ MODE



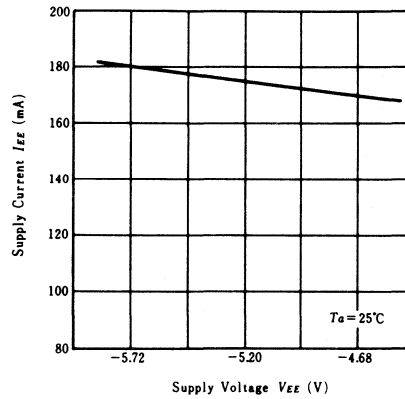
4. WRITE MODE



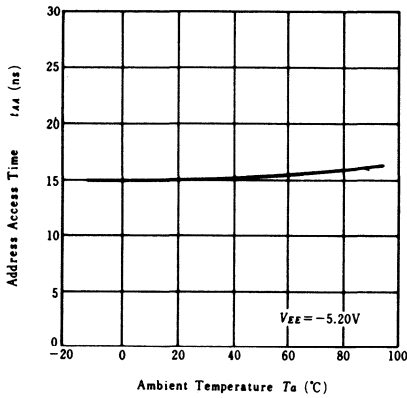
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



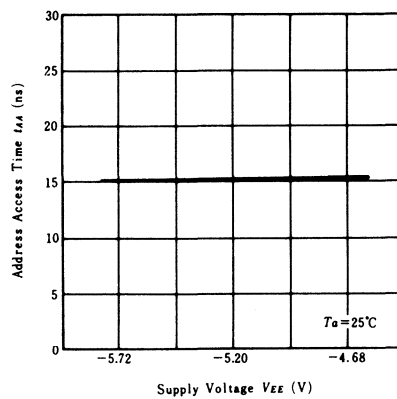
SUPPLY CURRENT vs. SUPPLY VOLTAGE



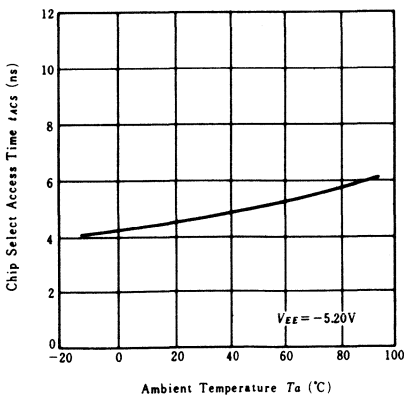
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



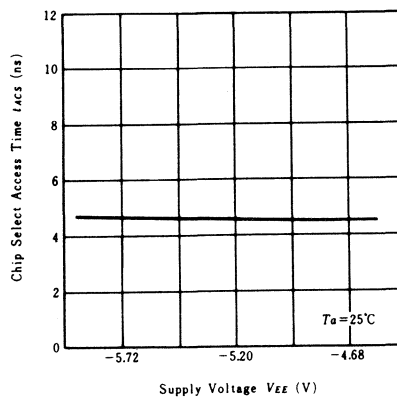
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



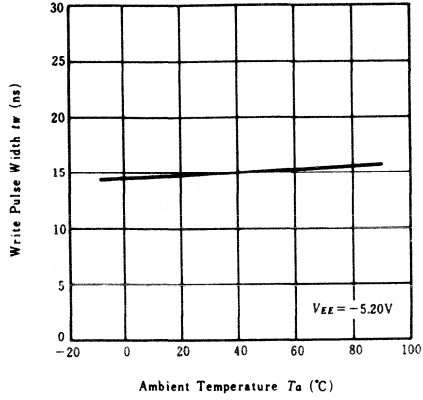
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



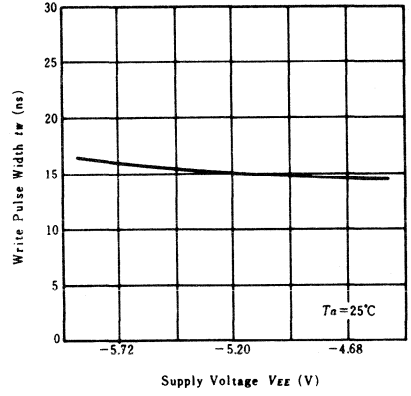
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



**WRITE PULSE WIDTH vs.
AMBIENT TEMPERATURE**



**WRITE PULSE WIDTH vs.
SUPPLY VOLTAGE**



HM10474-8, HM10474-10

1024-word × 4-bit Fully Decoded Random Access Memory

The HM10474 is ECL 10k compatible, 1024-words × 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10474 is encapsulated in cerdip-24pin package, compatible with Fairchild's F10474.

FEATURES

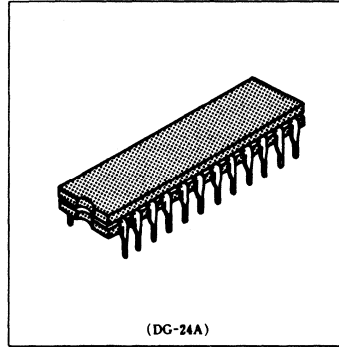
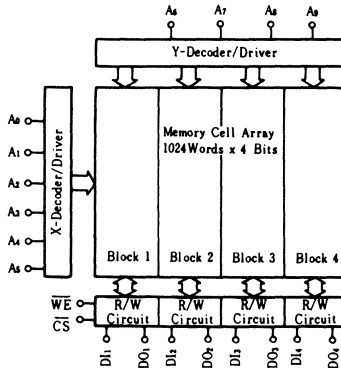
- 1024-word × 4-bit organization
- Fully compatible with 10K ECL level
- Address access time: HM10474-8 8ns (max)
HM10474-10 10ns (max)
- Write pulse width: HM10474-8 5ns (min)
HM10474-10 5ns (min)
- Low power dissipation: 0.3mW/bit
- Output obtainable by wired-OR (open emitter)

TRUTH TABLE

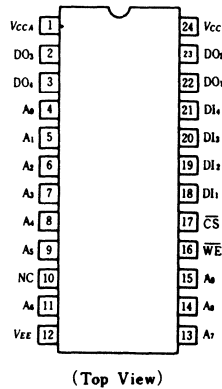
Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant
* : Read Out Noninvert

BLOCK DIAGRAM



PIN ARRANGEMENT



ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{iA}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit						
Output Voltage	V_{OH}	$V_{IN} = V_{IH\bar{A}}$ or $V_{IL\bar{B}}$		0°C	-1000	—	-840	mV					
				+25°C	-960	—	-810						
				+75°C	-900	—	-720						
	V_{OL}			0°C	-1870	—	-1665						
				+25°C	-1850	—	-1650						
				+75°C	-1830	—	-1625						
Output Threshold Voltage	$V_{OH\bar{C}}$	$V_{IN} = V_{IH\bar{B}}$ or $V_{IL\bar{A}}$		0°C	-1020	—	—	mV					
				+25°C	-980	—	—						
				+75°C	-920	—	—						
	$V_{OL\bar{C}}$			0°C	—	—	-1645						
				+25°C	—	—	-1630						
				+75°C	—	—	-1605						
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	-1145	—	-840	mV					
				+25°C	-1105	—	-810						
				+75°C	-1045	—	-720						
	V_{IL}			Guaranteed Input Voltage Low for All Inputs		0°C	-1870		—	-1490			
						+25°C	-1850		—	-1475			
						+75°C	-1830		—	-1450			
Input Current	I_{IH}	$V_{IN} = V_{IH\bar{A}}$				0 to +75°C		—	—	220	μA		
						I_{IL}	\bar{CS}	$V_{IN} = V_{IL\bar{B}}$	0 to +75°C			0.5	—
	Others						0 to +75°C		-50	—		—	
	Supply Current			I_{EE}	All Input and Output Open, Test Pin 12		$T_a = 0^\circ C$	-240	-220	—		mA	
$T_a = 75^\circ C$		—	-205				—						

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	6	ns
Address Access Time	t_{AA}		—	—	8	—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM10474-8			HM10474-10			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_w	$t_{WSA} = 2ns$	5	—	—	5	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	2	—	—	ns
Address Setup Time	t_{WSA}	$t_w = t_{wmin}$	2	—	—	2	—	—	ns
Address Hold Time	t_{WHA}		1	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	2	—	—	ns
Chip Select Hold Time	t_{WNCS}		1	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	6	ns
Write Recovery Time	t_{WR}		—	—	9	—	—	12	ns

3. RISE/FALL TIME

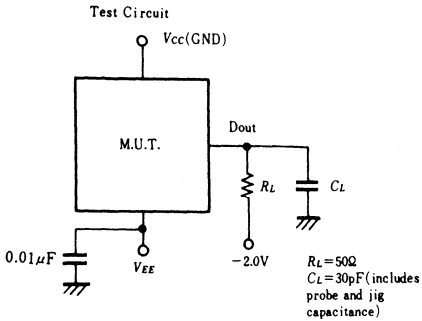
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

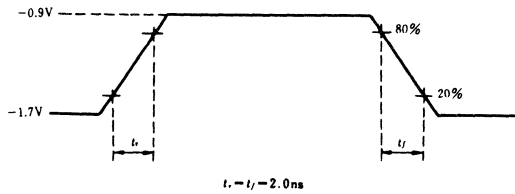
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

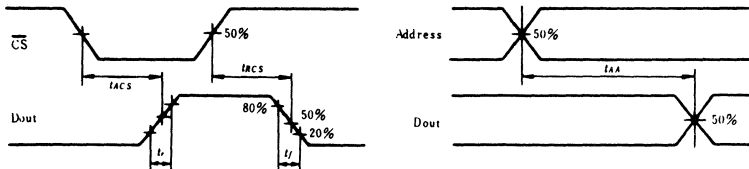
1. LOADING CONDITION



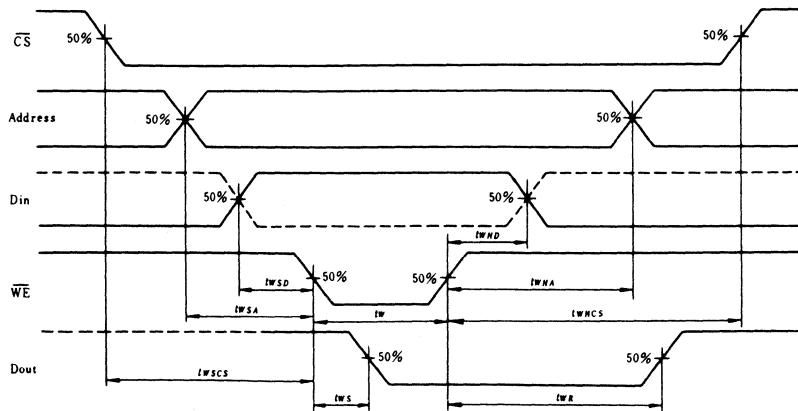
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM10470, HM10470-1

4096-word x 1-bit Fully Decoded Random Access Memory
 The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.

■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time:

HM10470	25ns (max)
HM10470-1	15ns (max)
- Write pulse width:

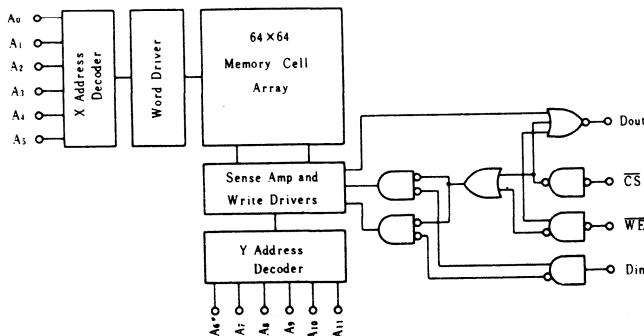
HM10470	25ns (min)
HM10470-1	15ns (min)
- Low power dissipation: 0.2mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant
 * : Read Out Noninvert

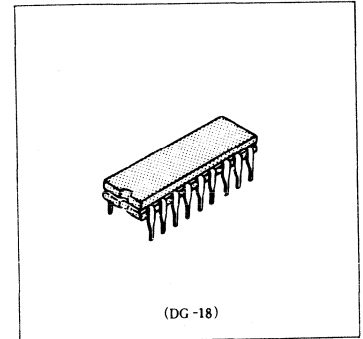
■ BLOCK DIAGRAM



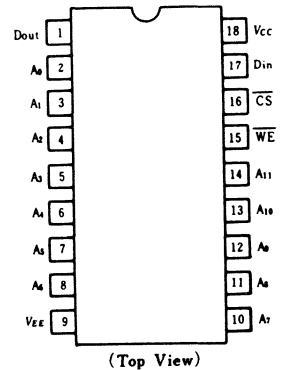
■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias



■ PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit					
Output Voltage	V_{OH}	$V_{IN} = V_{IH A}$ or $V_{IL B}$		0°C	-1000	-	-840	mV				
				+25°C	-960	-	-810					
				+75°C	-900	-	-720					
	V_{OL}			0°C	-1870	-	-1665					
				+25°C	-1850	-	-1650					
				+75°C	-1830	-	-1625					
Output Threshold Voltage	$V_{OH C}$	$V_{IN} = V_{IH B}$ or $V_{IL A}$		0°C	-1020	-	-	mV				
				+25°C	-980	-	-					
				+75°C	-920	-	-					
	$V_{OL C}$			0°C	-	-	-1645					
				+25°C	-	-	-1630					
				+75°C	-	-	-1605					
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	-1145	-	-840	mV				
				+25°C	-1105	-	-810					
				+75°C	-1045	-	-720					
	V_{IL}			Guaranteed Input Voltage Low for All Inputs		0°C	-1870		-	-1490		
						+25°C	-1850		-	-1475		
						+75°C	-1830		-	-1450		
Input Current	I_{IH}	$V_{IN} = V_{IH A}$				0 to +75°C		-	220	μA		
						I_{IL}	$V_{IN} = V_{IL B}$		CS		0.5	170
	Other								-50		-	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 9		Ta = 0°C		-200*			-160*	-		
				Ta = 75°C		-280**	-200**	-				
						-	-145	-				

* HM10470

** HM10470-1

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

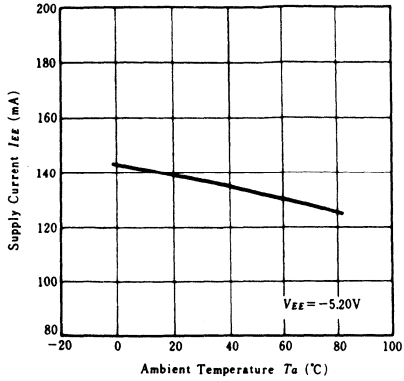
1. READ MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		-	-	10	-	-	8	ns
Chip Select Recovery Time	t_{RCS}		-	-	10	-	-	8	ns
Address Access Time	t_{AA}		-	15	25	-	12	15	ns

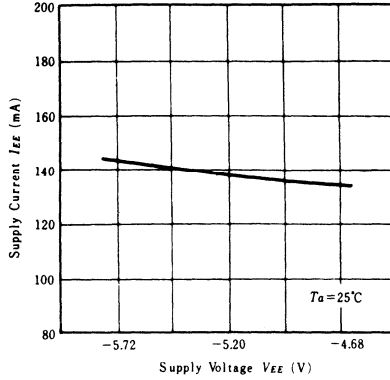
2. WRITE MODE

Item	Symbol	Test Condition	HM10470			HM10470-1			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_w	$t_{WSA} = 3ns$	25	-	-	15	-	-	ns
Data Setup Time	t_{WSD}		2	-	-	2	-	-	ns
Data Hold Time	t_{WHD}		2	-	-	2	-	-	ns
Address Setup Time	t_{WSA}		$t_w = t_{Wmin}$	3	-	-	3	-	-
Address Hold Time	t_{WHA}		2	-	-	2	-	-	ns
Chip Select Setup Time	t_{WSCS}		2	-	-	2	-	-	ns
Chip Select Hold Time	t_{WHCS}		2	-	-	2	-	-	ns
Write Disable Time	t_{WSD}		-	-	10	-	-	8	ns
Write Recovery Time	t_{WR}		-	-	27	-	-	17	ns

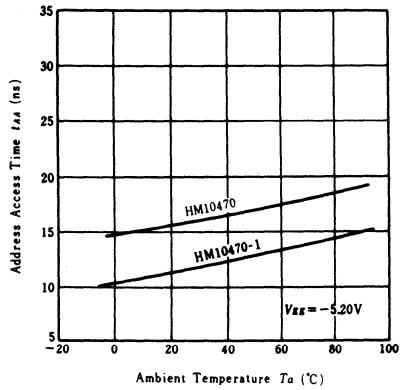
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



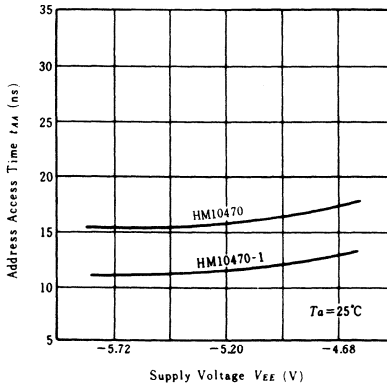
SUPPLY CURRENT vs. SUPPLY VOLTAGE



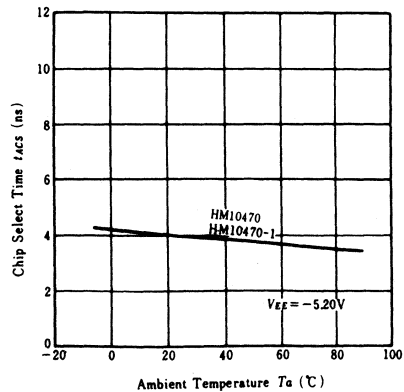
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



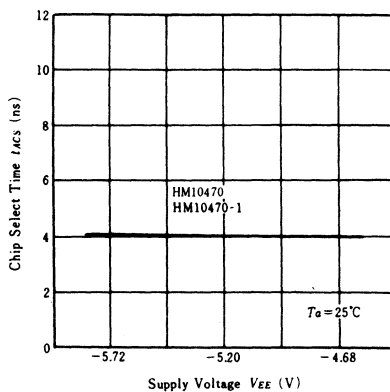
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



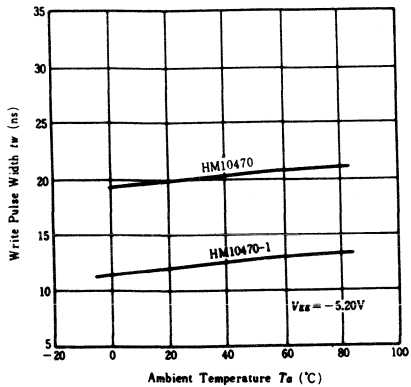
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



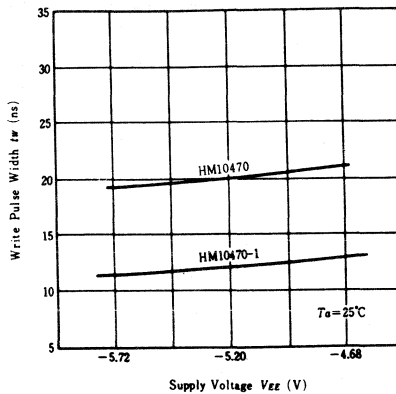
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



WRITE PULSE WIDTH vs. AMBIENT TEMPERATURE



WRITE PULSE WIDTH vs. SUPPLY VOLTAGE



HM10470-20

4096-word × 1-bit Fully Decoded Random Access Memory

The HM10470 is ECL 10K compatible, 4096-words x 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10470 is encapsulated in cerdip-18 pin package, compatible with Fairchild's F10470.

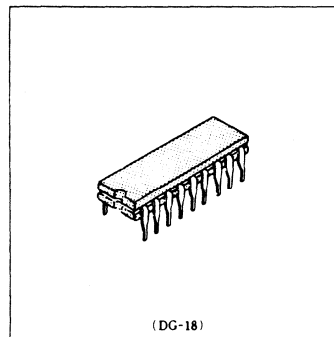
■ FEATURES

- 4096-word x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 20ns (max)
- Write pulse width: 20ns (min)
- Low power dissipation: 0.25 mW/bit
- Output obtainable by wired-OR (open emitter)

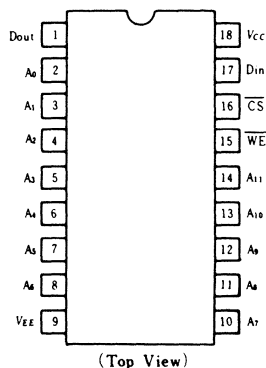
■ TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

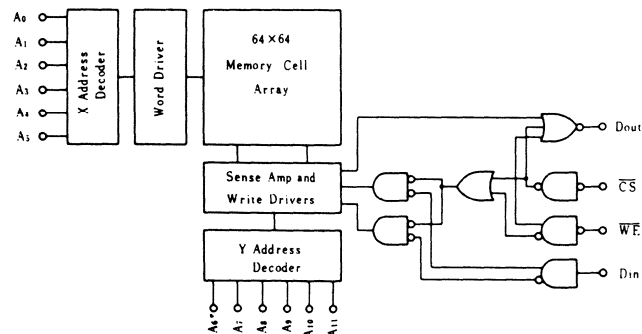
Notes) × : Irrelevant
* : Read Out Noninvert



■ PIN ARRANGEMENT



■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min (B)	typ	max (A)	Unit			
Output Voltage	V_{OH}	$V_{IN} = V_{INA}$ or V_{ILB}		0°C	-1000	-	-840	mV		
				+25°C	-960	-	-810			
				+75°C	-900	-	-720			
	V_{OL}			0°C	-1870	-	-1665			
				+25°C	-1850	-	-1650			
				+75°C	-1830	-	-1625			
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{INB}$ or V_{ILA}		0°C	-1020	-	-	mV		
				+25°C	-980	-	-			
				+75°C	-920	-	-			
	V_{OLC}			0°C	-	-	-1645			
				+25°C	-	-	-1630			
				+75°C	-	-	-1605			
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	-1145	-	-840	mV		
				+25°C	-1105	-	-810			
				+75°C	-1045	-	-720			
	V_{IL}			Guaranteed Input Voltage Low for All Inputs		0°C	-1870		-	-1490
						+25°C	-1850		-	-1475
						+75°C	-1830		-	-1450
Input Current	I_{IN}	$V_{IN} = V_{INA}$	0 to +75°C			-	-	220	μA	
	I_{IL}	\overline{CS}	$V_{IN} = V_{ILB}$			0 to +75°C	0.5	-		170
		Other				0 to +75°C	-50	-		-
Supply Current	I_{EE}	All Input and Output Open, Test Pin 12		$T_a = 0^\circ C$	-260	-220	-	mA		
				$T_a = 75^\circ C$	-	-210	-			

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		-	-	8	ns
Chip Select Recovery Time	t_{RCS}		-	-	8	ns
Address Access Time	t_{AA}		-	-	20	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA} = 3ns$	20	-	-	ns
Data Setup Time	t_{WBD}		3	-	-	ns
Data Hold Time	t_{WHD}		2	-	-	ns
Address Setup Time	t_{WSA}		$t_W = 20ns$	3	-	-
Address Hold Time	t_{WHA}		2	-	-	ns
Chip Select Setup Time	t_{WSCS}		3	-	-	ns
Chip Select Hold Time	t_{WNCS}		2	-	-	ns
Write Disable Time	t_{WS}		-	-	8	ns
Write Recovery Time	t_{WR}		-	-	22	ns

3. RISE/FALL TIME

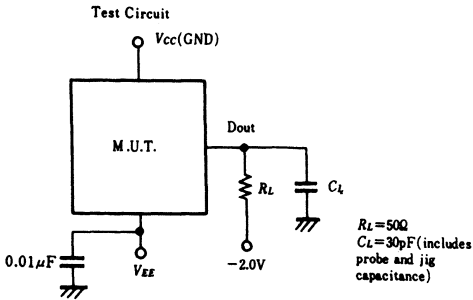
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

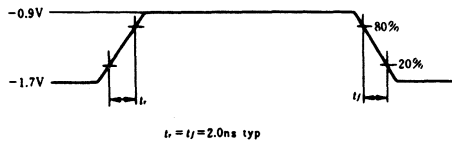
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

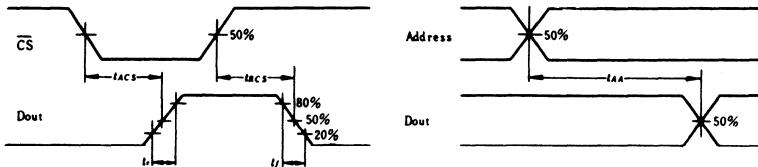
1. LOADING CONDITION



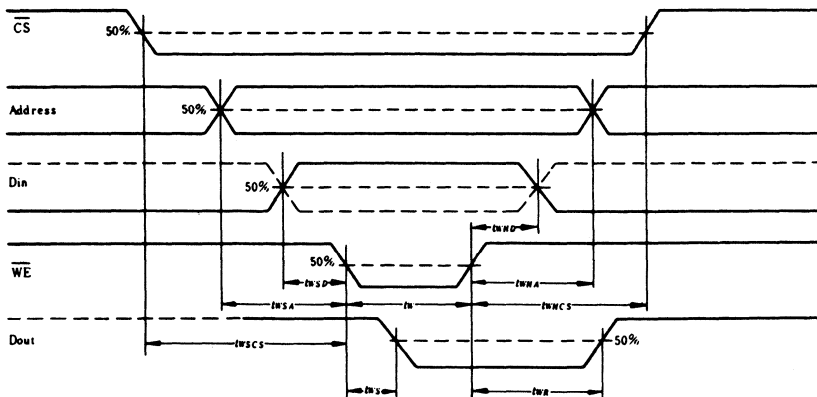
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM2142

4096-words × 1-bit Very High Speed Random Access Memory

The HM2142 is 4096-words x 1-bit very high speed read/write, random access memory developed for high speed systems such as pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM2142 is encapsulated in cerdip-20 pin package.

FEATURES

- 4096-words x 1 bit organization
- Very high speed address access time: 10ns (max)
- Write pulse width: 10ns (min)
- Power dissipation: 0.3 mW/bit
- Output obtainable by wired-OR

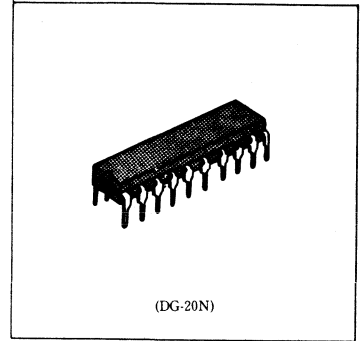
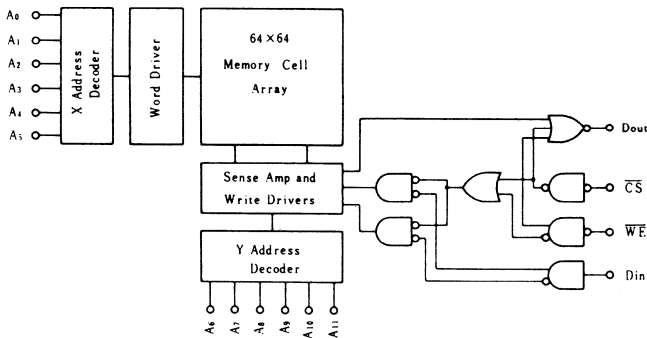
TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout *	Read

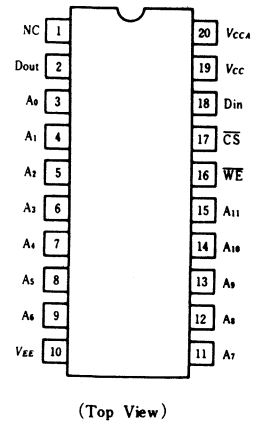
Notes) × : Irrelevant

* : Read Out Noninvert

BLOCK DIAGRAM



PIN ARRANGEMENT



■ ABSOLUTE MAXIMUM RATINGS ($T_a=25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	T_{stg} (Bias)*	-55 to +125	$^\circ\text{C}$

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE}=-5.2\text{V}$, $R_L=50\Omega$ to -2.0V , $T_a=0$ to $+75^\circ\text{C}$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit		
Output Voltage	V_{OH}	$V_{IN}=V_{INA}$ or V_{ILB}	0 $^\circ\text{C}$	-1000	—	-840	mV	
			+25 $^\circ\text{C}$	-980	—	-810		
			+75 $^\circ\text{C}$	-950	—	-720		
	V_{OL}		0 $^\circ\text{C}$	-1870	—	-1665		
			+25 $^\circ\text{C}$	-1850	—	-1650		
			+75 $^\circ\text{C}$	-1830	—	-1625		
Output Threshold Voltage	V_{OHC}	$V_{IN}=V_{INB}$ or V_{ILA}	0 $^\circ\text{C}$	-1020	—	—	mV	
			+25 $^\circ\text{C}$	-980	—	—		
			+75 $^\circ\text{C}$	-920	—	—		
	V_{OLC}		0 $^\circ\text{C}$	—	—	-1645		
			+25 $^\circ\text{C}$	—	—	-1630		
			+75 $^\circ\text{C}$	—	—	-1605		
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0 $^\circ\text{C}$	-1165	—	-880	mV	
			+25 $^\circ\text{C}$	-1165	—	-880		
			+75 $^\circ\text{C}$	-1165	—	-880		
	V_{IL}		0 $^\circ\text{C}$	-1810	—	-1560		
			+25 $^\circ\text{C}$	-1810	—	-1560		
			+75 $^\circ\text{C}$	-1810	—	-1560		
Input Current	I_{IH}	$V_{IN}=V_{INA}$	0 to +75 $^\circ\text{C}$	—	—	220	μA	
			I_{IL}	C S	0 to +75 $^\circ\text{C}$	0.5		—
	Others			-50		—		—
Supply Current	I_{EE}	All Input and Output Open.	$T_a=0^\circ\text{C}$	-270	-240	—	mA	
			$T_a=75^\circ\text{C}$	—	-220	—		

● AC CHARACTERISTICS ($V_{EE}=-5.2\text{V}\pm 5\%$, $T_a=0$ to $+75^\circ\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	6	ns
Chip Select Recovery Time	t_{RCS}		—	—	6	ns
Address Access Time	t_{AA}		—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{WSA}=3\text{ns}$	10	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	ns
Address Setup Time	t_{WSA}	$t_w=10\text{ns}$	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WCS}		1	—	—	ns
Chip Select Hold Time	t_{WCS}		1	—	—	ns
Write Disable Time	t_{WS}		—	—	6	ns
Write Recovery Time	t_{WR}		—	—	12	ns

3. RISE/FALL TIME

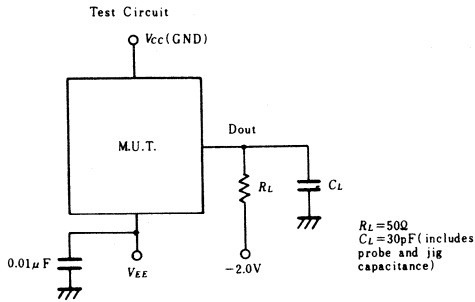
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

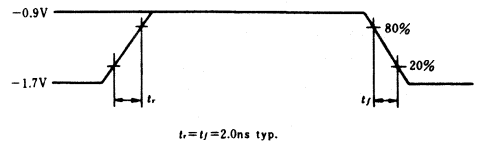
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

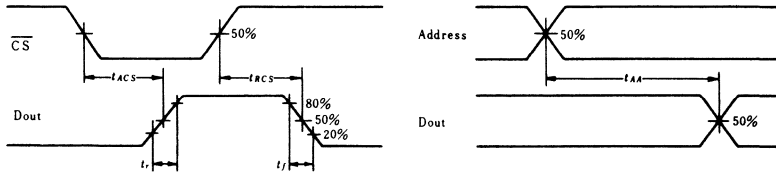
1. LOADING CONDITION



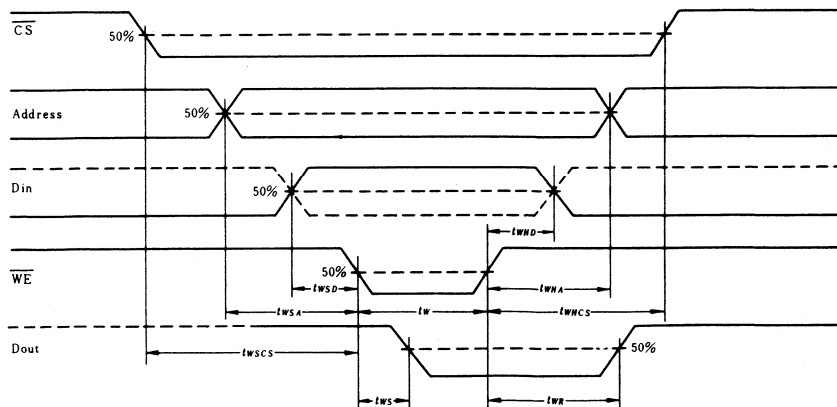
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM10480, HM10480F

16,384-words × 1-bit Fully Decoded Random Access Memory

The HM10480 is ECL 10K compatible, 16,384-words × 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

FEATURES

- 16,384-words × 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 25ns(min)
- Low power dissipation: 0.05mW/bit
- Output obtainable by wired-OR (open emitter)

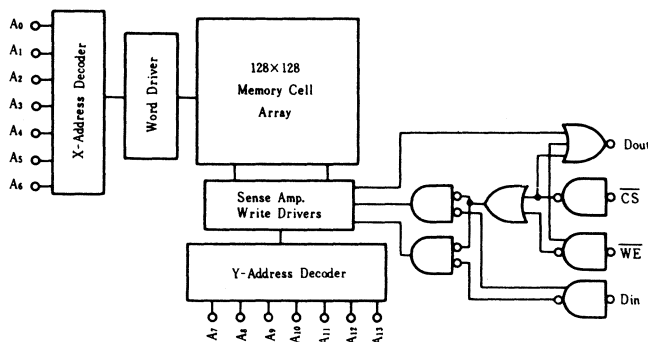
TRUTH TABLE

CS	Input		Output	Mode
	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant

* : Read Out Noninvert

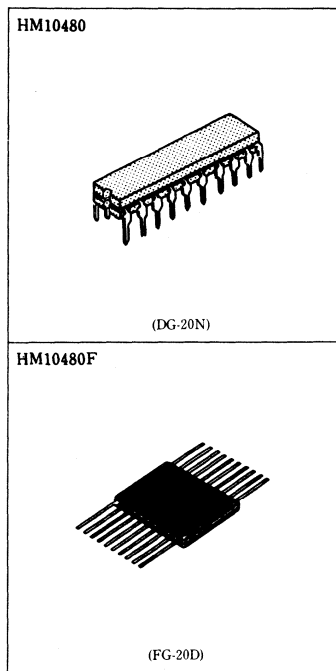
BLOCK DIAGRAM



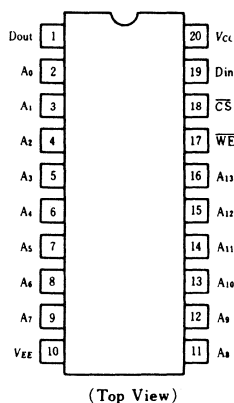
ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias



PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{IN} = V_{IH\bar{A}}$ or $V_{IL\bar{B}}$		0°C	-1000	-	-840	mV
				+25°C	-960	-	-810	
				+75°C	-900	-	-720	
	V_{OL}			0°C	-1870	-	-1665	
				+25°C	-1850	-	-1650	
				+75°C	-1830	-	-1625	
Output Threshold Voltage	V_{OHC}	$V_{IN} = V_{IH\bar{B}}$ or $V_{IL\bar{A}}$		0°C	-1020	-	-	mV
				+25°C	-980	-	-	
				+75°C	-920	-	-	
	V_{OLC}			0°C	-	-	-1645	
				+25°C	-	-	-1630	
				+75°C	-	-	-1605	
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	-1145	-	-840	mV
				+25°C	-1105	-	-810	
				+75°C	-1045	-	-720	
	V_{IL}			0°C	-1870	-	-1490	
				+25°C	-1850	-	-1475	
				+75°C	-1830	-	-1450	
Input Current	I_{IH}	$V_{IN} = V_{IH\bar{A}}$	$V_{IN} = V_{IL\bar{B}}$	0 to +75°C	-	-	220	μA
	I_{IL}	\overline{CS}		0 to +75°C	0.5	-	170	
		Others		0 to +75°C	-50	-	-	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10		$T_a = 0^\circ C$	-200	-140	-	mA
				$T_a = 75^\circ C$	-	-130	-	

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	-	15	ns
Chip Select Recovery Time	t_{RCS}		2	-	15	ns
Address Access Time	t_{AA}		3	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{WSA} = 5ns$	25	-	-	ns
Data Setup Time	t_{WSD}		5	-	-	ns
Data Hold Time	t_{WHD}		5	-	-	ns
Address Setup Time	t_{WSA}		$t_w = 25ns$	5	-	-
Address Hold Time	t_{WHA}		5	-	-	ns
Chip Select Setup Time	t_{WSCS}		5	-	-	ns
Chip Select Hold Time	t_{WHCS}		5	-	-	ns
Write Disable Time	t_{WS}		-	-	15	ns
Write Recovery Time	t_{WR}		-	-	30	ns

HM10480-15, HM10480F-15

16,384-words × 1-bit Fully Decoded Random Access Memory

The HM10480 is ECL 10K compatible, 16,384-words × 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM10480 is encapsulated in cerdip-20 pin and flat 20-pin package, compatible with Fairchild's F10480.

FEATURES

- 16,384-words × 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 15ns (max)
- Write pulse width: 15ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

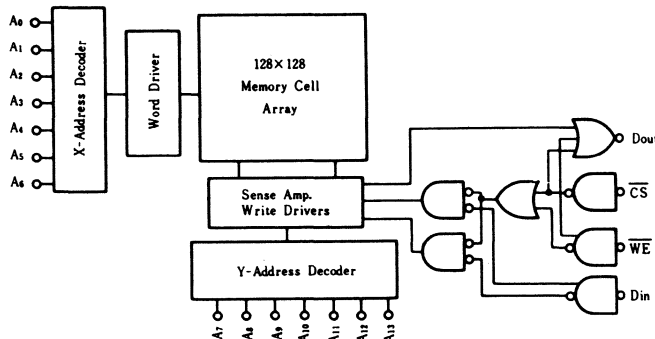
TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	x	x	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	x	Dout*	Read

Notes) x : Irrelevant

* : Read Out Noninvert

BLOCK DIAGRAM

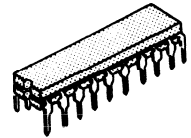


ABSOLUTE MAXIMUM RATINGS (Ta = 25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	$V_{i\alpha}$	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	°C

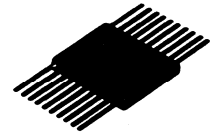
* Under Bias

HM10480-15



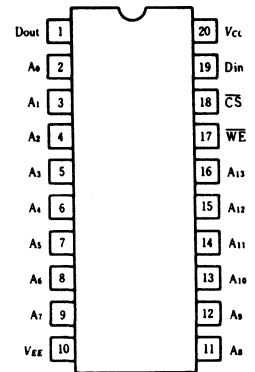
(DG-20N)

HM10480F-15



(FG-20D)

PIN ARRANGEMENT



(Top View)

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit		
Output Voltage	V_{OH}	$V_{IN} = V_{IH}$ or V_{IL}	0°C	-1000	—	-840	mV	
			+25°C	-960	—	-810		
			+75°C	-900	—	-720		
	V_{OL}		0°C	-1870	—	-1665		
			+25°C	-1850	—	-1650		
			+75°C	-1830	—	-1625		
Output Threshold Voltage	V_{OHc}	$V_{IN} = V_{IH}$ or V_{IL}	0°C	-1020	—	—	mV	
			+25°C	-980	—	—		
			+75°C	-920	—	—		
	V_{OLc}		0°C	—	—	-1645		
			+25°C	—	—	-1630		
			+75°C	—	—	-1605		
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs	0°C	-1145	—	-840	mV	
			+25°C	-1105	—	-810		
			+75°C	-1045	—	-720		
	V_{IL}		0°C	-1870	—	-1490		
			+25°C	-1850	—	-1475		
			+75°C	-1830	—	-1450		
Input Current	I_{IH}	$V_{IN} = V_{IH}$	0 to +75°C	—	—	220	μA	
				I_{IL}	\overline{CS}	0 to +75°C		0.5
	Others		$V_{IN} = V_{IL}$		-50			—
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10	$T_a = 0^\circ C$	-240	-220	—	mA	
			$T_a = 75^\circ C$	—	-200	—		

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	8	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	ns
Address Access Time	t_{AA}		3	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{WSA} = 3ns$	15	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		3	—	—	ns
Address Setup Time	t_{WSA}	$t_w = 15ns$	3	—	—	ns
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		3	—	—	ns
Chip Select Hold Time	t_{WHCS}		3	—	—	ns
Write Disable Time	t_{WS}		—	—	12	ns
Write Recovery Time	t_{WR}		—	—	17	ns

3. RISE/FALL TIME

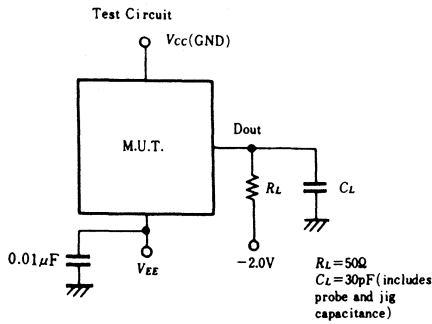
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

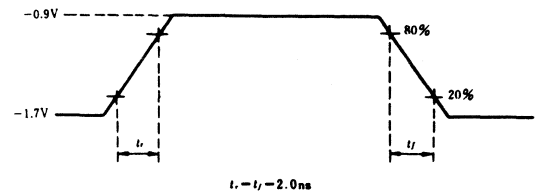
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

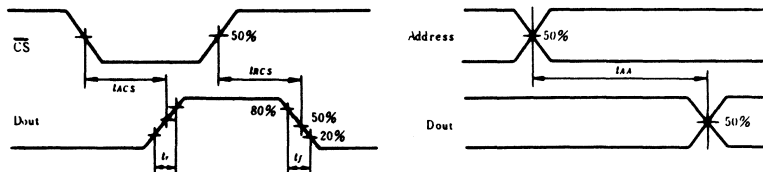
1. LOADING CONDITION



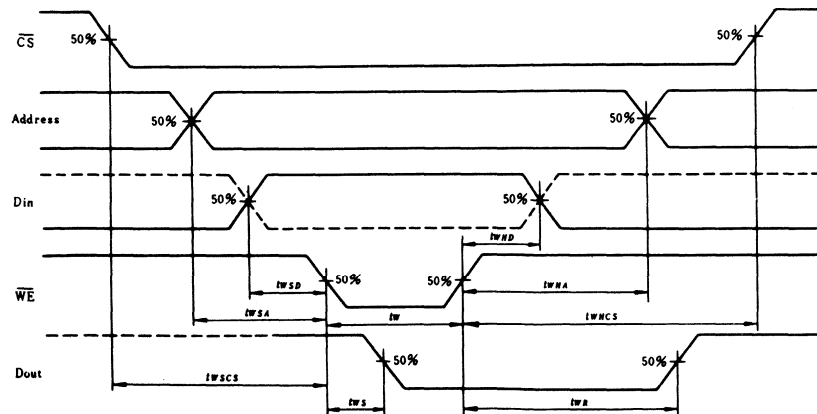
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM10480L

16,384-words X 1-bit Fully Decoded Random Access Memory

The HM10480L is ECL 10K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed and low power systems such as control/buffer and main storages.

The HM10480L is encapsulated in cerdip-20 pin package.

■ FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 10K ECL level
- Address access time: 25ns (max)
- Write pulse width: 20ns (min)
- Low power dissipation: Standby 220mW (typ.), Operation 350mW (typ.)
- Output obtainable by wired-OR (open emitter)

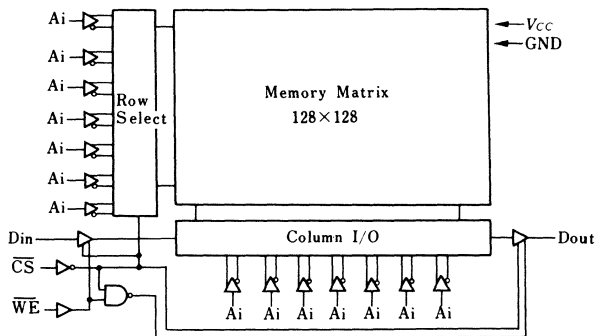
■ TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant

* : Read Out Noninvert

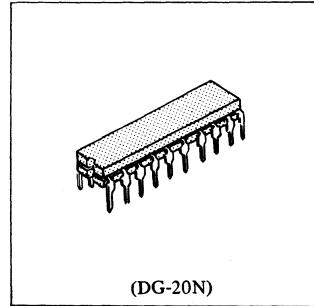
■ BLOCK DIAGRAM



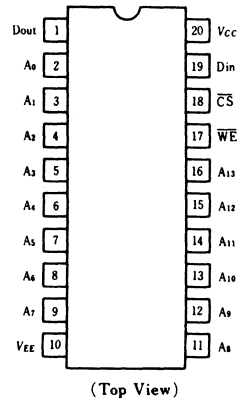
■ ABSOLUTE MAXIMUM RATINGS (Ta=25°C)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	°C
Storage Temperature	$T_{stg}(Bias)^*$	-55 to +125	°C

* Under Bias



■ PIN ARRANGEMENT



■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -5.2V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition		min(B)	typ	max(A)	Unit				
Output Voltage	V_{OH}	$V_{IN} = V_{INA}$ or V_{ILB}		0°C	-1000	—	-840	mV			
				+25°C	-960	—	-810				
				+75°C	-900	—	-720				
	V_{OL}			0°C	-1870	—	-1665				
				+25°C	-1850	—	-1650				
				+75°C	-1830	—	-1625				
Output Threshold Voltage	V_{OHc}	$V_{IN} = V_{INB}$ or V_{ILc}		0°C	-1020	—	—	mV			
				+25°C	-980	—	—				
				+75°C	-920	—	—				
	V_{OLc}			0°C	—	—	-1645				
				+25°C	—	—	-1630				
				+75°C	—	—	-1605				
Input Voltage	V_{IH}	Guaranteed Input Voltage High for All Inputs		0°C	-1145	—	-840	mV			
				+25°C	-1105	—	-810				
				+75°C	-1045	—	-720				
	V_{IL}			0°C	-1870	—	-1490				
				+25°C	-1850	—	-1475				
				+75°C	-1830	—	-1450				
Input Current	I_{IH}	$V_{IN} = V_{INA}$		0 to +75°C		—	—	220	μA		
				I_{IL}	\overline{CS}	$V_{IN} = V_{ILB}$	0 to +75°C			0.5	—
	Others				0 to +75°C		-50	—		—	
Supply Current	I_{EE}	All Input and Output Open, Test Pin 10		$T_a = 0^\circ C$		—	-70	-120	mA		
				$T_a = 75^\circ C$		—	-61	-110			

● AC CHARACTERISTICS ($V_{EE} = -5.2V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	15	25	ns
Chip Select Recovery Time	t_{RCS}		—	9	25	ns
Address Access Time	t_{AA}		3	17	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{wSA} = 3ns$	20	—	—	ns
Data Setup Time	t_{wSD}		3	—	—	ns
Data Hold Time	t_{wHD}		2	—	—	ns
Address Setup Time	t_{wSA}	$t_w = 20ns$	3	—	—	ns
Address Hold Time	t_{wHA}		2	—	—	ns
Chip Select Setup Time	t_{wSCS}		3	—	—	ns
Chip Select Hold Time	t_{wHCS}		2	—	—	ns
Write Disable Time	t_{wS}		—	—	10	ns
Write Recovery Time	t_{wR}		—	—	25	ns

3. RISE/FALL TIME

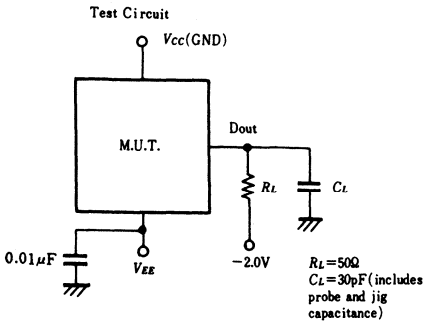
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

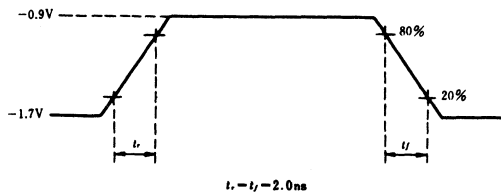
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	5	—	pF
Output Capacitance	C_{out}		—	6.5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

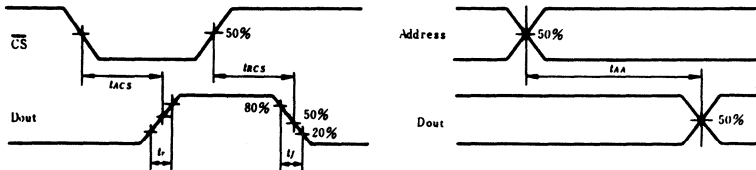
1. LOADING CONDITION



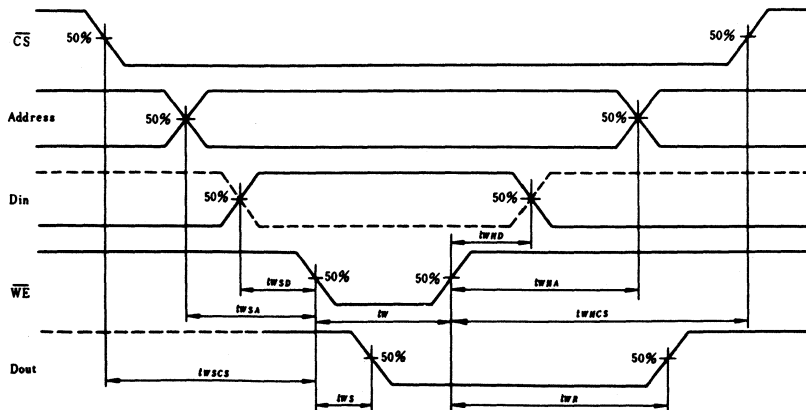
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100422, HM100422F HM100422CG

256-word × 4-bit Fully Decoded Random Access Memory

The HM100422 is ECL 100K compatible, 256-word × 4-bit, read write, random access memory developed for high speed system such as scratch pads and control/buffer storages.

Four active Low Block Select lines are provided to select each block independently.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100422 is encapsulated in cerdip-24pin package, or 24pin flat package compatible with Fairchild's F100422.

■ FEATURES

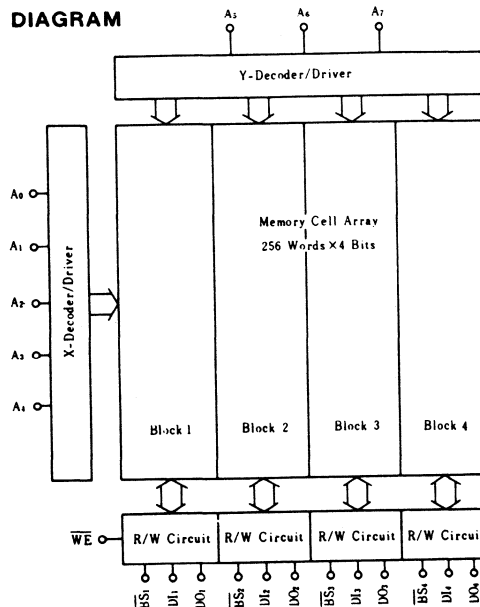
- 256-word × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 10ns (max.)
- Minimum write pulse width: 6ns (min.)
- Low power dissipation: 0.8mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

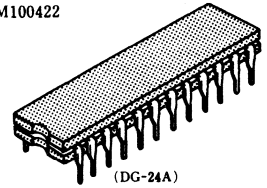
Input			Output	Mode
\overline{BS}	\overline{WE}	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM

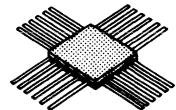


HM100422



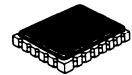
(DG-24A)

HM100422F



(FG-24)

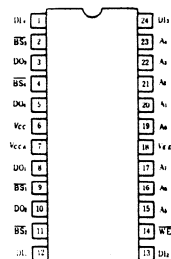
HM100422CG



(CG-24)

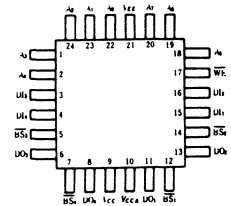
■ PIN ARRANGEMENT

● HM100422



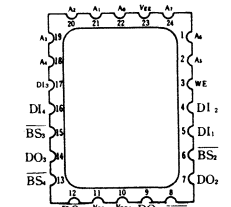
(Top View)

● HM100422F



(Top View)

● HM100422CG



(Top View)

■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{iA}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -4.5\text{V}$, $R_L = 50\Omega$ to -2.0V , $T_a = 0$ to $+85^\circ\text{C}$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit
Output Voltage	V_{OH}	$V_{iA} = V_{iNA}$ or V_{iLB}	-1025	-955	-880	mV
	V_{OL}		-1810	-1715	-1620	mV
Output Threshold Voltage	V_{OHC}	$V_{iA} = V_{iNB}$ or V_{iLA}	-1035	—	—	mV
	V_{OLC}		—	—	-1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage	-1165	—	-880	mV
	V_{iL}	High/Low for All Inputs	-1810	—	-1475	mV
Input Current	I_{IH}	$V_{iA} = V_{iNA}$	—	—	220	μA
	I_{iL}	$V_{iA} = V_{iLB}$				
		BS	0.5	—	170	μA
		Others	-50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open	-200	-165	—	mA

● AC CHARACTERISTICS ($V_{EE} = -4.5\text{V} \pm 5\%$, $T_a = 0$ to $+85^\circ\text{C}$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Block Select Access Time	t_{ABS}		—	—	6	ns
Block Select Recovery Time	t_{RBS}		—	—	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA} = 2\text{ns}$	6	4.5	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}		$t_W = 6\text{ns}$	2	0	—
Address Hold Time	t_{WHA}		2	0	—	ns
Block Select Setup Time	t_{WSBS}		2	0	—	ns
Block Select Hold Time	t_{WHBS}		2	0	—	ns
Write Disable Time	t_{WSD}		—	4	6	ns
Write Recovery Time	t_{WR}		—	4.5	12	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{iA}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

HM100415, HM100415CG

1024-word × 1-bit Fully Decoded Random Access Memory

The HM100415 is a 1024-word x 1-bit, read/write random access memory developed for application to scratch pads, control and buffer storages which require very high speeds.

The HM100415 is compatible with the HD100K families and includes on-chip voltage and temperature compensation for improved noise margin. This memory is encapsulated in cerdip-16pin package.

■ FEATURES

- Level 100K ECL Compatible
- Organization 1024-word by 1-bit
- Address Access Time 10ns (max)
- Chip Select Access Time 5ns (max.)
- Power Consumption 0.6mW/bit (typ)
- Output Obtainable by Wired-OR (open emitter)
- Compatible with Fairchild F100415.

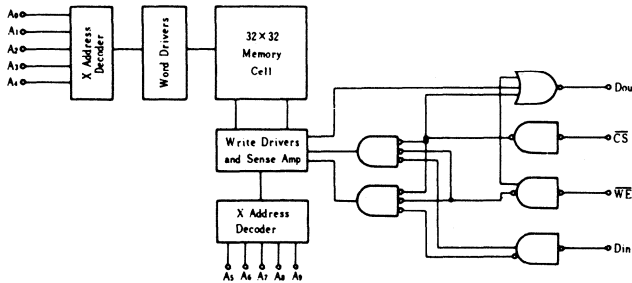
■ TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant

* : Read Out Noninvert

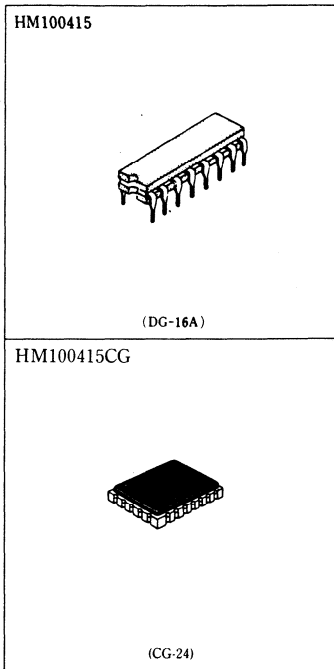
■ BLOCK DIAGRAM



■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

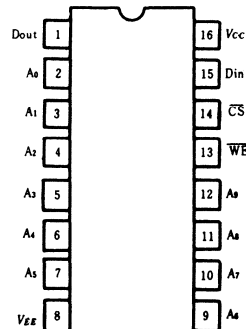
Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias



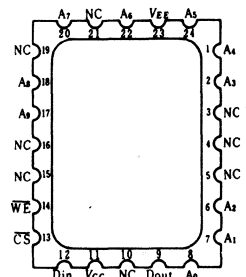
■ PIN ARRANGEMENT

● HM100415



(Top View)

● HM100415CG



(Top View)

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -4.5V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{in} = V_{iNA}$ or V_{iLB}	-1025	-955	-880	mV	
	V_{OL}		-1810	-1715	-1620	mV	
Output Threshold Voltage	V_{OHc}	$V_{in} = V_{iNB}$ or V_{iLA}	-1035	—	—	mV	
	V_{OLc}		—	—	-1610	mV	
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs	-1165	—	-880	mV	
	V_{iL}		-1810	—	-1475	mV	
Input Current	I_{iN}	$V_{in} = V_{iNA}$	—	—	220	μA	
	I_{iL}	$V_{in} = V_{iLB}$	\overline{CS}	0.5	—	170	μA
			Others	-50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open	-200	-150	—	mA	

● AC CHARACTERISTICS ($V_{EE} = -4.5V \pm 5\%$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	3	5	ns
Chip Select Recovery Time	t_{RCS}		—	3	5	ns
Address Access Time	t_{AA}		—	7	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA} = 2ns$	6	4	—	ns
Data Setup Time	t_{WSD}		2	0	—	ns
Data Hold Time	t_{WHD}		2	0	—	ns
Address Setup Time	t_{WSA}		$t_W = 6ns$	2	0	—
Address Hold Time	t_{WHA}		2	0	—	ns
Chip Select Setup Time	t_{WSCS}		2	0	—	ns
Chip Select Hold Time	t_{WHCS}		2	0	—	ns
Write Disable Time	t_{WS}		—	3	5	ns
Write Recovery Time	t_{WR}		—	3	12	ns

3. RISE/FALL TIME

Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

HM100474, HM100474F

1024-word × 4-bit Fully Decoded Random Access Memory

The HM100474 is a 1024-words × 4-bit, read/write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100474 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-24-pin and flat 24pin package, compatible with Fairchild's F100474.

FEATURES

- 1024-word × 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns(min)
- Output obtainable by wired-OR (open emitter)

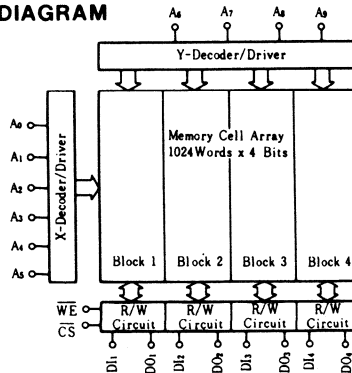
TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant

* : Read Out Noninvert

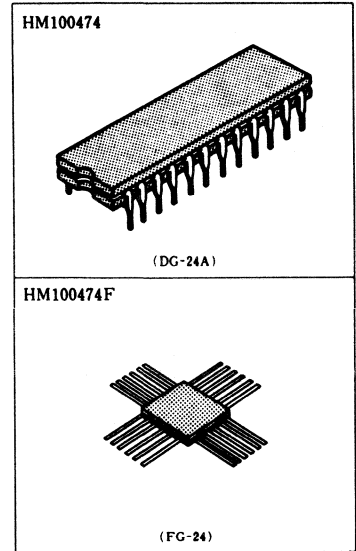
BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

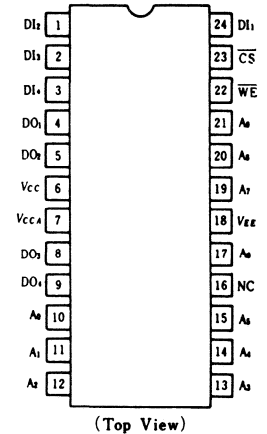
Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias



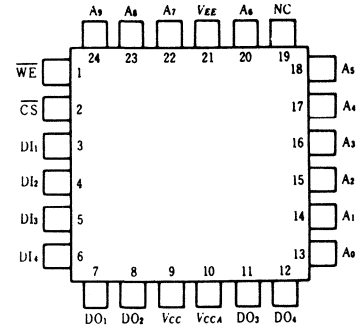
PIN ARRANGEMENT

HM100474



(Top View)

HM100474F



(Top View)

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -4.5V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max (A)	Unit
Output Voltage	V_{OH}	$V_{iA} = V_{iHA}$ or V_{iLB}	-1025	-955	-880	mV
	V_{OL}		-1810	-1715	-1620	mV
Output Threshold Voltage	V_{OHc}	$V_{iA} = V_{iHB}$ or V_{iLA}	-1035	—	—	mV
	V_{OLc}		—	—	-1610	mV
Input Voltage	V_{IH}	Guaranteed Input Voltage	-1165	—	-880	mV
	V_{iL}	High/Low for All Inputs	-1810	—	-1475	mV
Input Current	I_{IH}	$V_{iA} = V_{iHA}$	—	—	220	μA
	I_{iL}	$V_{iA} = V_{iLB}$	\overline{CS}	0.5	—	170
Others			-50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open	-200	-165	—	mA

● AC CHARACTERISTICS ($V_{EE} = -4.5V \pm 5\%$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	15	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{wSA} = 3ns$	25	15	—	ns
Data Setup Time	t_{wSD}		2	—	—	ns
Data Hold Time	t_{wHD}		2	—	—	ns
Address Setup Time	t_{wSA}	$t_w = t_{wmin}$	3	—	—	ns
Address Hold Time	t_{wHA}		2	—	—	ns
Chip Select Setup Time	t_{wSCS}		2	—	—	ns
Chip Select Hold Time	t_{wHCS}		2	—	—	ns
Write Disable Time	t_{wS}		—	—	10	ns
Write Recovery Time	t_{wR}		—	—	27	ns

3. RISE/FALL TIME

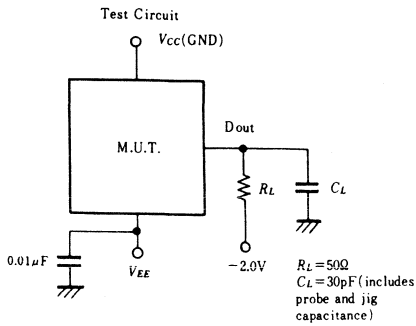
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

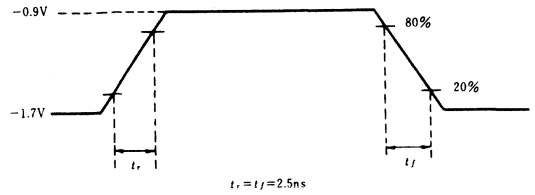
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{iA}		—	4	—	pF
Output Capacitance	C_{out}		—	7	—	pF

■ TEST CIRCUIT AND WAVEFORMS

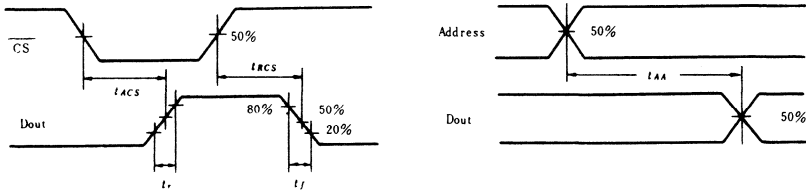
1. LOADING CONDITION



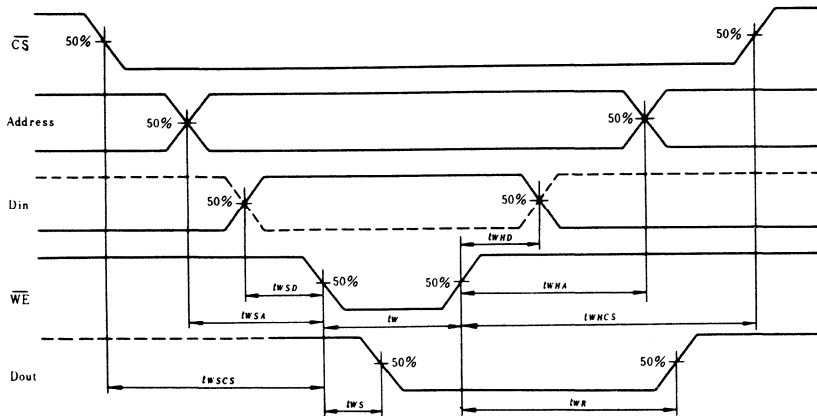
2. INPUT PULSE



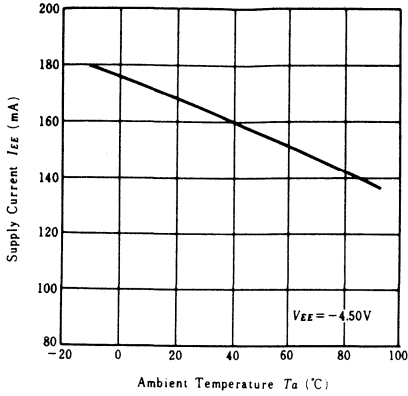
3. READ MODE



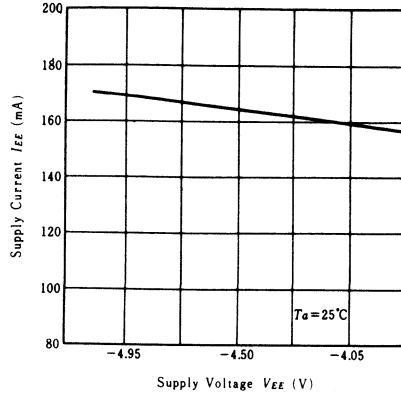
4. WRITE MODE



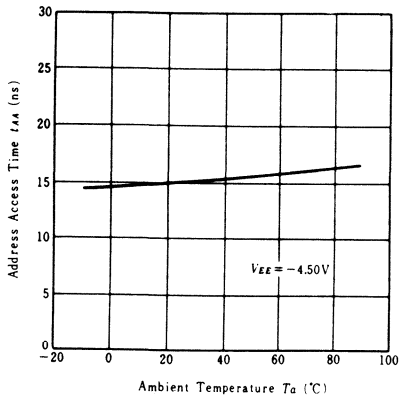
SUPPLY CURRENT vs. AMBIENT TEMPERATURE



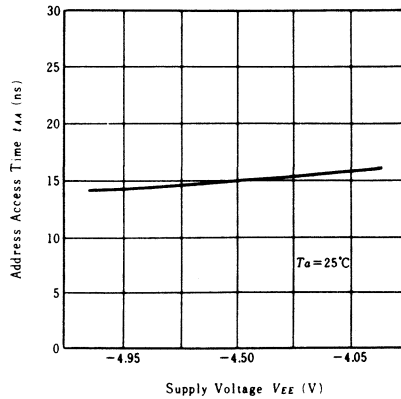
SUPPLY CURRENT vs. SUPPLY VOLTAGE



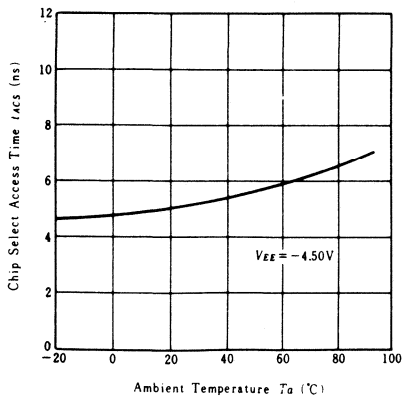
ADDRESS ACCESS TIME vs. AMBIENT TEMPERATURE



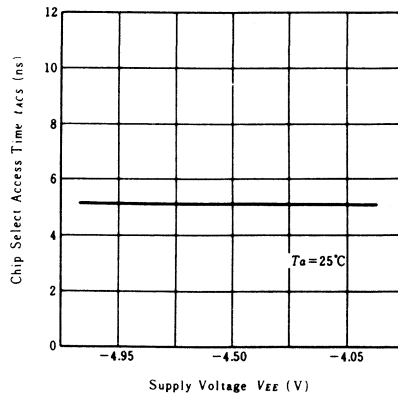
ADDRESS ACCESS TIME vs. SUPPLY VOLTAGE



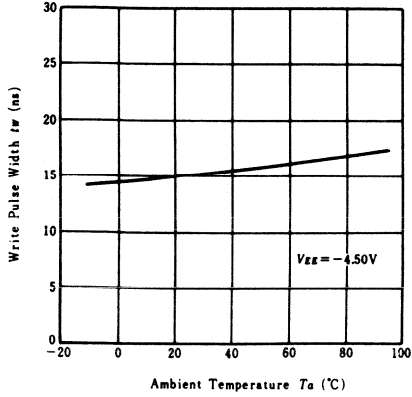
CHIP SELECT ACCESS TIME vs. AMBIENT TEMPERATURE



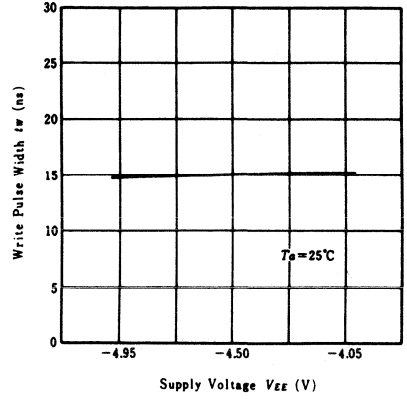
CHIP SELECT ACCESS TIME vs. SUPPLY VOLTAGE



**WRITE PULSE WIDTH vs.
AMBIENT TEMPERATURE**



**WRITE PULSE WIDTH vs.
SUPPLY VOLTAGE**



HM100474-8, HM100474-10 Preliminary HM100474F-8, HM100474F-10

1024-word × 4-bit Fully Decoded Random Access Memory

The HM100474 is ECL 100k compatible, 1024-words x 4-bit, read write, random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process is the Hitachi's U-groove isolation method. The HM100474 is encapsulated in cerdip-24 pin and flat 24 pin package, compatible with Fairchild's F100474.

■ FEATURES

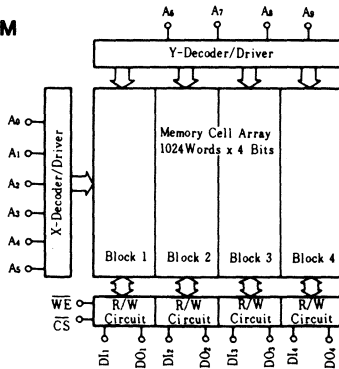
- 1024-word x 4-bit organization
- Fully compatible with 100K ECL level
- Address access time: HM100474-8 8ns (max)
HM100474-10 10ns (max)
- Write pulse width: HM100474-8 5ns (min)
HM100474-10 5ns (min)
- Low power dissipation: 0.3mW/bit
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	x	x	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	x	Dout*	Read

Notes) x : Irrelevant
* : Read Out Noninvert

■ BLOCK DIAGRAM

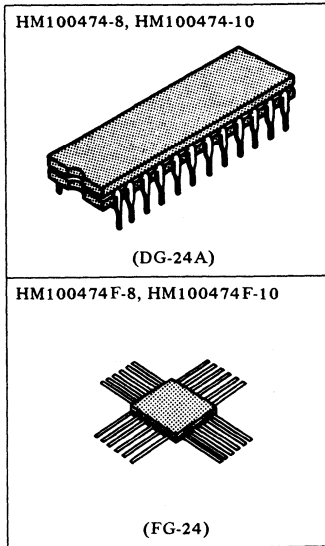


■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

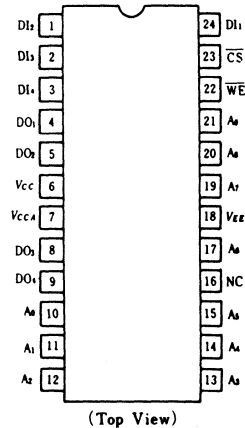
* Under Bias

Note) The specifications of this device are subject to change without notice. Please contact your nearest Hitachis Sales Dept, regarding specifications.

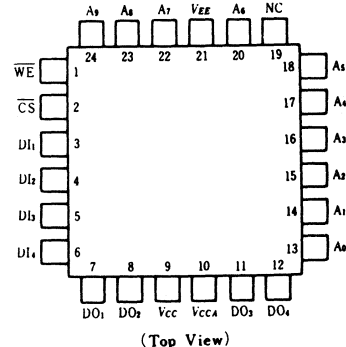


■ PIN ARRANGEMENT

- HM100474-8, HM100474-10



- HM100474F-8, HM100474F-10



■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -4.5V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{iA} - V_{iHA}$ or V_{iLB}	-1025	-955	-880	mV	
	V_{OL}		-1810	-1715	-1620	mV	
Output Threshold Voltage	V_{OHc}	$V_{iA} - V_{iHB}$ or V_{iLA}	-1035	—	—	mV	
	V_{OLc}		—	—	-1610	mV	
Input Voltage	V_{IH}	Guaranteed Input Voltage High/Low for All Inputs	-1165	—	-880	mV	
	V_{iL}		-1810	—	-1475	mV	
Input Current	I_{IH}	$V_{iA} - V_{iHA}$	—	—	220	μA	
	I_{iL}	$V_{iA} - V_{iLB}$	\overline{CS}	0.5	—	170	μA
			Others	-50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open	-240	-220	—	mA	

● AC CHARACTERISTICS ($V_{EE} = -4.5V \pm 5\%$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	HM100474/F-8			HM100474/F-10			Unit
			min	typ	max	min	typ	max	
Chip Select Access Time	t_{ACS}		—	—	6	—	—	6	s
Chip Select Recovery Time	t_{RCS}		—	—	6	—	—	6	ns
Address Access Time	t_{AA}		—	—	8	—	—	10	ns

2. WRITE MODE

Item	Symbol	Test Condition	HM100474/F-8			HM100474/F-10			Unit
			min	typ	max	min	typ	max	
Write Pulse Width	t_W	$t_{WSA} = 2ns$	5	—	—	5	—	—	ns
Data Setup Time	t_{WSD}		1	—	—	2	—	—	ns
Data Hold Time	t_{WHD}		1	—	—	2	—	—	ns
Address Setup Time	t_{WSA}		$t_W = t_W \text{ min}$	2	—	—	2	—	—
Address Hold Time	t_{WHA}		1	—	—	2	—	—	ns
Chip Select Setup Time	t_{WSCS}		1	—	—	2	—	—	ns
Chip Select Hold Time	t_{WHCS}		1	—	—	2	—	—	ns
Write Disable Time	t_{WS}		—	—	6	—	—	6	ns
Write Recovery Time	t_{WR}		—	—	9	—	—	12	ns

3. RISE/FALL TIME

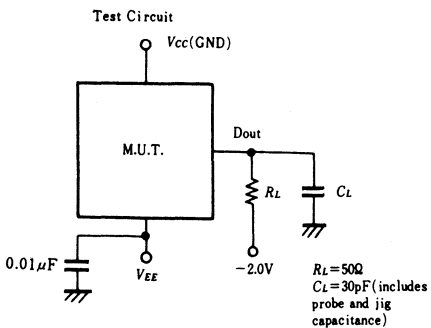
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

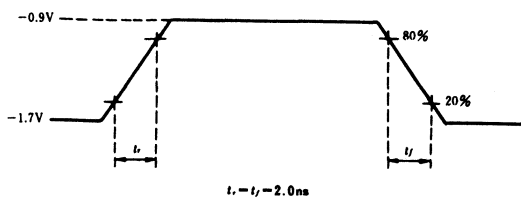
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{iA}		—	3	—	pF
Output Capacitance	C_{oA}		—	5	—	pF

TEST CIRCUIT AND WAVEFORMS

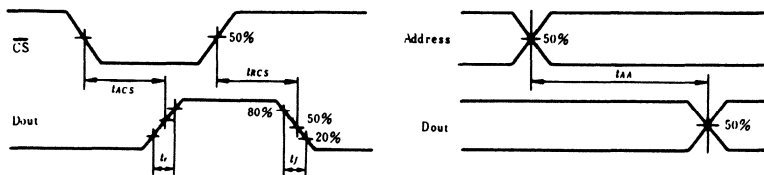
1. LOADING CONDITION



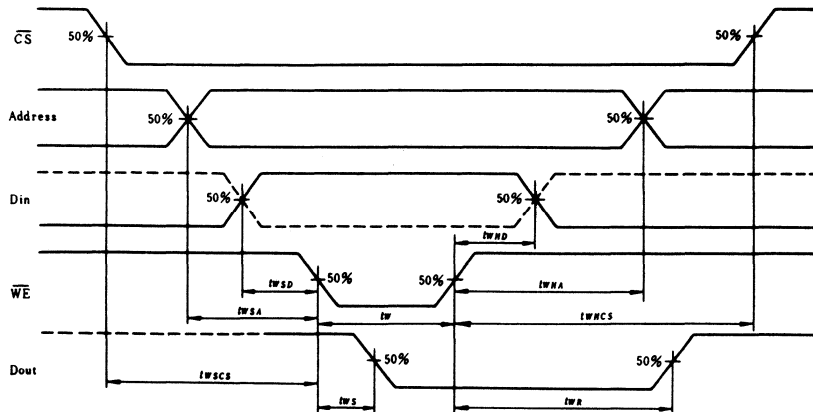
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100470

4096-word × 1-bit Fully Decoded Random Access Memory

The HM100470 is a 4096-words × 1-bit, read/write, random access memory developed for high speed systems such as scratch pads and control buffer storages.

The fabrication process is the Hitachi's low capacitance, oxide isolation method with double metalization.

The HM100470 is compatible with the HD100K ECL families and includes on-chip voltage and temperature compensation for improved noise margin. This device is encapsulated in cerdip-18pin package, compatible with Fairchild's F100470.

■ FEATURES

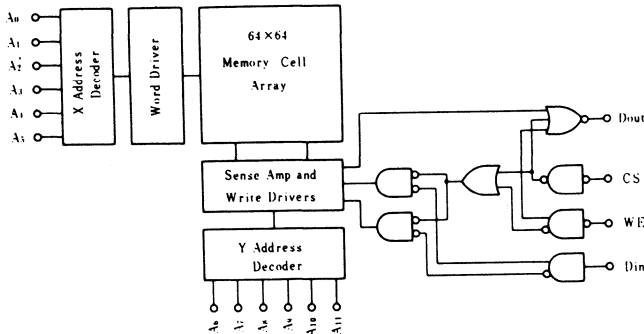
- 4096-word × 1-bit organization
- Full compatible with 100K ECL level
- Address access time: 25ns(max)
- Write pulse width: 25ns (min)
- Output obtainable by wired-OR (open emitter)

■ TRUTH TABLE

Input			Output	Mode
CS	WE	Din		
H	×	×	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	×	Dout*	Read

Notes) × : Irrelevant
* : Read Out Noninvert

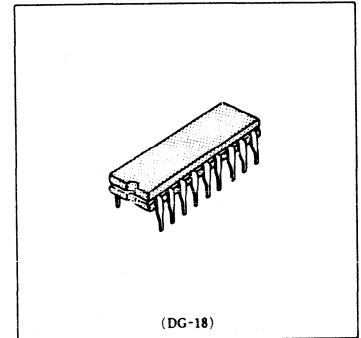
■ BLOCK DIAGRAM



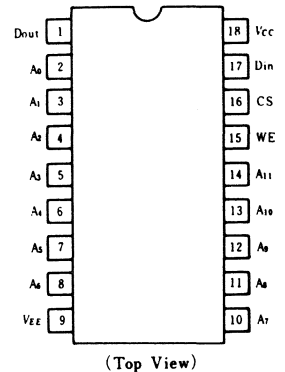
■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias



■ PIN ARRANGEMENT



(Top View)

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -4.5V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{in} = V_{IH}$ or V_{IL}	-1025	-955	-880	mV	
	V_{OL}		-1810	-1715	-1620	mV	
Output Threshold Voltage	V_{ONC}	$V_{in} = V_{IH}$ or V_{ILA}	-1035	—	—	mV	
	V_{OLC}		—	—	-1610	mV	
Input Voltage	V_{IH}	Guaranteed Input Voltage	-1165	—	-880	mV	
	V_{IL}	High/Low for All Inputs	-1810	—	-1475	mV	
Input Current	I_{IH}	$V_{in} = V_{IH}$	—	—	220	μA	
	I_{IL}	$V_{in} = V_{IL}$	\overline{CS}	0.5	—	170	μA
			Others	-50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open	-200	-165	—	mA	

● AC CHARACTERISTICS ($V_{EE} = -4.5V \pm 5\%$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		—	—	10	ns
Chip Select Recovery Time	t_{RCS}		—	—	10	ns
Address Access Time	t_{AA}		—	—	25	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_W	$t_{WSA} = 3ns$	25	—	—	ns
Data Setup Time	t_{WSD}		2	—	—	ns
Data Hold Time	t_{WHD}		2	—	—	ns
Address Setup Time	t_{WSA}		$t_W = t_W \text{ min}$	3	—	—
Address Hold Time	t_{WHA}		2	—	—	ns
Chip Select Setup Time	t_{WSCS}		2	—	—	ns
Chip Select Hold Time	t_{WHCS}		2	—	—	ns
Write Disable Time	t_{WS}		—	—	10	ns
Write Recovery Time	t_{WR}		—	—	27	ns

3. RISE/FALL TIME

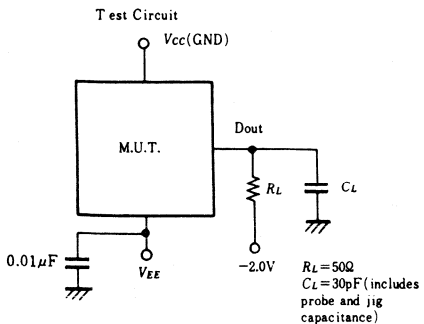
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

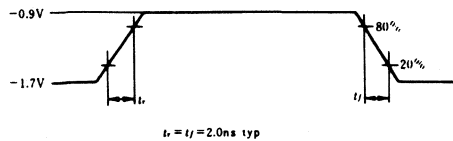
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

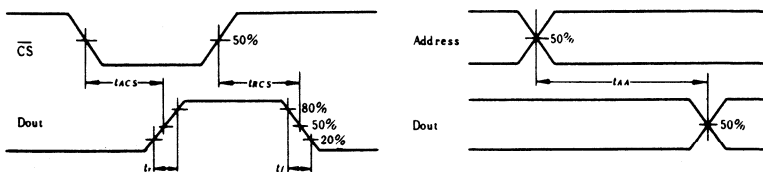
1. LOADING CONDITION



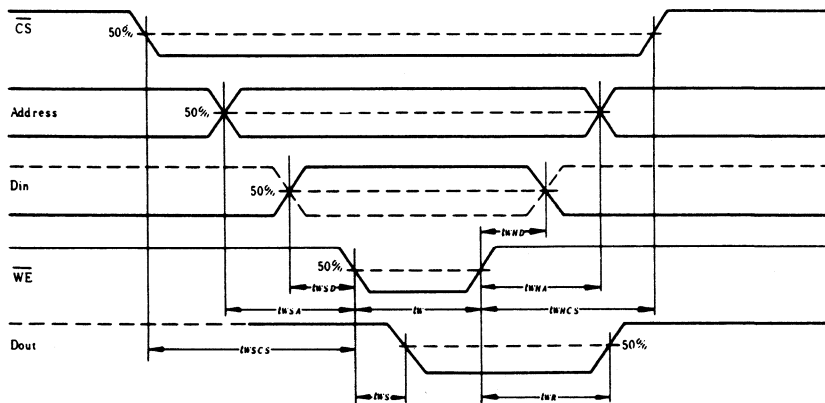
2. INPUT PULSE



3. READ MODE



4. WRITE MODE



HM100480-15, HM100480F-15

Preliminary

16,384-words × 1-bit Fully Decoded Random Access Memory

The HM100480-15 is ECL 100K compatible, 16,384-words x 1-bit, read/write random access memory developed for high speed systems such as scratch pads and control/buffer storages.

The fabrication process uses the Hitachi's U-groove isolation method.

The HM100480-15 is encapsulated in cerdip-20 pin and flat-20 pin package, compatible with Fairchild's 100480.

■ FEATURES

- 16,384-words x 1-bit organization
- Fully compatible with 100K ECL level
- Address access time: 15ns (max)
- Write pulse width: 15ns (min)
- Low power dissipation: 0.06mW/bit
- Output obtainable by wired-OR (open emitter)

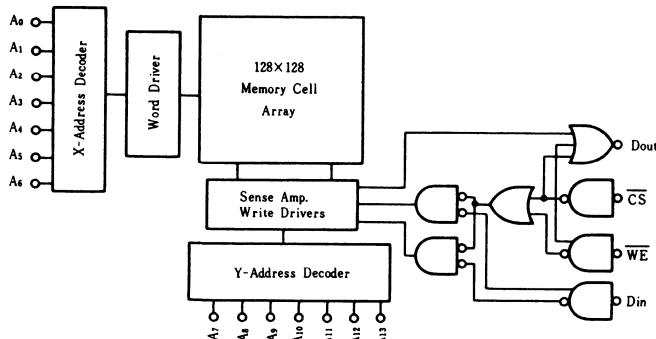
■ TRUTH TABLE

Input			Output	Mode
\overline{CS}	\overline{WE}	Din		
H	X	X	L	Not Selected
L	L	L	L	Write "0"
L	L	H	L	Write "1"
L	H	X	Dout*	Read

Notes) X : Irrelevant

* : Read Out Noninvert

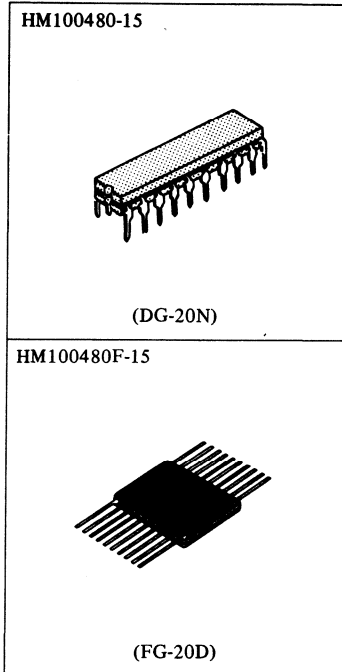
■ BLOCK DIAGRAM



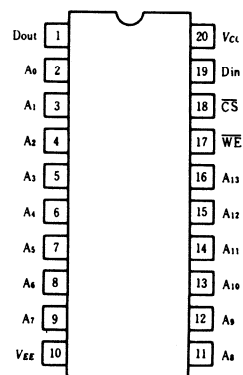
■ ABSOLUTE MAXIMUM RATINGS ($T_a = 25^\circ\text{C}$)

Item	Symbol	Rating	Unit
Supply Voltage	V_{EE} to V_{CC}	+0.5 to -7.0	V
Input Voltage	V_{in}	+0.5 to V_{EE}	V
Output Current	I_{out}	-30	mA
Storage Temperature	T_{stg}	-65 to +150	$^\circ\text{C}$
Storage Temperature	$T_{stg}(\text{Bias})^*$	-55 to +125	$^\circ\text{C}$

* Under Bias



■ PIN ARRANGEMENT



(Top View)

Note)

The specifications of this device are subject to change without notice.

Please contact your nearest Hitachi's Sales Dept. regarding specifications.

■ ELECTRICAL CHARACTERISTICS

● DC CHARACTERISTICS ($V_{EE} = -4.5V$, $R_L = 50\Omega$ to $-2.0V$, $T_a = 0$ to $+85^\circ C$, air flow exceeding 2m/sec)

Item	Symbol	Test Condition	min(B)	typ	max(A)	Unit	
Output Voltage	V_{OH}	$V_{iA} = V_{iHA}$ or V_{iLB}	-1025	-955	-880	mV	
	V_{OL}		-1810	-1715	-1620	mV	
Output Threshold Voltage	V_{OHc}	$V_{iA} = V_{iHB}$ or V_{iLA}	-1035	—	—	mV	
	V_{OLc}		—	—	-1610	mV	
Input Voltage	V_{IH}	Guaranteed Input Voltage	-1165	—	-880	mV	
	V_{iL}	High/Low for All Input	-1810	—	-1475	mV	
Input Current	I_{iH}	$V_{iA} = V_{iHA}$	—	—	220	μA	
	I_{iL}	$V_{iA} = V_{iLB}$	\overline{CS}	0.5	—	170	μA
			Others	-50	—	—	
Supply Current	I_{EE}	All Inputs and Outputs Open	-220	—	—	mA	

● AC CHARACTERISTICS ($V_{EE} = -4.5V \pm 5\%$, $T_a = 0$ to $+75^\circ C$, air flow exceeding 2m/sec)

1. READ MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Chip Select Access Time	t_{ACS}		2	—	8	ns
Chip Select Recovery Time	t_{RCS}		2	—	8	ns
Address Access Time	t_{AA}		3	12	15	ns

2. WRITE MODE

Item	Symbol	Test Condition	min	typ	max	Unit
Write Pulse Width	t_w	$t_{wSA} = 3ns$	15	—	—	ns
Data Setup Time	t_{wSD}		2	—	—	ns
Data Hold Time	t_{wHD}		2	—	—	ns
Address Setup Time	t_{wSA}		$t_w = t_w \text{ min}$	3	—	—
Address Hold Time	t_{wHA}		3	—	—	ns
Chip Select Setup Time	t_{wSCS}		2	—	—	ns
Chip Select Hold Time	t_{wHCS}		2	—	—	ns
Write Disable Time	t_{wS}		—	—	12	ns
Write Recovery Time	t_{wR}		—	—	17	ns

3. RISE/FALL TIME

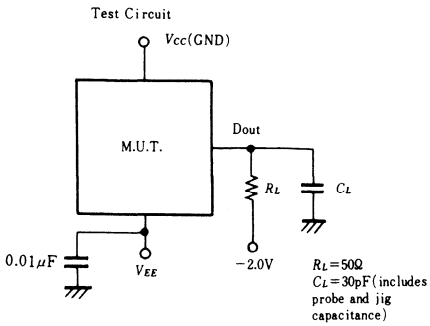
Item	Symbol	Test Condition	min	typ	max	Unit
Output Rise Time	t_r		—	2	—	ns
Output Fall Time	t_f		—	2	—	ns

4. CAPACITANCE

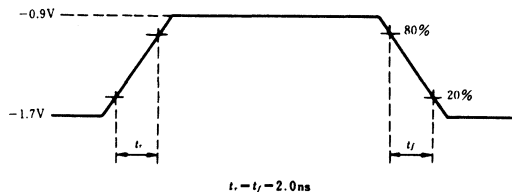
Item	Symbol	Test Condition	min	typ	max	Unit
Input Capacitance	C_{in}		—	3	—	pF
Output Capacitance	C_{out}		—	5	—	pF

■ TEST CIRCUIT AND WAVEFORMS

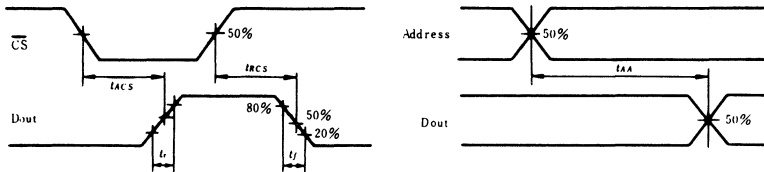
1. LOADING CONDITION



2. INPUT PULSE



3. READ MODE



4. WRITE MODE

